Ultralow, I_Q, anyCAP® Low Dropout Regulator

ADP3342

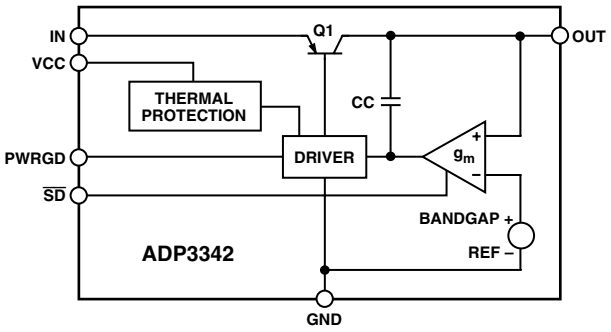
FEATURES

Accuracy Over Line and Load: ±4.0% @ 25°C, ±5% Over Temperature
Ultralow Dropout Voltage: 300 mV (Typ) @ 300 mA
Requires Only C_O = 1.0 µF for Stability
anyCAP = Stable with any Type of Capacitor (including MLCC)
Current and Thermal Limiting
Low Shutdown Current: < 2 µA
1.7 V ≤ V_{IN} ≤ 6 V
2.8 V ≤ VCC ≤ 6 V
V_{OUT} = 1.2 V ±5%
–40°C to +100°C Ambient Temperature Range
Ultrasmall Thermally Enhanced 8-Lead MSOP Package

APPLICATIONS

Notebook PCs
Desktop PCs

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3342 is a unique member of the ADP330x family of precision low dropout anyCAP voltage regulators. The ADP3342 operates with an input voltage range of 1.7 V to 6 V and delivers a continuous load current up to 300 mA. In order to support the ability to regulate from such a low input voltage, the power rail to the IC, VCC, has been split off from the main power rail, V_{IN}, from which the output is powered.

The ADP3342 stands out from the conventional LDOs with the lowest thermal resistance of any MSOP-8 package and an enhanced process that enables it to offer performance advantages beyond its competition. Its patented design requires only a 1.0 µF output capacitor for stability. This device is insensitive to output capacitor Equivalent Series Resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. The dropout voltage of the ADP3342 is only 190 mV (typical) at 300 mA. This device also includes a safety current limit, thermal overload protection and a shutdown control pin.

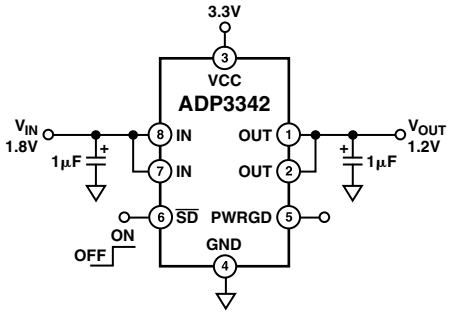


Figure 1. Typical Application Circuit

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REV. 0

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ADP3342–SPECIFICATIONS

(VCC = 3.0 V, V_{IN} = 1.8 V, C_{IN} = C_{OUT} = 1 μF, T_A = 0°C to 100°C and T_A = –40°C to +100°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy	V_{OUT}	VCC = 2.8 V to 6 V, V_{IN} = 1.7 V to 6 V I_L = 0.1 mA to 300 mA T_A = 25°C	–4.0		+4.0	%
		VCC = 2.8 V to 6 V, V_{IN} = 1.7 V to 6 V I_L = 0.1 mA to 300 mA, T_A = –40°C to +100°C	–5.0		+5.0	%
Line Regulation		VCC = 2.8 V to 6 V, V_{IN} = 1.7 V to 6 V T_A = 25°C		0.04		mV/V
Load Regulation		I_L = 0.1 mA to 300 mA T_A = 25°C		0.12		mV/mA
Dropout Voltage	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 300 mA		190	450	mV
		I_L = 200 mA		125		mV
		I_L = 100 mA		70		mV
Current Limiting	I_{LIM}	VCC = 3 V, V_{IN} = 1.8 V		450		mA
Output Noise	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 1 μF I_L = 300 mA		60		μV rms
OPERATING CURRENTS						
Ground Current in Regulation	I_{GND}	I_L = 300 mA, T_A = –40°C to +100°C		3.0	8.5	mA
		I_L = 300 mA, T_A = 0°C to 100°C		3.0	6.0	mA
		I_L = 300 mA, T_A = 25°C		3.0	4.0	mA
		I_L = 200 mA		2.0		mA
		I_L = 0.1 mA		100	175	μA
VCC Current in Regulation	IVCC	I_L = 300 mA		100	170	μA
Ground Current in Shutdown	I_{GNDSD}	SD = 0 V, VCC = 6 V, V_{IN} = 1.8 V		0.01	2	μA
SHUTDOWN						
Threshold Voltage	V_{THSD}	ON	VCC – 0.9			V
		OFF			0.6	V
SD Input Current	I_{SD}	0 ≤ SD ≤ 6 V		1.4	7	μA
Output Current In Shutdown	I_{OSD}	T_A = 25°C VCC = 6 V, V_{IN} = 6 V		0.01	1	μA
		T_A = 100°C VCC = 6 V, V_{IN} = 6 V		0.01	2	μA
PWRGD						
Power Good Output Voltage	I_{PWRGDL}	V_{PWRGD} = 1.2 V, VCC = 3.0 V	0.85	1.5		mA
	V_{PWRGDL}[2]	I_{PWRGD} = 300 μA			0.4	V
	V_{PWRGDH}[2]	I_{PWRGD} = 300 μA	VCC – 0.4			V
Power Good On Time Delay	TD1[3]	I_L = 3 mA to 300 mA, C_{OUT} = 1 μF to 10 μF	5		300	μs
	TD2[4]	I_L = 3 mA to 300 mA, C_{OUT} = 1 μF to 10 μF	50		300	μs
Power Good Off Time Delay	TD3[5]	I_L = 3 mA to 300 mA, C_{OUT} = 1 μF to 10 μF	0.05		1	μs
THERMAL PROTECTION						
Shutdown Temperature	TH_{PROT}	I_L = 100 mA		165		°C

NOTES

[1]Ambient temperature of 100°C corresponds to a junction temperature of 125°C under typical full load test conditions.

[2]V_{PWRGDL}, V_{PWRGDH},: Powergood output voltages. Guaranteed by design and characterization.

[3]TD1: Delay time from V_{OUT} crossing 1 V to PWRGD high. Guaranteed by design.

[4]TD2: Delay time from $\overline{SD}$ high to PWRGD high. Guaranteed by design.

[5]TD3: Delay time between $\overline{SD}$ low to PWRGD low. Guaranteed by design.

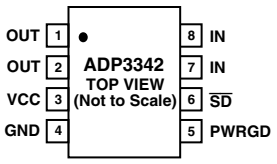
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage . . . . . –0.3 V to +13 V
Shutdown Input Voltage . . . . . –0.3 V to +13 V
Power Dissipation . . . . . Internally Limited
Operating Ambient Temperature Range . . . –40°C to +100°C
Operating Junction Temperature Range . . . –40°C to +125°C
θ_{JA} (2-layer) . . . . . 157°C/W
θ_{JA} (4-layer) . . . . . 121°C/W
θ_{JC} . . . . . 56°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN CONFIGURATION



ORDERING GUIDE

Model	Output Voltage*	Package Option	Marking Code	Temperature Range
ADP3342JRM-REEL7	1.2 V	RM-8 (MSOP-8)	LJA	0°C to 100°C
ADP3342ARM-REEL7	1.2 V	RM-8 (MSOP-8)	LJB	–40°C to +100°C

*Contact the factory for other output voltage options.

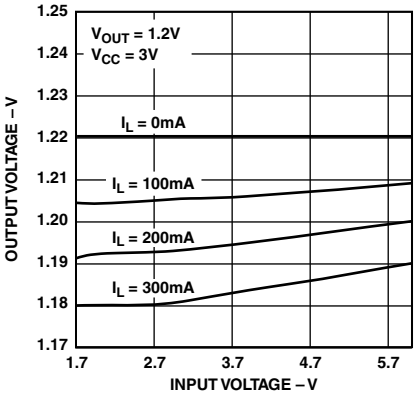
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 2	OUT	Output of the Regulator. Bypass to ground with a 1.0 µF or larger capacitor. All pins must be connected together for proper operation.
3	VCC	Supply Voltage
4	GND	Ground Pin
5	PWRGD	Power Good. Used to indicate output is in regulation.
6	SD	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shut down is not used, this pin should be connected to the input pin.
7, 8	IN	Regulator Input. All pins must be connected together for proper operation.

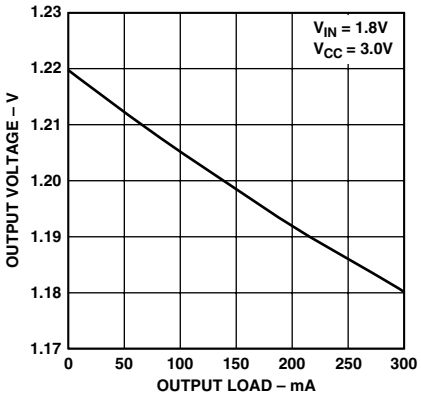
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3342 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

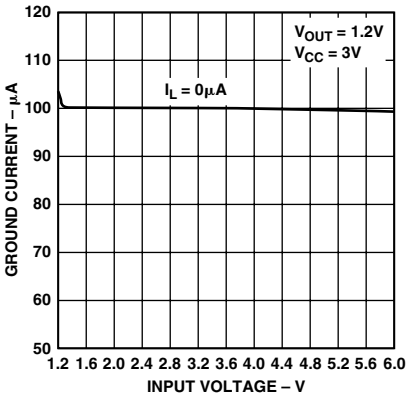
ADP3342–Typical Performance Characteristics



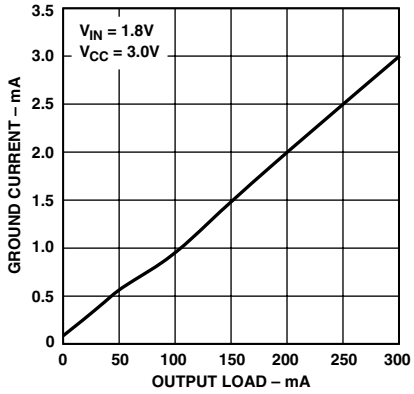
TPC 1. Line Regulation Output Voltage vs. Supply Voltage



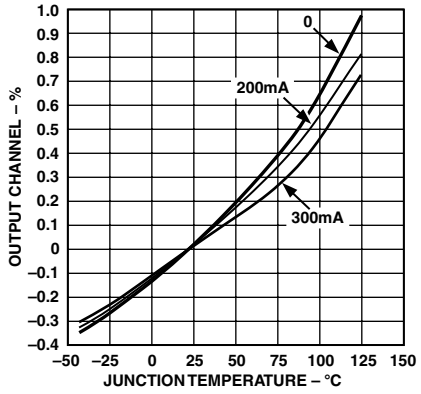
TPC 2. Output Voltage vs. Load Current



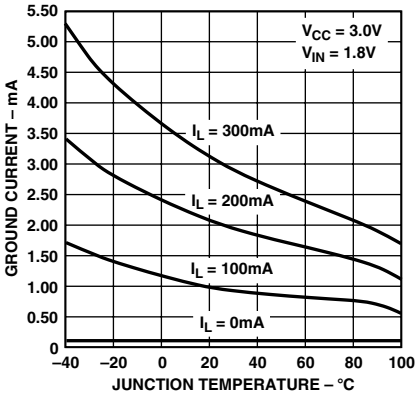
TPC 3. Ground Current vs. Supply Voltage



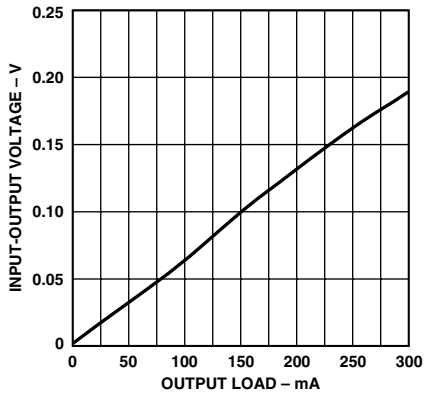
TPC 4. Ground Current vs. Load Current



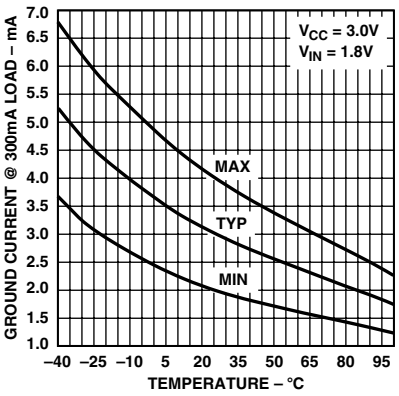
TPC 5. Output Voltage Variation vs. Junction Temperature



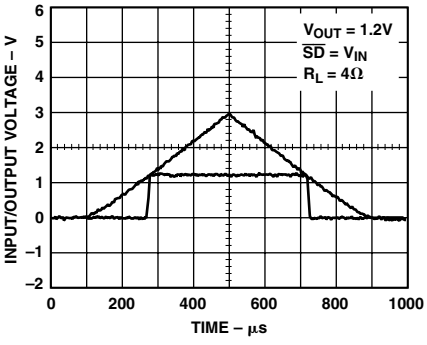
TPC 6. Ground Current vs. Junction Temperature



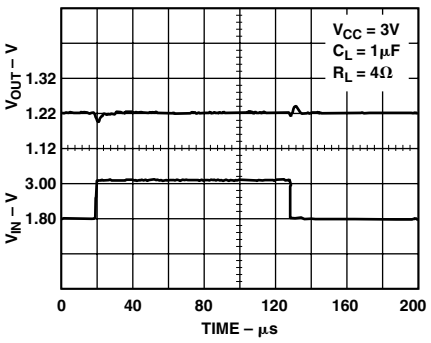
TPC 7. Dropout Voltage vs. Output Current



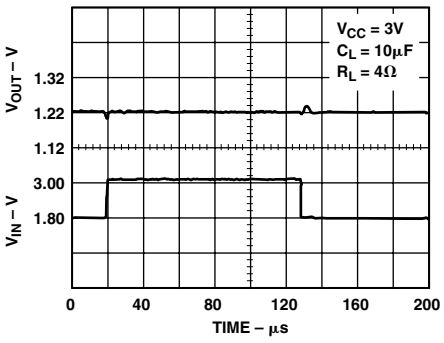
TPC 8. Ground Current @ 300 mA Load vs. Ambient Temperature



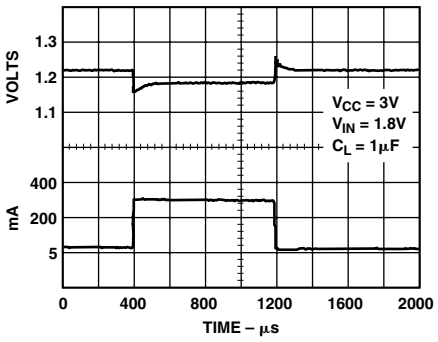
TPC 9. Power-Up/Power-Down



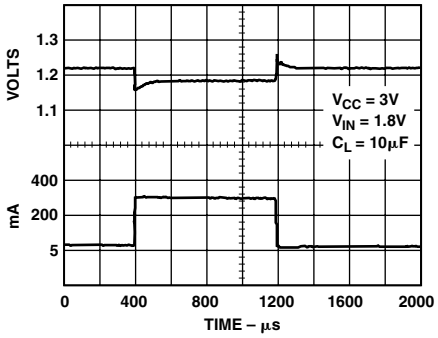
TPC 10. Line Transient Response



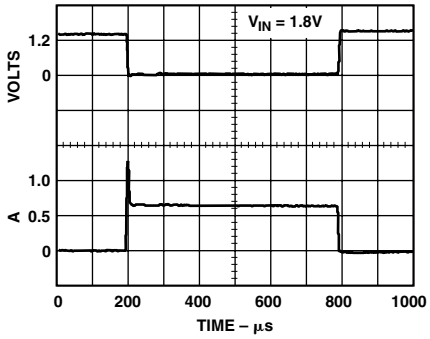
TPC 11. Line Transient Response



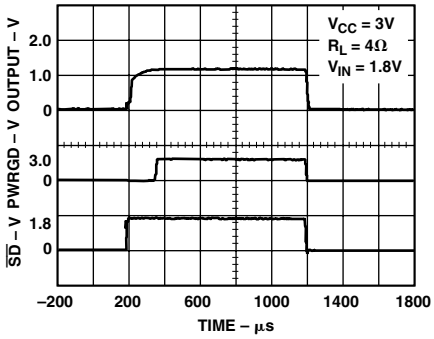
TPC 12. Load Transient Response



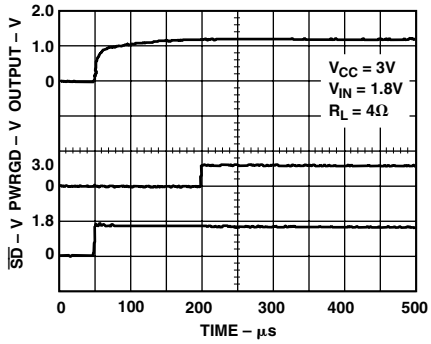
TPC 13. Load Transient Response



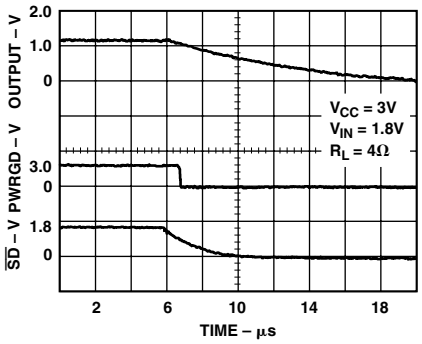
TPC 14. Short Circuit Current



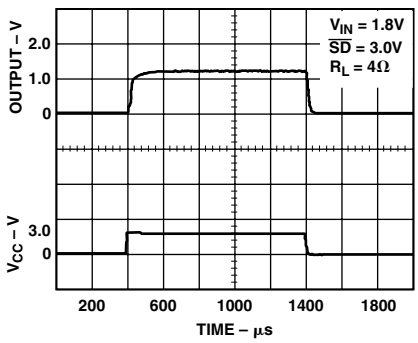
TPC 15. Power-On/Power-Off Response from Shutdown



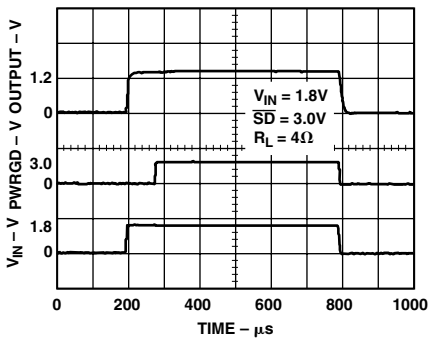
TPC 16. Turn On Delay



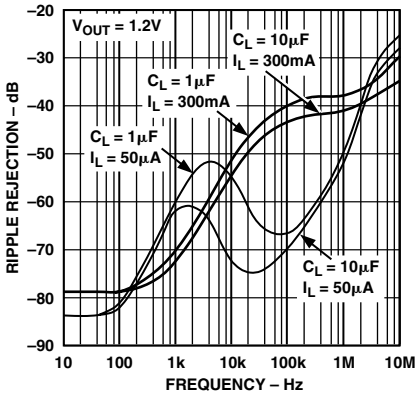
TPC 17. Turn Off Delay



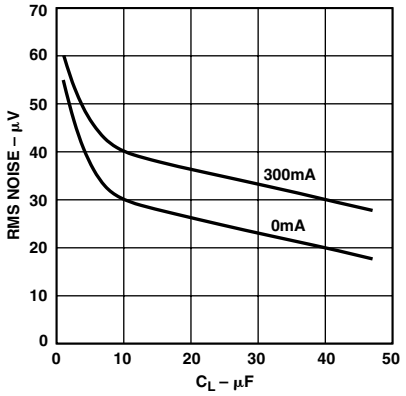
TPC 18. Power-On/Power-Off Response from V_{CC}



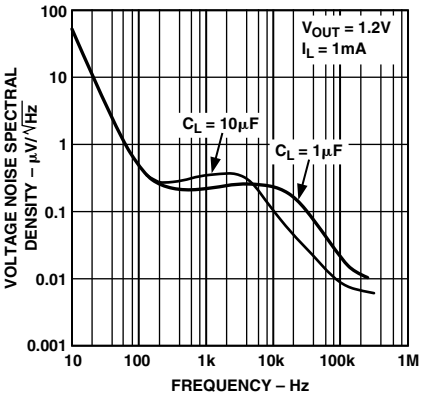
TPC 19. Power On/Power Off Response from V_{IN}



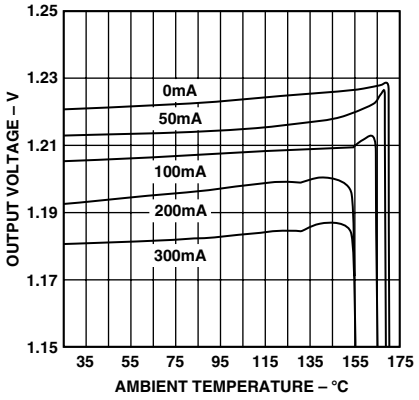
TPC 20. Power Supply Ripple Rejection



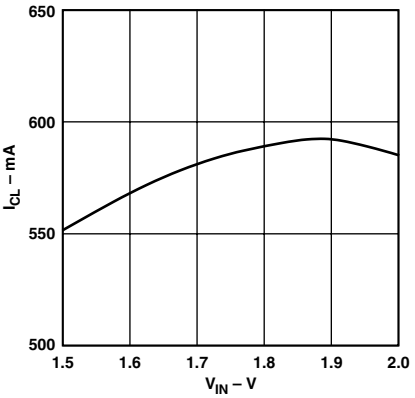
TPC 21. RMS Noise vs. C_L (10 Hz–100 Hz)



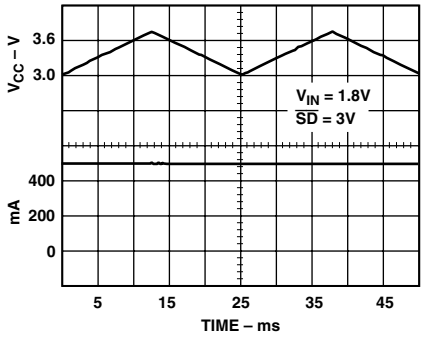
TPC 22. Output Noise Density



TPC 23. Thermal Protection



TPC 24. Current Limit vs. V_{IN}



TPC 25. Current Limiting from V_{CC}

THEORY OF OPERATION

The new anyCAP LDO ADP3342 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

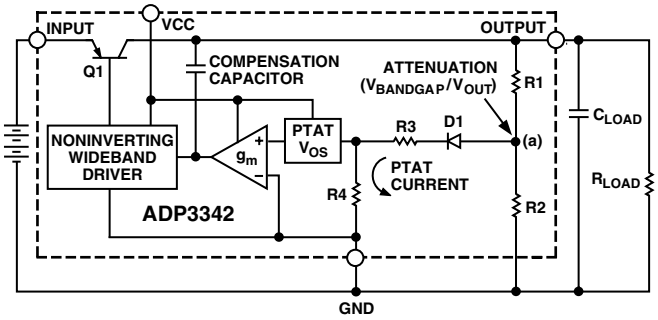


Figure 2. Control Loop Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature proportional input "offset voltage" that is repeatable and very well controlled. The temperature proportional offset voltage is combined with the complementary diode voltage to form a "virtual bandgap" voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3342 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain which leads to excellent line and load regulation.

Additional features of the circuit include current limit and thermal shutdown and noise reduction.

APPLICATION INFORMATION

PC Application—VCCVID

The ADP3342 has been optimized for PC applications that require a 1.2 V output for powering the voltage identification rail, VCCVID. The rail from which the output draws current, the IN pin, is separated from the rail that powers the IC, the VCC pin. This allows a higher efficiency design when, as recommended for the IMVP-3 application, the VCC pin is connected to a 3.3 V supply to power the IC adequately, and the IN pin is connected to a 1.8 V supply. The efficiency is nearly 60% in this case.

Capacitor Selection

As with any voltage regulator, output transient response is a function of the output capacitance. The ADP3342 is stable with a wide range of capacitor values, types and ESR (anyCAP). A capacitor as low as 1 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3342 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types may fall below the minimum at cold temperature. Ensure that the capacitor provides more than 1 µF at minimum temperature.

Input Bypass Capacitor

An input bypass capacitor is not strictly required but is advisable in any application involving long input wires or high source impedance. Connecting a 1 µF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

Power Good Monitoring Function

The PWRGD pin does not monitor the output voltage directly, but rather detects whether the internal PNP pass transistor is being modulated by the regulation loop. This means of detecting PWRGD, rather than using a voltage threshold detection, provides an inherent and desirable delay in asserting the PWRGD signal. During startup or overload, the regulation loop is not in control, so the PWRGD pin is low.

Shutdown Mode

Applying a TTL high signal to the shutdown ($\overline{SD}$) pin or tying it to the input pin, will turn the output ON. Pulling $\overline{SD}$ down to 0.4 V or below, or tying it to ground will turn the output OFF. In shutdown mode, quiescent current is reduced.

Paddle-Under-Lead Package

The ADP3342 uses a patented paddle-under-lead package design to ensure the best thermal performance in an MSOP-8 footprint. This new package uses an electrically isolated die attach that allows all pins to contribute to heat conduction. This technique reduces the thermal resistance to 110°C/W on a 4-layer board as compared to >160°C/W for a standard MSOP-8 leadframe.

Thermal Overload Protection

The ADP3342 is protected against damage due to excessive power dissipation by its thermal overload protection circuit which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be limited by operating conditions so that junction temperatures will not exceed 150°C.

Calculating Junction Temperature

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})I_{LOAD} + (V_{IN})I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are input and output voltages respectively.

Assuming I_{LOAD} = 300 mA, I_{GND} = 4 mA, V_{IN} = 1.8 V and V_{OUT} = 1.2 V, device power dissipation is:

$$P_D = (1.8 - 1.2)\ 300\ mA + (1.8)\ 4\ mA = 187\ mW$$

The proprietary package used in the ADP3342 has a thermal resistance of 110°C/W, significantly lower than a standard MSOP-8 package. Assuming a 4-layer board, the junction temperature rise above ambient temperature will be approximately equal to:

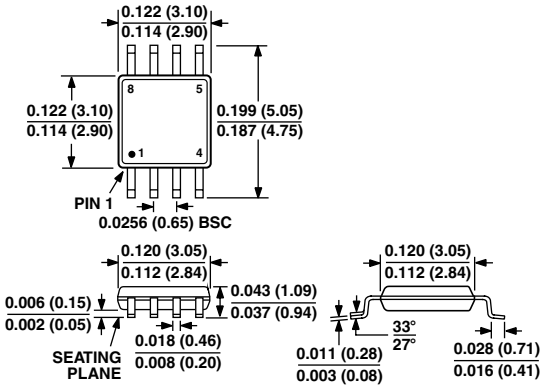
$$\Delta T_{JA} = 0.187\,W \times 110°C/W = 20.6°C$$

C02712–.8–1/02(0)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Micro SOIC (MSOP)
(RM-8)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS. INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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