

FEATURES

- Guaranteed V_{OS} 500 μ V Max
- Guaranteed Matched CMRR 94dB Min
- Guaranteed Matched V_{OS} 750 μ V Max
- RC/RM4136 Direct Replacement (OP-09)
- LM148/LM348 Direct Replacement (OP-11)
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short-Circuit Protection
- Low Input Bias Current
- Available in Die Form

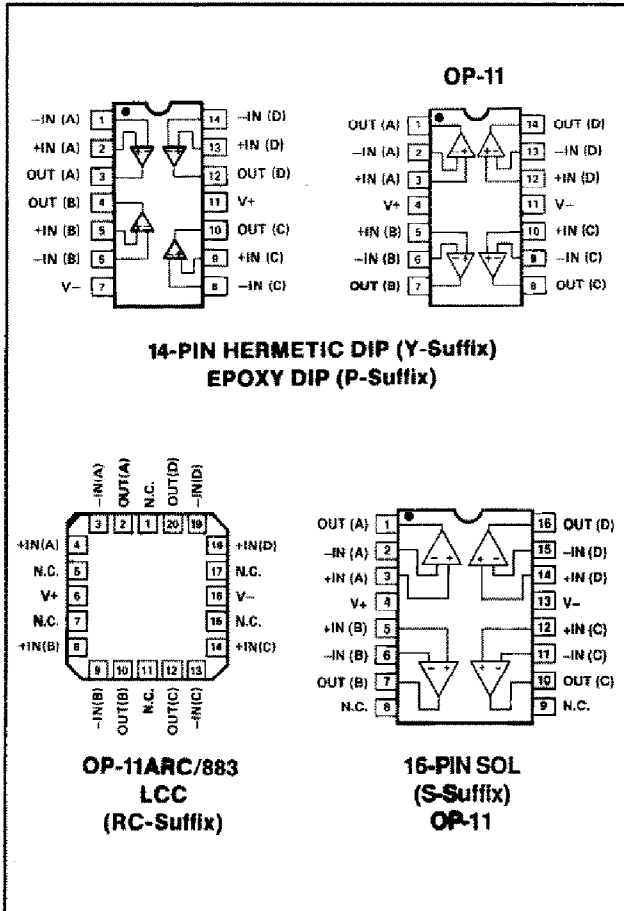
ORDERING INFORMATION [†]

$T_A = +25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC 20-CONTACT	
0.5	OP09AY*	-	-	MIL
	OP11AY*	-	OP11ARC/883	
0.5	OP09EY	-	-	COM
	OP11EY	OP11EP	-	
2.5	OP11BY*	-	-	MIL
2.5	-	OP09FP	-	XIND
	OP11FY	OP11FP	-	
5.0	OP11CY/883	-	-	MIL
5.0	-	OP11GP	-	XIND
	-	OP11GS	-	

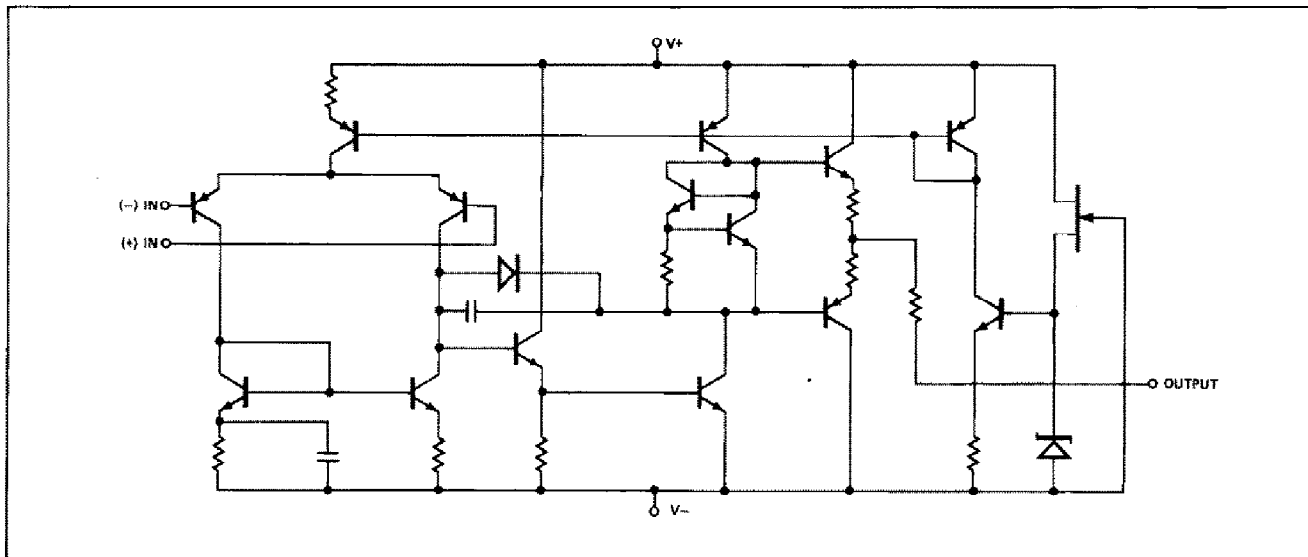
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



OP-09/OP-11

GENERAL DESCRIPTION

The OP-09 and OP-11 provide four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148, LM348, RM4156, and HA4741 amplifiers. The OP-09 is pin compatible with the RM4136 and RC4136. The amplifiers are matched for common-mode rejection ratio and offset voltage which is very important in designing instrumentation amplifiers. In addition, the amplifier is designed to have equal positive-going and negative-going slew rates. This is an important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift, and excellent long-term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise", provides high reliability, and assures long-term stability of parameters.

The OP-09 and OP-11 are ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance.

OP-09's and OP-11's with processing per the requirements of MIL-STD-883 are available. For dual-741-type versions, see the OP-04/14 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±22V
OP-09GR and OP-11GR (Only)	±18V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
	(One Amplifier Only)

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.5	0.75	—	0.8	2.0	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$	—	1	20	—	1	20	$\mu V/V$
		$V_{CM} = \pm 12V$	94	120	—	94	120	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-09A, OP-09B, OP-11A, OP-11B, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-09E, OP-11E and $-40^\circ C \leq T_A \leq +85^\circ C$ for OP-09F, OP-11F, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.6	1.0	—	1.0	2.5	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$	—	3.2	20	—	3.2	20	$\mu V/V$
		$V_{CM} = \pm 12V$	94	110	—	94	110	—	dB

Storage Temperature Range

RC, Y-Package	-65°C to +150°C
P-Package	-65°C to +125°C

Lead Temperature Range (Soldering, 60 sec) 300°C

Junction Temperature (T_J) -65°C to +150°C

Operating Temperature Range

OP-09A, OP-09B	-55°C to +125°C
OP-09E	0°C to +70°C
OP-09F	-40°C to +85°C
OP-11A, OP-11B, OP-11C, OP-11ARC	-55°C to +125°C
OP-11E	0°C to +70°C
OP-11F, OP-11G	-40°C to +85°C

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
20-Contact LCC (RC)	98	33	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$ $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A/E OP-11A/E			OP-09B/F OP-11B/F			OP-11C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.3	0.5	—	0.6	2.5	—	1.2	5.0	mV
Input Offset Current	I_{OS}		—	5.5	20	—	25	50	—	75	200	nA
Input Bias Current	I_B		—	180	300	—	300	500	—	300	500	nA
Input Resistance Differential Mode	R_{IN}	(Note 3)	0.17	0.29	—	0.1	0.17	—	0.1	0.17	—	M Ω
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V, R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V,$ $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \leq 2k\Omega, V_O = \pm 10V$	100	650	—	100	650	—	50	500	—	V/mV
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	105	180	—	123	180	—	210	340	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.7	—	—	0.7	—	—	0.7	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	—	18	—	—	18	—	nV/\sqrt{Hz}
		$f_O = 100Hz$	—	14	—	—	14	—	—	14	—	
		$f_O = 1000Hz$	—	12	—	—	12	—	—	12	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	17	—	—	17	—	—	17	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.8	—	—	1.8	—	—	1.8	—	pA/\sqrt{Hz}
		$f_O = 100Hz$	—	1.5	—	—	1.5	—	—	1.5	—	
		$f_O = 1000Hz$	—	1.2	—	—	1.2	—	—	1.2	—	
Channel Separation	CS		100	130	—	100	130	—	—	130	—	dB
Slew Rate (Note 2)	SR		0.7	1.0	—	0.7	1.0	—	0.7	1.0	—	V/ μs
Large-Signal Bandwidth (Note 2)		$V_O = 20V_{p-p}$	11	16	—	11	16	—	11	16	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	2.4	3.0	—	2.4	3.0	—	2.4	3.0	—	MHz
Risetime (Note 2)	t_r	$A_V = +1, V_{IN} = 50mV$	—	110	145	—	110	145	—	110	145	ns
Overshoot (Note 2)	OS		—	15	25	—	15	25	—	15	25	%

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed by input bias current.
4. Guaranteed by risetime.

OP-09/OP-11

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A OP-11A			OP-09B OP-11B			OP-11C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	1.0	—	1.0	3.5	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 3)	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	20	40	—	40	80	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	$nA/^\circ C$
Input Bias Current	I_B		—	200	375	—	400	650	—	400	800	nA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-09E, OP-11E, $-40^\circ C \leq T_A \leq +85^\circ C$ for OP-09F, OP-11F, OP-11G, unless otherwise noted.

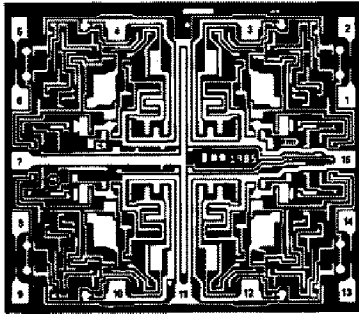
PARAMETER	SYMBOL	CONDITIONS	OP-09E OP-11E			OP-09F OP-11F			OP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	0.8	—	0.8	3.0	—	1.5	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	14	30	—	40	60	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	$nA/^\circ C$
Input Bias Current	I_B		—	200	350	—	400	550	—	400	800	nA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed but not tested.

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

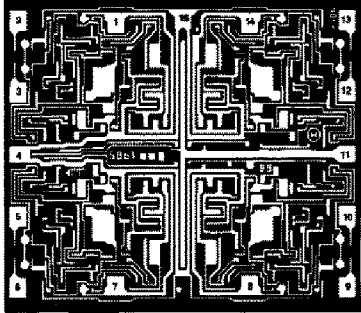
OP-09



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V-
8. INVERTING INPUT (C)
9. NONINVERTING INPUT (C)
10. OUTPUT (C)
11. V+
12. OUTPUT (D)
13. NONINVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V+

DIE SIZE 0.086 × 0.072 inch, 6192 sq. mils
(2.18 × 1.83 mm, 3.99 sq. mm)

OP-11



1. OUTPUT (A)
2. INVERTING INPUT (A)
3. NONINVERTING INPUT (A)
4. V+
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. OUTPUT (B)
8. OUTPUT (C)
9. INVERTING INPUT (C)
10. NONINVERTING INPUT (C)
11. V-
12. NONINVERTING INPUT (D)
13. INVERTING INPUT (D)
14. OUTPUT (D)
15. V+

DIE SIZE 0.086 × 0.072 inch, 6192 sq. mils
(2.18 × 1.83 mm, 3.99 sq. mm)

NOTE:
Either or both V+ pads may be used without any change in performance.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-09/11N, OP-09/11G and OP-09/11GR devices; $T_A = 125^\circ C$ for OP-09/11NT and OP-09/11GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT LIMIT	OP-09N OP-11N LIMIT	OP-09GT OP-11GT LIMIT	OP-11G LIMIT	OP-09GR OP-11GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	1.0	0.5	3.5	2.5	5.0	mV MAX
Input Offset Current	I_{OS}		20	20	50	50	200	nA MAX
Input Bias Current	I_B		300	300	500	500	500	nA MAX
Input Voltage Range	IVR		± 12	± 12	± 12	± 12	± 12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$ $R_S \leq 10k\Omega$	100	100	100	100	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$ $R_S \leq 10k\Omega$	32	32	32	32	100	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L = 2k\Omega$	± 11 ± 11	± 12 ± 11	± 11 ± 11	± 12 ± 11	± 11 ± 11	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	50	100	50	V/mV MIN
Power Consumption (Four Amplifiers)	P_d	$V_{OUT} = 0$ No Load	200	180	200	180	340	mW MAX

NOTES:

For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

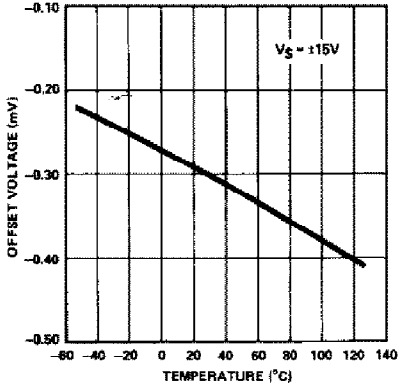
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT TYPICAL	OP-09N OP-11N TYPICAL	OP-09GT OP-11GT TYPICAL	OP-11G TYPICAL	OP-09GR OP-11GR TYPICAL	UNITS
Slew Rate	SR	$A_V = 1$ $R_L \geq 2k\Omega$	1	1	1	1	1	V/ μs
Unity Gain Bandwidth	GBW		2	2	2	2	2	MHz
Channel Separation	CS	$A_V = 100$ $f = 10kHz$ $R_S = 1k\Omega$	130	130	130	130	130	dB

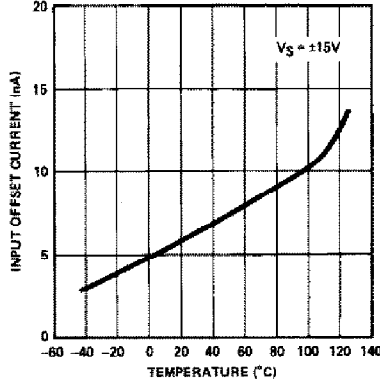
OP-09/OP-11

TYPICAL PERFORMANCE CHARACTERISTICS

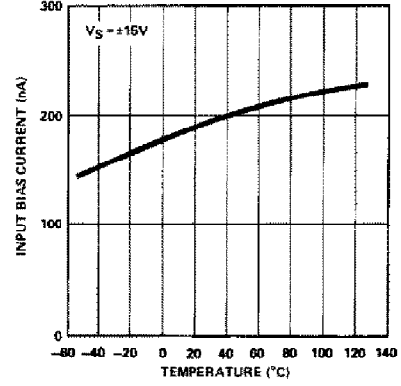
INPUT OFFSET VOLTAGE vs TEMPERATURE



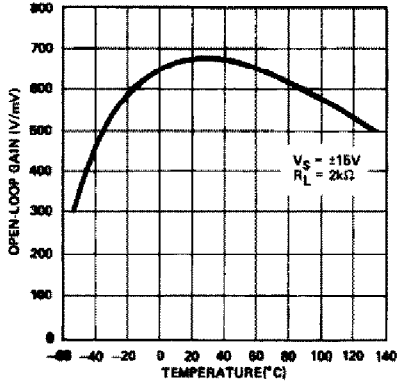
OFFSET CURRENT vs TEMPERATURE



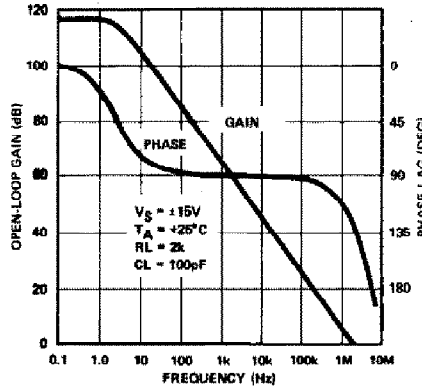
BIAS CURRENT vs TEMPERATURE



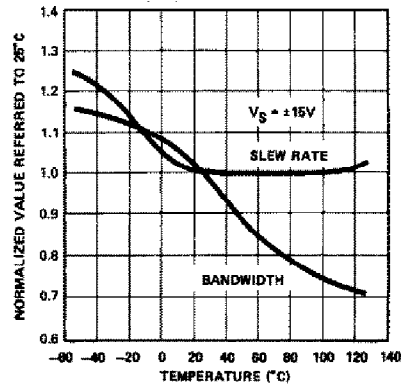
OPEN-LOOP GAIN vs TEMPERATURE



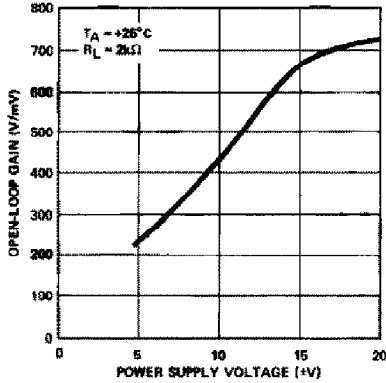
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



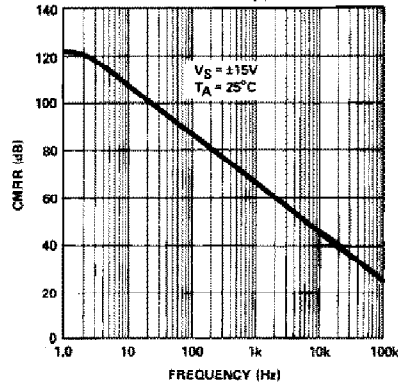
NORMALIZED SLEW RATE AND BANDWIDTH vs TEMPERATURE



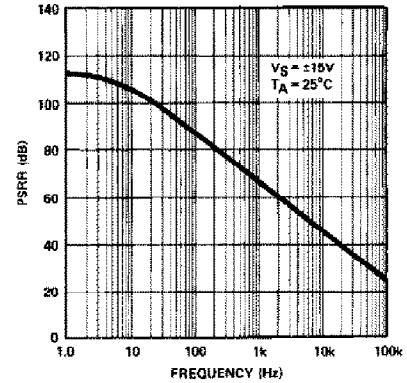
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



CMRR vs FREQUENCY



PSRR vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS

