

**1.0 SCOPE**

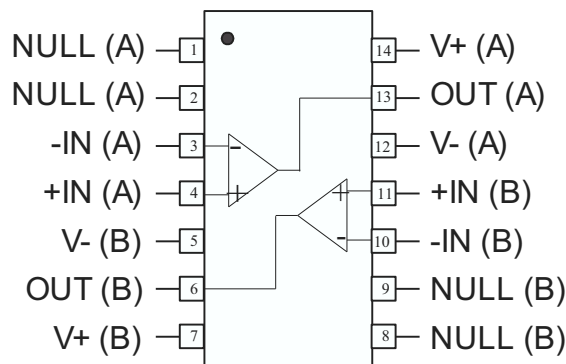
This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>. This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at [www.analog.com/OP227](http://www.analog.com/OP227).

**2.0 Part Number.** The complete part number(s) of this specification follow:

Part Number	Description
OP227R903Y	Radiation Tested, Dual, low-offset, low noise operational amplifier
OP227R903M	Radiation Tested, Dual, low-offset, low noise operational amplifier

**2.1 Case Outline.**

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Y	GDIP1-T14	14-Lead ceramic dual-in-line package (CERDIP)
M	GDFP1-F14	14-Lead ceramic flat pack (CERPAK)


**NOTES:**

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B
2. V-(A) and V-(B) are internally connected via substrate resistance.

Figure 1 - Terminal connections.

**3.0 Absolute Maximum Ratings. 1/**

Supply voltage (V ) .....	±22 V dc CC
Input voltage range (V ) .....	±22 V dc IN
Output short circuit duration .....	.Indefinite
Differential input current 2/ .....	±25 mA
Differential input voltage range .....	±0.7 V dc
Lead temperature (soldering, 60 seconds) .....	+300°C
Storage temperature range ..	-65°C to +150°C
Maximum power dissipation (P <sub>D</sub> ) 3/ .....	500 mW
Junction Temperature (T <sub>J</sub> ).....	150°C

NOTES:

- 1/ Unless otherwise specified, all voltages are referenced to ground.
- 2/ The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current should be limited to 25 mA.
- 3/ For T greater than 106°C, derate linearly at 11.3 mW/°C.

**3.1 Thermal Characteristics:**

- Thermal Resistance, Y (cerdip) Package
  - Junction-to-Case ( $\Theta_{JC}$ ) = 29°C/W Max
  - Junction-to-Ambient ( $\Theta_{JA}$ ) = 91°C/W Max
- Thermal Resistance, M (cerpak) Package
  - Junction-to-Case ( $\Theta_{JC}$ ) = 90°C/W Max
  - Junction-to-Ambient ( $\Theta_{JA}$ ) = 150°C/W Max

4.0 Electrical Table:

Parameter See notes at end of table	Symbol	Conditions Note 1	Sub-group	Limit Min	Limit Max	Units	
Input Offset Voltage	V <sub>IO</sub>		1		80	μV	
			2, 3		180		
			M, D, L, R	1			160
Average input offset drift <u>2/ 4/</u>	TCV <sub>IO</sub>		1,2,3		1.0	μV/°C	
Input offset current	I <sub>IO</sub>		1		±35	nA	
			2,3		±50		
			M, D, L, R	1			±120
Input bias current	I <sub>B</sub>		1		±40		
			2,3		±60		
			M, D, L, R	2, 3			±1200
Power supply rejection ratio <u>4/</u>	PSRR	V <sub>S</sub> = ±4V to ±18V	1		10	μV/V	
		V <sub>S</sub> = ±4.5V to ±18V	2, 3		16		
Common mode rejection ratio <u>4/</u>	CMRR	V <sub>CM</sub> = ±11V	1	114		dB	
		V <sub>CM</sub> = ±10V	2, 3	108			
Large signal voltage gain	A <sub>VOL</sub>	V <sub>O</sub> = ±10V, R <sub>L</sub> = 2KΩ	4	1000		V/mV	
			5,6	600			
			M, D, L, R	4	500		
			V <sub>O</sub> = ±10V, R <sub>L</sub> = 600Ω	4	800		
Input voltage range <u>4/</u>	IVR		1	±11		V	
			2,3	±10			
Output voltage range <u>4/</u>	V <sub>O</sub>	R <sub>L</sub> = 2KΩ	4	±12			
			5,6	±11.5			
			R <sub>L</sub> = 600Ω	4	±10		
Slew rate <u>2/ 4/</u>	SR	R <sub>L</sub> = 2KΩ	7	1.7		V/μS	
Input noise voltage <u>4/</u>	e <sub>N</sub>	f <sub>0</sub> = 1 to 100Hz	7		50	nV <sub>RMS</sub>	
Gain bandwidth product <u>2/ 4/</u>	GBW	f = 100kHz	7	5.0		MHz	
Input offset voltage match <u>4/</u>	V <sub>OS</sub>		1		80	μV	
			2,3		180		
Average non-inverting bias current <u>4/</u>	I <sub>E+</sub>	<u>3/</u>	1		±40	nA	
			2,3		±60		
Non-inverting offset current <u>4/</u>	I <sub>OS+</sub>	I <sub>OS+</sub> = I <sub>B+</sub> A - I <sub>E+</sub> B	1		±60		
			2,3		±90		
Inverting offset current <u>4/</u>	I <sub>OS-</sub>	I <sub>OS-</sub> = I <sub>B-</sub> A - I <sub>E-</sub> B	1		±60		
			2,3		±90		

TABLE I NOTES:

1/ V<sub>S</sub> = ±15V, unless otherwise specified

2/ Guaranteed but not tested.

$$3/ I_{B+} = \frac{(I_{B-} + A) + (I_{B+} + B)}{2}$$

4/ Not tested post irradiation.

**4.1 Electrical Test Requirements:**

<b>Table II</b>	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.  
2/ See Table III for delta parameters. See table I for conditions.

**4.2 Table III. Burn-in/Life Test delta limits.**

<b>Table III</b>				
TEST TITLE	BURN-IN ENDPOINT	GROUP C ENDPOINT	DELTA LIMIT	UNITS
VOS	±80	±180	±100	μV
±IB	±40	±50	±10	nA

**5.0 Life Test/Burn-In Circuit:**

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	7/18/2000
B	Update web address	2/18/2002
C	Add note 2 to TCVIO, Guaranteed if not tested, ref SMD 86887	11/22/2002
D	Update web address. Add note 4 to indicate parameters not test post irradiation	5/13/2003
E	Delete burn-in and radiation bias circuits	8/5/2003
F	Add OP227-903M & OP227R903M versions	7/29/2004
G	Update header/footer and add to 1.0 Scope description.	2/25/2008
H	Add Junction Temperature(T <sub>J</sub> ) 150°C to 3.0 Absolute Max Ratings	3/28/2008
I	Remove obsolete part numbers and update ASD to ADI Standard	11/8/2011