ANALOG DEVICES

High Speed, Dual Operational Amplifier

OP-271

FEATURES

- **Excellent Speed .... 8.5V/µs Typ**
- **Fast Settling (0.01%) .... 2µs Typ**
- **Unity-Gain Stable**
- **High Gain-Bandwidth .... 5MHz Typ**
- **Low Input Offset Voltage .... 200µV Max**
- **Low Offset Voltage Drift .... 2µV/°C Max**
- **High Gain .... 400V/mV Min**
- **Outstanding CMR .... 106 dB Min**
- **Industry Standard 8-Pin Dual Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE CERDIP 8-PIN	PLASTIC	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
200	OP271AZ*	–	OP271ARC/883	MIL
200	OP271EZ	–	–	XND
300	OP271FZ	–	–	XND
400	–	OP271GP	–	XND
400	–	OP271GS††	–	XND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

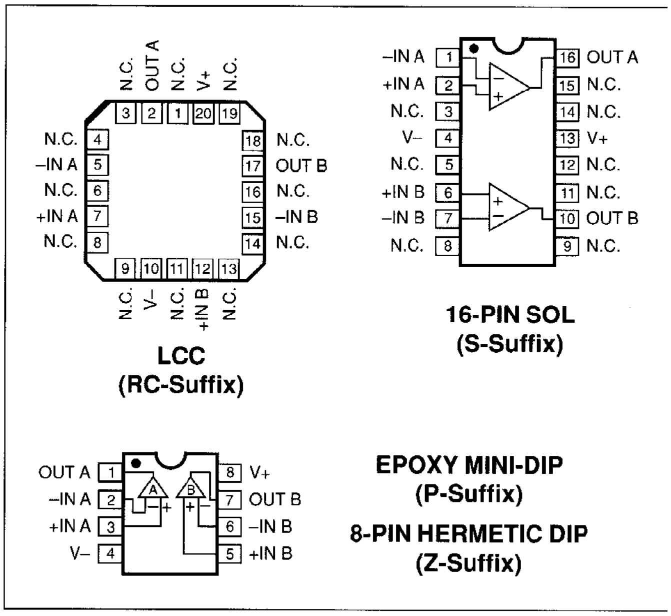
GENERAL DESCRIPTION

The OP-271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5V/µs typical, and fast settling time, 2µs typical to 0.01%. The OP-271 has a gain-bandwidth of 5MHz with a high phase margin of 62°.

Input offset voltage of the OP-271 is under 200µV with input offset voltage drift below 2µV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 20nA limiting errors due to source resistance. The OP-271's outstanding CMR, over 106dB, and low PSRR, under 5.6µV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP-271 exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

Continued

PIN CONNECTIONS



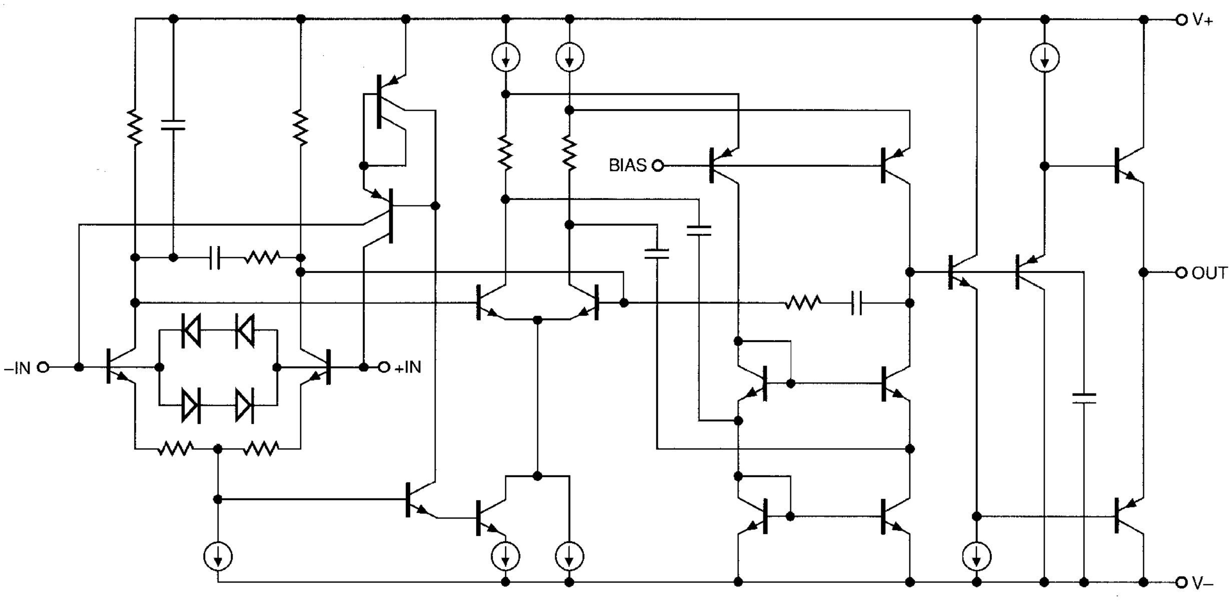
LCC (RC-Suffix)

16-PIN SOL (S-Suffix)

EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (One of the two amplifiers is shown.)



The OP-271 offers outstanding DC and AC matching between channels. This is especially valuable for applications such as multiple gain blocks, high-speed instrumentation and amplifiers, buffers and active filters.

The OP-271 conforms to the industry standard 8-pin dual op amp pinout. It is pin compatible with the TL072, TL082, LF412, and 1458/1558 dual op amps and can be used to significantly improve systems using these devices.

For applications requiring lower voltage noise, see the OP-270. For a quad version of the OP-271, see the OP-471.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±18V
Differential Input Voltage (Note 2) .... ±1.0V
Differential Input Current (Note 2) .... ±25mA
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Continuous
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C
Junction Temperature (T_j) .... –65°C to +150C
Operating Temperature Range
OP-271A .... –55°C to +125°C
OP-271E, OP-271F, OP-271G .... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

			OP-271A/E			OP-271F			OP-271G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	75	200	–	150	300	–	200	400	µV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1	10	–	4	15	–	7	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	4	20	–	6	40	–	12	60	nA
Input Noise Voltage Density	e_n	$f_O = 1kHz$	–	7.6	–	–	7.6	–	–	7.6	–	nV/ Hz
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$	400	650	–	300	500	–	250	400	–	V/mV
		$R_L = 2k\Omega$	300	500	–	200	300	–	175	250	–	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	106	120	–	100	115	–	90	105	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	–	0.6	3.2	–	1.8	5.6	–	2.4	7.0	µV/V
Slew Rate	SR		5.5	8.5	–	5.5	8.5	–	5.5	8.5	–	V/µs
Phase Margin	ϕ_m	$A_V = +1$	–	62	–	–	62	–	–	62	–	deg
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	6.5	–	4.5	6.5	–	4.5	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	$V_O = 20V_{p\text{-}p}$ $f_O = 10Hz$ (Note 2)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	$A_V = +1$, 10V Step to 0.01%	–	2	–	–	2	–	–	2	–	µs

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$ for OP-271A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A MIN	 TYP	 MAX	UNITS
Input Offset Voltage	V_{OS}		—	115	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	7	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$				
		$R_L = 10k\Omega$	300	600	—	V/mV
		$R_L = 2k\Omega$	200	500	—	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	—	1.0	5.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	5.3	7.5	mA

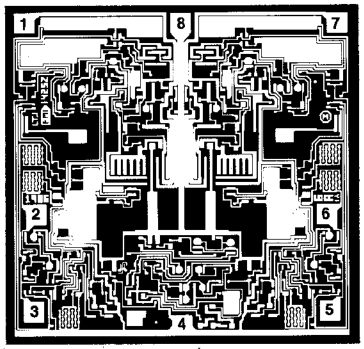
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A/E MIN	 TYP	 MAX	OP-271F MIN	 TYP	 MAX	OP-271G MIN	 TYP	 MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	330	–	215	560	–	300	700	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.4	2	–	1	4	–	2.0	5	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	–	10	70	–	15	80	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$										
		$R_L = 10k\Omega$	300	600	–	200	500	–	150	400	–	V/mV
		$R_L = 2k\Omega$	200	500	–	100	400	–	90	300	–	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	–	0.7	5.6	–	51.8	10	–	2.0	15	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	5.2	7.2	–	5.2	7.2	–	5.2	7.2	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT A
2. −IN A
3. +IN A
4. V−
5. +IN B
6. −IN B
7. OUT B
8. V+

DIE SIZE 0.094 × 0.092 inch, 8,648 sq. mils
(2.39 × 2.34 mm, 5.60 sq. mm)

WAFER TEST LIMITS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

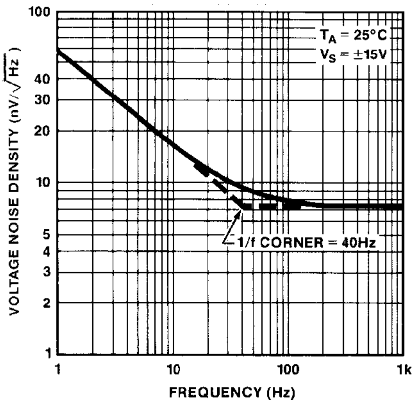
			OP-271GBC	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
Input Offset Voltage	V_{OS}		300	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	15	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	40	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$		
		$R_L = 10k\Omega$	300	V/mV MIN
		$R_L = 2k\Omega$	200	
Input Voltage Range	IVR	(Note 1)	±12	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	5.6	μV/V MAX
Supply Current (All Amplifiers)	I_{SY}	No Load	6.5	mA MAX

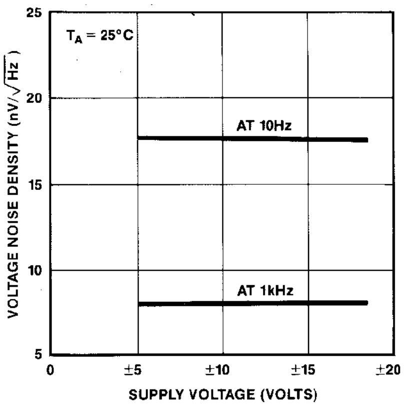
NOTES:

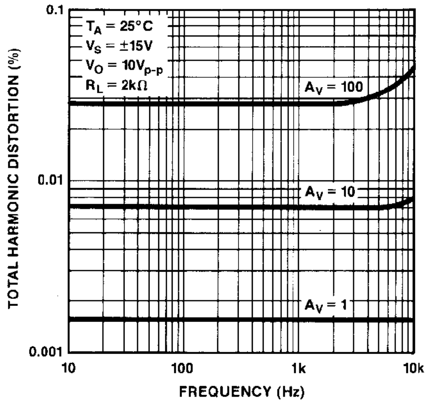
1. Guaranteed by CMR test.

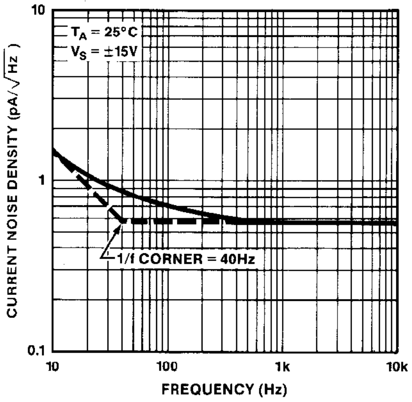
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

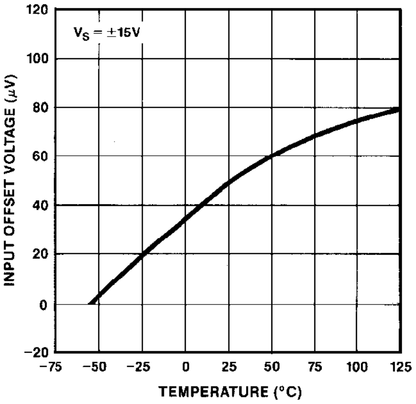
TYPICAL PERFORMANCE CHARACTERISTICS

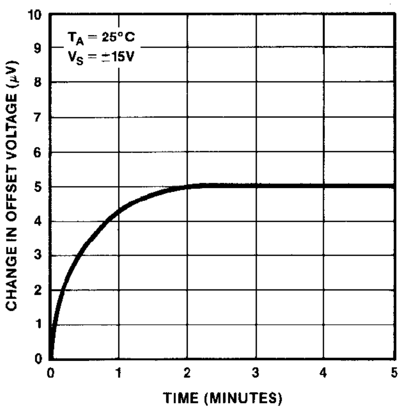

VOLTAGE NOISE DENSITY vs FREQUENCY

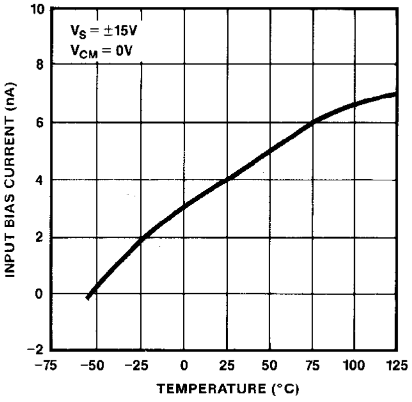

VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE

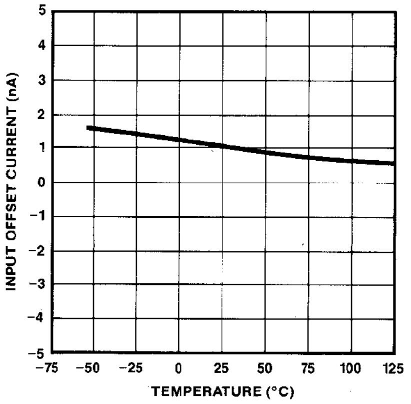

TOTAL HARMONIC DISTORTION vs FREQUENCY

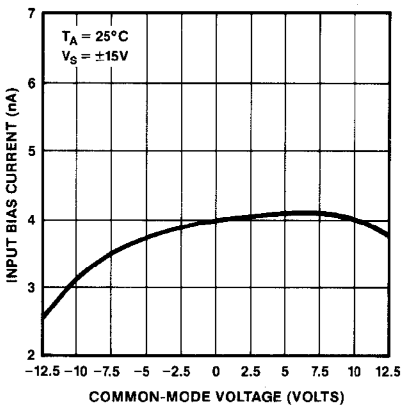

CURRENT NOISE DENSITY vs FREQUENCY


INPUT OFFSET VOLTAGE vs TEMPERATURE


WARM-UP OFFSET VOLTAGE DRIFT

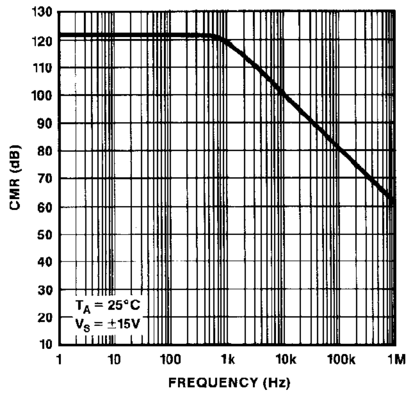

INPUT BIAS CURRENT vs TEMPERATURE


INPUT OFFSET CURRENT vs TEMPERATURE

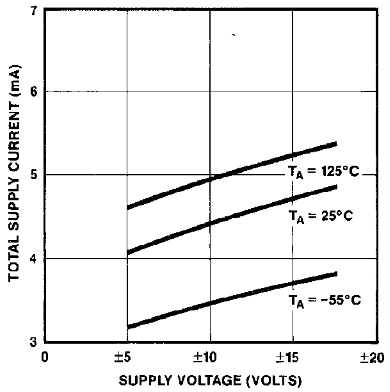

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

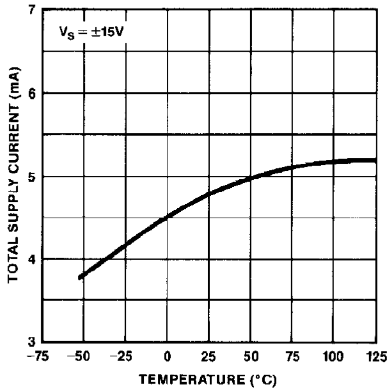
CMR vs FREQUENCY



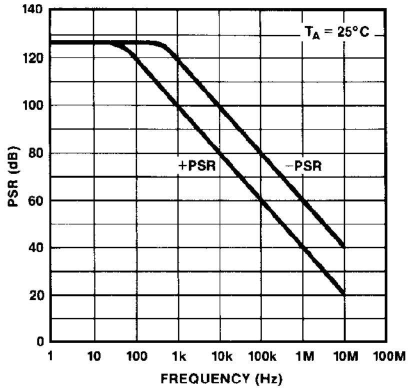
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



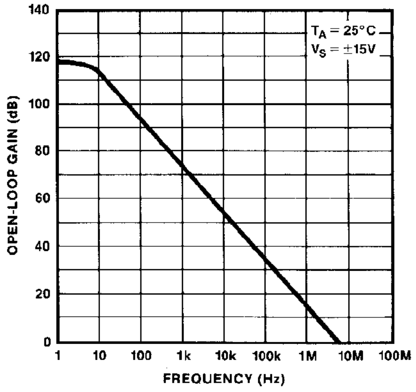
TOTAL SUPPLY CURRENT vs TEMPERATURE



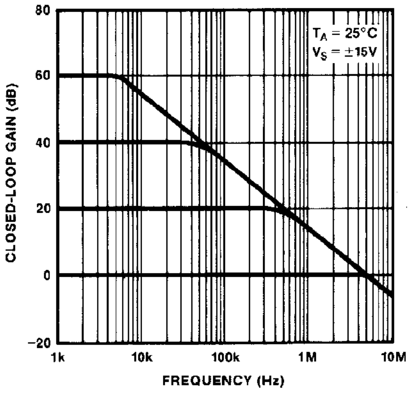
PSR vs FREQUENCY



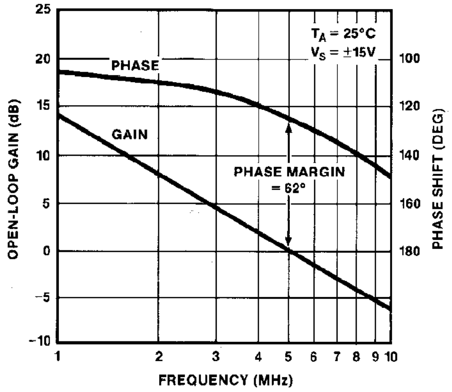
OPEN-LOOP GAIN vs FREQUENCY



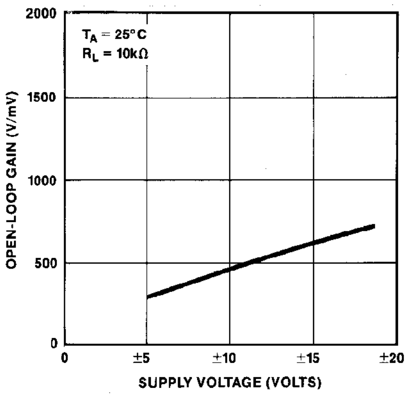
CLOSED-LOOP GAIN vs FREQUENCY



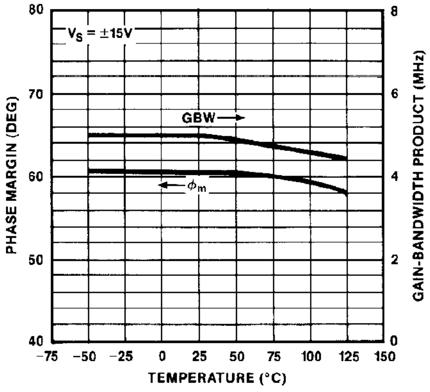
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

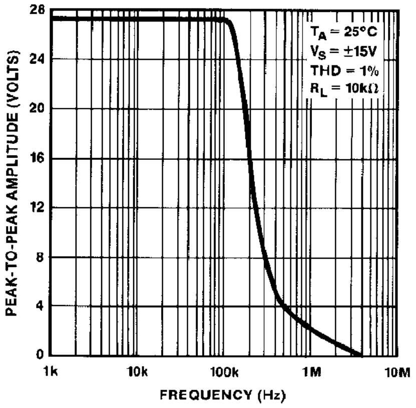


GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

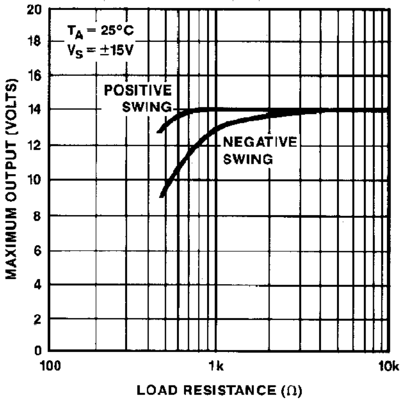


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

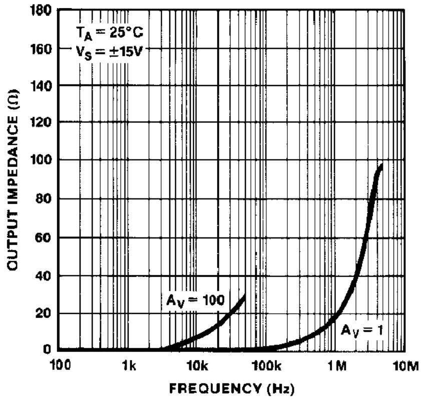
MAXIMUM OUTPUT SWING vs FREQUENCY



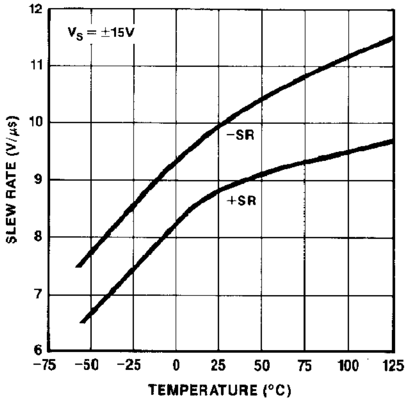
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



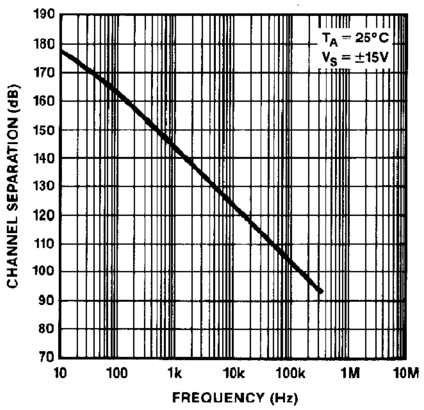
OUTPUT IMPEDANCE vs FREQUENCY



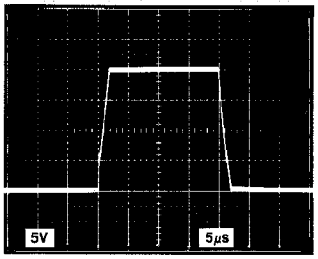
SLEW RATE vs TEMPERATURE



CHANNEL SEPERATION vs FREQUENCY

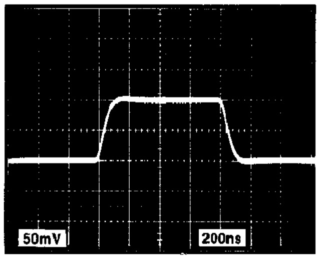


LARGE-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

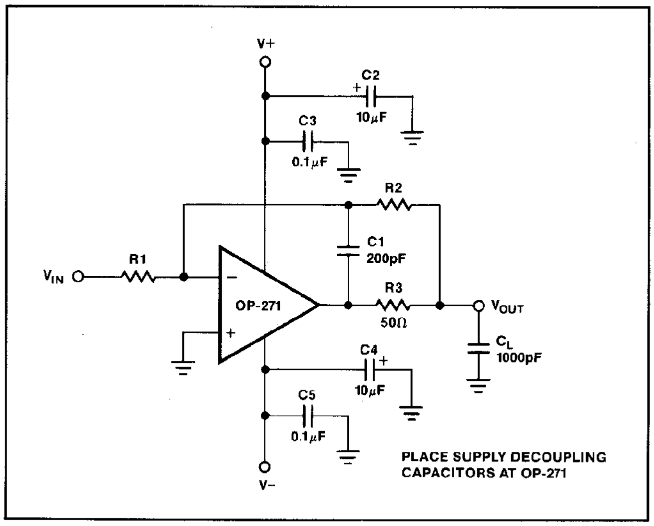
APPLICATIONS INFORMATION

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-271 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-271.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 1. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-271.

FIGURE 1: Driving Large Capacitive Loads

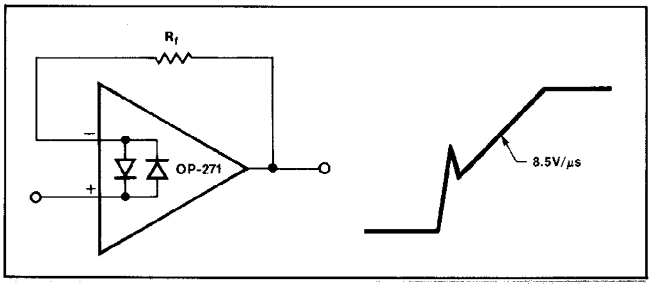


UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 2.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

FIGURE 2: Pulsed Operation



When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (3pF) creates additional phase shift and reduces phase margin. A small capacitor in parallel with R_f helps eliminate this problem.

COMPUTER SIMULATIONS

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP-271 are listed below. Their location will vary slightly between production lots. Typically, they will be within ±15% of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboarded circuit.

POLES	ZEROS
15 Hz	2.5 MHz
1.2 MHz	4 × 23 MHz
2 × 32 MHz	—
8 × 40 MHz	—

APPLICATIONS

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 3 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note that, like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

FIGURE 3: Low Phase Error Amplifier

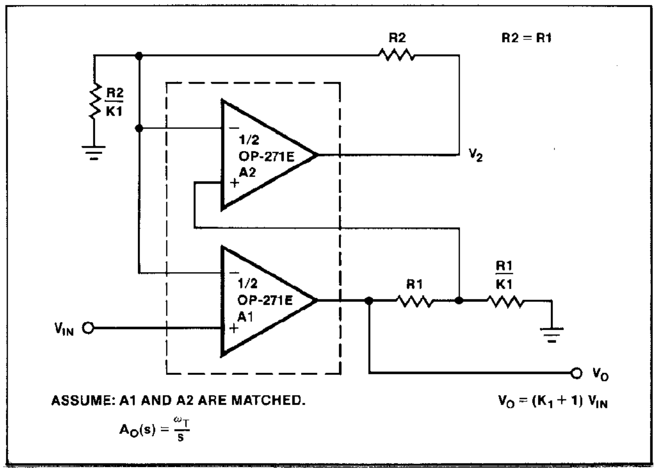


FIGURE 4: Phase Error Comparison

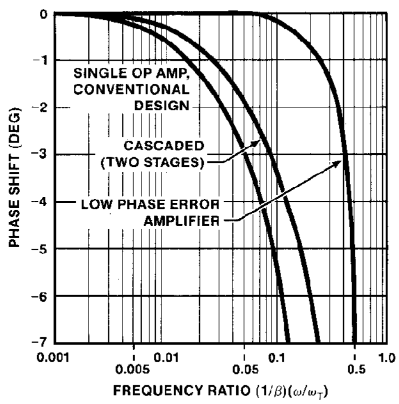


Figure 4 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of $-0.1°$ occurs at 0.002 $\omega/\beta\omega_T$ for the single op amp amplifier, but at 0.11 $\omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual voltage output DAC shown in Figure 5 will settle to 12-bit accuracy from zero to full scale in 2μs typically. The CMOS DAC-8222 utilizes a 12-bit, double-buffered input structure allowing faster digital throughput and minimizing digital feedthrough.

FAST CURRENT PUMP

Maximum output current of the fast current pump shown in Figure 6 is ±11mA. Voltage compliance exceeds ±10V with ±15V supplies. The current pump has an output resistance of over 3MΩ and maintains 12-bit linearity over its entire output range.

FIGURE 6: Fast Current Pump

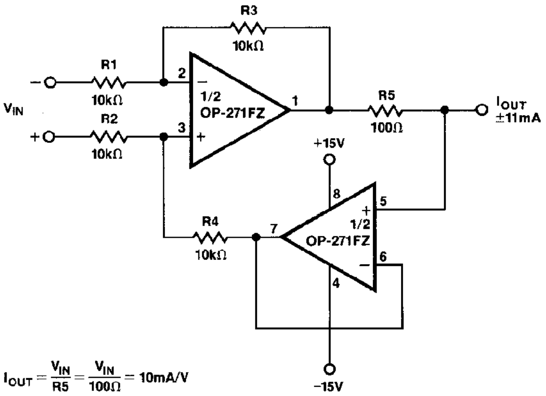


FIGURE 5: Dual 12-Bit Voltage Output DAC