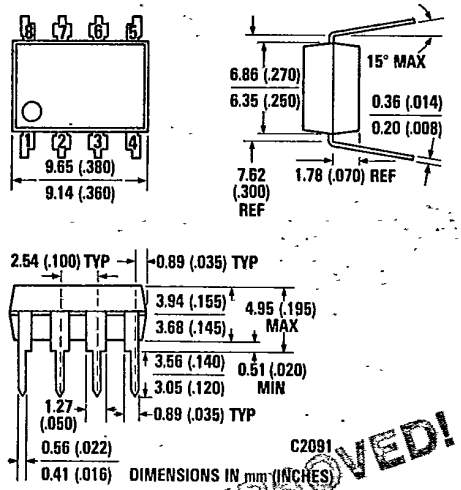
GENERAL INSTRUMENT

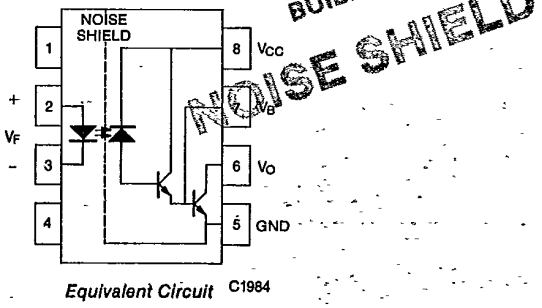
HIGH GAIN SPLIT-DARLINGTON OPTOCOUPLERS

FOR 6N135/6 SEE MCL2501 DATA SHEET — **1.6 mA 6N138**
FOR 6N137 SEE MCL/HCPL-2601 DATA SHEET — **0.5 mA 6N139**

PACKAGE DIMENSIONS



IMPROVED! BUILT-IN NOISE SHIELD



Equivalent Circuit C1984

DESCRIPTION

The 6N138/9 single channel optocouplers contain a 700 nm GaAsP LED emitter which is optically coupled to a high gain detector in a split Darlington configuration, providing extremely high current transfer ratio.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

An internal noise shield provides exceptional common mode rejection of 10 kV/μs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard 220 V.

FEATURES

- Low current — 0.5 mA
- Superior CTR — 2000%
- Superior CMR — 10 kV/μs
- Double working voltage — 480 V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File #E50151)
- Superior insulation; 2500 VAC RMS, 1 min

APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... -55°C to +125°C
Operating temperature ..... 0°C to +70°C
Lead solder temperature ..... 260°C for 10 sec
Average input current ..... 20 mA *(1)*
Peak input current ..... 40 mA
(50% duty cycle, 1 ms P.W.)
Peak transient input current — I_F ..... 1.0 A
(≤ 1 μsec P.W., 300 pps)

Reverse input voltage ..... 5 V
Input power dissipation ..... 35 mW *(2)*
Output current (Pin 6) ..... 60 mA *(3)*
Emitter-base reverse voltage (Pin 5-7) ..... .5 V
Supply and output voltage—V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 ..... -0.5 to 7 V
6N139 ..... -0.5 to 18 V
Output power dissipation ..... 100 mW *(4)*

ELECTRICAL SPECIFICATIONS (T_A = **0°C to +70°C** Unless Otherwise Specified)

PARAMETER	SYMBOL	DEVICE	MIN.	TYP.**	MAX.	UNITS	TEST CONDITIONS
Current transfer ratio (Notes 5, 6)	CTR	6N139	400*	2000		%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V
			500*	2000			I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V
		6N138	300*	2000		%	I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V
Logic low output voltage (Note 6)	V_{OL}	6N139		0.06	0.4	V	I_F = 1.6 mA, I_O = 6.4 mA, V_{CC} = 4.5 V
				0.08	0.4		I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V
				0.09	0.4		I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V
		6N138		0.06	0.4	V	I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V
Logic high output current (Note 6)	I_{OH}	6N139		0.1	100*	μA	I_F = 0 mA, V_O = V_{CC} = 18 V
		6N138		0.001	250*	μA	I_F = 0 mA, V_O = V_{CC} = 7 V
Logic low supply current (Note 6)	I_{CCL}			0.20		mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 5 V
Logic high supply current (Note 6)	I_{CCH}			10.0		nA	I_F = 0 mA, V_O = Open, V_{CC} = 5 V
Input forward voltage	V_F			1.45	1.7*	V	I_F = 1.6 mA, T_A = 25°C
Reverse breakdown voltage	BV_R		5*			V	I_R = 10 μA, T_A = 25°C
Temperature coefficient of forward voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA
Input capacitance	C_O			60		pF	f = 1 MHz, V_F = 0
Isolation leakage (Input-Output) (Note 7)	I_{I-O}				1.0*	μA	45% Relative Humidity, T_A = 25°C V_{I-O} = 3000 V, t_d = 5 sec
Withstand isolation test voltage	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, T_A = 25°C, t = 1 min
Resistance (Input-Output) (Note 7)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc
Capacitance (Input-Output) (Note 7)	C_{I-O}			0.6		pF	f = 1 MHz

SWITCHING SPECIFICATIONS (T_A = 25°C, V_{CC} = 5.0 V)

PARAMETER	SYMBOL	DEVICE	MIN.	TYP.**	MAX.	UNITS	TEST CONDITIONS
Propagation delay time to logic low at output (see Fig. 8; Notes 6, 8)	t_{PHL}	6N139		5.0	25*	μs	I_F = 0.5 mA, R_L = 4.7 kΩ
		6N139		0.2	1*	μs	I_F = 12 mA, R_L = 270 Ω
		6N138		1.0	10*	μs	I_F = 1.6 mA, R_L = 2.2 kΩ
Propagation delay time to logic high at output (see Fig. 8; Notes 6, 8)	t_{PLH}	6N139		1.0	60*	μs	I_F = 0.5 mA, R_L = 4.7 kΩ
		6N139		1.0	7*	μs	I_F = 12 mA, R_L = 270 Ω
		6N138		4.0	35*	μs	I_F = 1.6 mA, R_L = 2.2 kΩ
Common mode transient immunity at logic high level output (see Fig. 9; Note 9)	CM_H			1000	10,000	V/μs	I_F = 0 mA, R_L = 2.2 kΩ $\|V_{cm}\|$ = 10 V_{p-p}
Common mode transient immunity at logic low level output (see Fig. 9; Note 9)	CM_L			-1000	-10,000	V/μs	I_F = 1.6 mA, R_L = 2.2 kΩ $\|V_{cm}\|$ = 10 V_{p-p}

**JEDEC registered data*

***All typicals at T_A = 25°C and V_{CC} = 5 V*

NOTES

1. *Derate linearly above 50°C free-air temperature at a rate of 0.4 mA/°C.*
2. *Derate linearly above 50°C free-air temperature at a rate of 0.7 mW/°C.*
3. *Derate linearly above 25°C free-air temperature at a rate of 0.7 mA/°C.*
4. *Derate linearly above 25°C free-air temperature at a rate of 2.0 mW/°C.*
5. *DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.*
6. *Pin 7 Open.*
7. *Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.*
8. *Use of a resistor between pin 5 and 7 will decrease gain and delay time.*
9. *Common mode transient immunity in Logic High level is the maximum tolerable (positive) dv_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dv_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).*

ELECTRICAL CHARACTERISTIC CURVES (T_A = 25° C Unless Otherwise Specified)

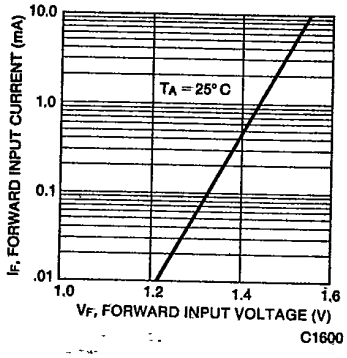


Fig. 1. Input Diode Forward Current vs. Forward Voltage

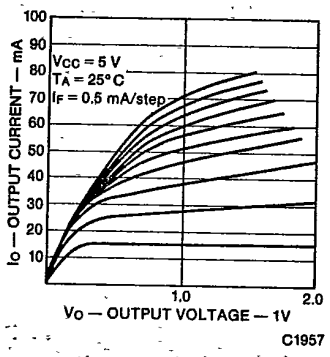


Fig. 2. 6N138/9 DC Transfer Characteristics

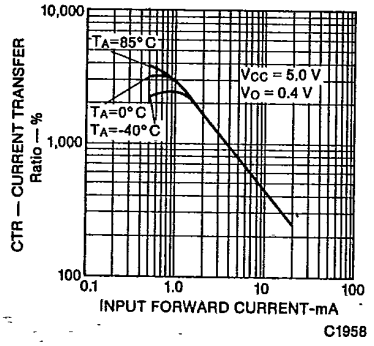


Fig. 3. Current Transfer Ratio vs. Input Forward Current

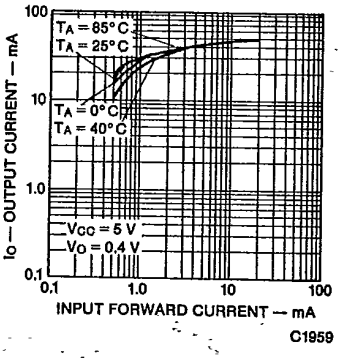


Fig. 4. 6N138 Output Current vs. Input Diode Forward Current

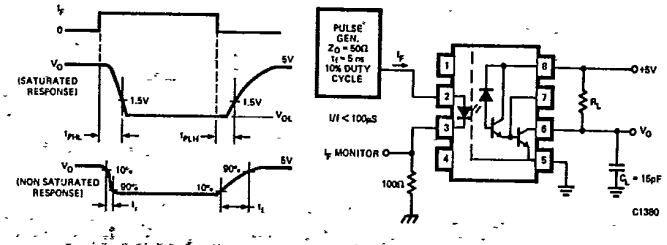


Fig. 5. Switching Test Circuit

ELECTRICAL CHARACTERISTIC CURVES (T_A = 25° C Unless Otherwise Specified)

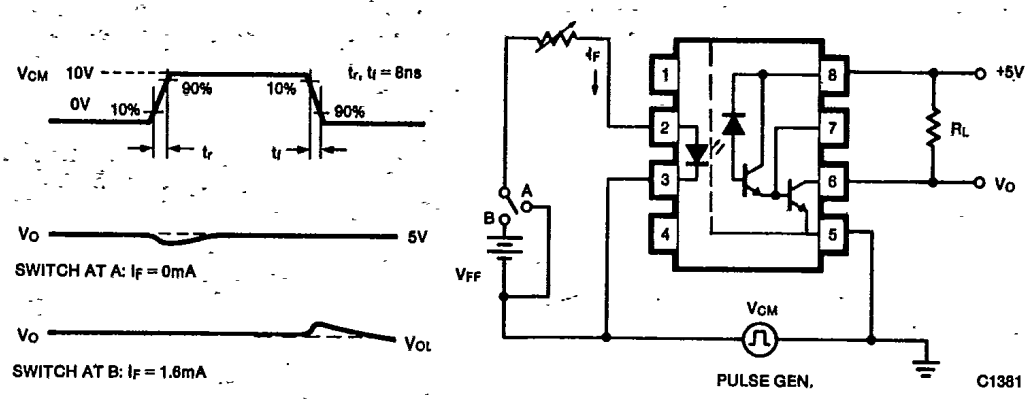
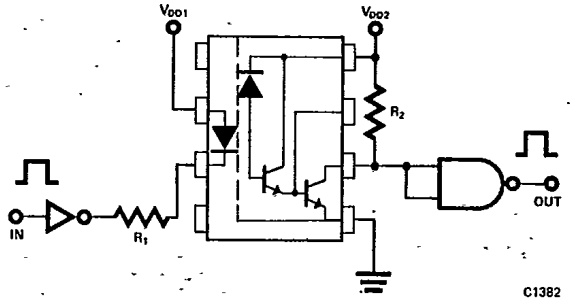
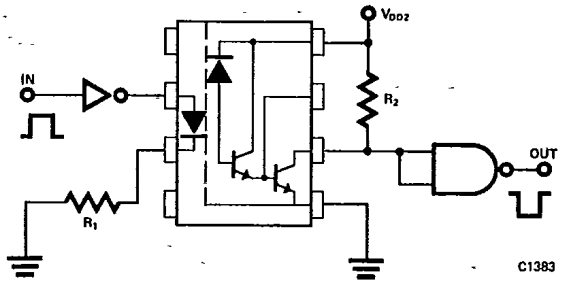


Fig. 6. Test Circuit for Transient Immunity and Typical Waveforms



NON-INVERTING LOGIC INTERFACE



INVERTING LOGIC INTERFACE

$$R_1 \text{ (NON-INVERT)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (INVERT)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} - V_{OLX} (@\ I_L + I_2)}{I_L}$$

WHERE:
- V_{DD1} : INPUT SUPPLY VOLTAGE
- V_{DD2} : OUTPUT SUPPLY VOLTAGE
- V_{DF} : DIODE FORWARD VOLTAGE
- V_{OL1} : LOGIC "0" VOLTAGE OF DRIVER
- V_{OH1} : LOGIC "1" VOLTAGE OF DRIVER
- I_F : DIODE FORWARD CURRENT
- V_{OLX} : SATURATION VOLTAGE OF MCC670
- I_L : LOAD CURRENT THROUGH RESISTOR R_2
- I_2 : INPUT CURRENT OF OUTPUT GATE.

CURRENT LIMITING RESISTOR CALCULATION

INPUT			OUTPUT						
			CMOS @ 5V	CMOS @ 10V	74XX	74LXX	74SXX	74LSXX	74HXX
		R_1 (Ω)	R_2 (Ω)	R_2 (Ω)	R_2 (Ω)	R_2 (Ω)	R_2 (Ω)	R_2 (Ω)	R_2 (Ω)
CMOS @ 5V	NON INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10V	NON INV.	5100							
	INV.	4700							
74XX	NON INV.	2200							
	INV.	180							
74LXX	NON INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

RESISTOR VALUES FOR LOGIC INTERFACE