

DEMO BOARD  
AVAILABLE

## FEATURES

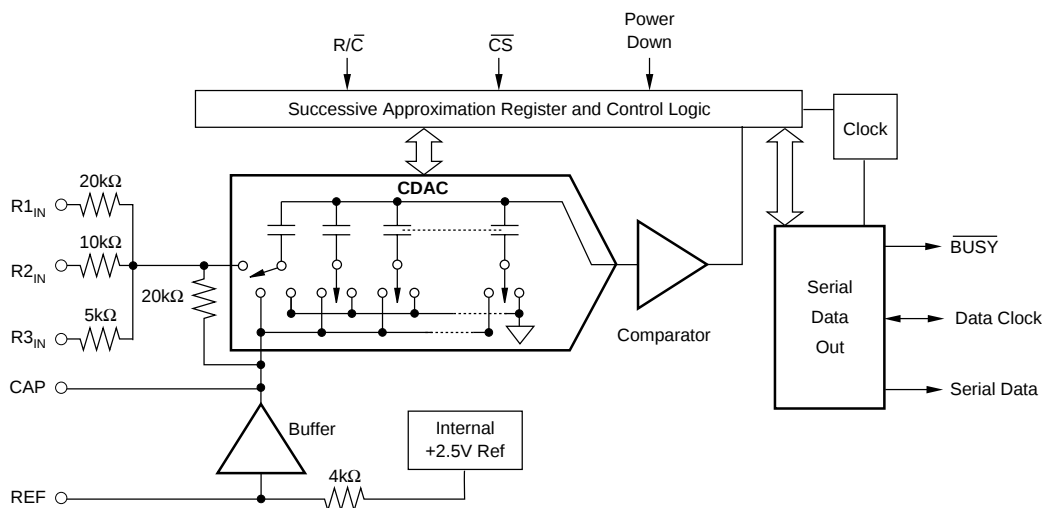
- 100kHz SAMPLING RATE
- 86dB SINAD WITH 20kHz INPUT
- $\pm 2$  LSB INL
- DNL: 16 BITS "No Missing Codes"
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7808
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

## DESCRIPTION

The ADS7809 is a complete 16-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including  $\pm 10\text{V}$  and  $0\text{V}$  to  $5\text{V}$ , while an innovative design operates from a single  $+5\text{V}$  supply, with power dissipation under  $100\text{mW}$ .

The 20-pin ADS7809 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  range.



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## ELECTRICAL

| PARAMETER                                                                           | CONDITIONS                       | ADS7809P, U |      |                                   | ADS7809PB, UB |     |     | UNITS              |
|-------------------------------------------------------------------------------------|----------------------------------|-------------|------|-----------------------------------|---------------|-----|-----|--------------------|
|                                                                                     |                                  | MIN         | TYP  | MAX                               | MIN           | TYP | MAX |                    |
| RESOLUTION                                                                          |                                  |             |      | 16                                |               |     | *   | Bits               |
| ANALOG INPUT                                                                        |                                  |             |      |                                   |               |     |     |                    |
| Voltage Ranges                                                                      |                                  |             |      | ±10, 0V to 5V, etc. (See Table I) |               |     |     |                    |
| Impedance                                                                           |                                  |             |      | See Table I                       |               |     |     |                    |
| Capacitance                                                                         |                                  |             | 35   |                                   |               | *   |     | pF                 |
| THROUGHPUT SPEED                                                                    |                                  |             |      |                                   |               |     |     |                    |
| Complete Cycle                                                                      | Acquire and Convert              |             |      | 10                                |               |     | *   | μs                 |
| Throughput Rate                                                                     |                                  | 100         |      |                                   | *             |     |     | kHz                |
| DC ACCURACY                                                                         |                                  |             |      |                                   |               |     |     |                    |
| Integral Linearity Error                                                            |                                  |             |      | ±3                                |               |     | ±2  | LSB <sup>(1)</sup> |
| Differential Linearity Error                                                        |                                  |             |      | +3, -2                            |               |     | ±1  | LSB                |
| No Missing Codes                                                                    |                                  | 15          |      |                                   | 16            |     |     | Bits               |
| Transition Noise <sup>(2)</sup>                                                     |                                  |             | 1.3  |                                   |               | *   |     | LSB                |
| Full Scale Error <sup>(3,4)</sup>                                                   |                                  |             |      | ±0.5                              |               | *   | *   | %                  |
| Full Scale Error Drift                                                              |                                  |             | ±7   |                                   |               | *   | *   | ppm/°C             |
| Full Scale Error <sup>(3,4)</sup>                                                   | Ext. 2.5000V Ref                 |             |      | ±0.5                              |               | *   | *   | %                  |
| Full Scale Error Drift                                                              | Ext. 2.5000V Ref                 |             | ±2   |                                   |               | *   | *   | ppm/°C             |
| Bipolar Zero Error <sup>(3)</sup>                                                   | Bipolar Ranges                   |             |      | ±10                               |               | *   | *   | mV                 |
| Bipolar Zero Error Drift                                                            | Bipolar Ranges                   |             | ±2   |                                   |               | *   | *   | ppm/°C             |
| Unipolar Zero Error <sup>(3)</sup>                                                  | 0V tp 10V Ranges                 |             |      | ±5                                |               | *   | *   | mV                 |
| Unipolar Zero Error <sup>(3)</sup>                                                  | 0V to 4V, 0V to 5V Ranges        |             |      | ±3                                |               | *   | *   | mV                 |
| Unipolar Zero Error Drift                                                           | Unipolar Ranges                  |             | ±2   |                                   |               | *   | *   | ppm/°C             |
| Recovery to Rated Accuracy<br>after Power Down                                      | 1μF Capacitor to CAP             |             | 1    |                                   |               | *   | *   | ms                 |
| Power Supply Sensitivity<br>(V <sub>DIG</sub> = V <sub>ANA</sub> = V <sub>D</sub> ) | +4.75V < V <sub>D</sub> < +5.25V |             |      | ±8                                |               |     | *   | LSB                |
| AC ACCURACY                                                                         |                                  |             |      |                                   |               |     |     |                    |
| Spurious-Free Dynamic Range                                                         | f <sub>IN</sub> = 20kHz          | 90          | 100  |                                   | 96            | *   |     | dB <sup>(5)</sup>  |
| Total Harmonic Distortion                                                           | f <sub>IN</sub> = 20kHz          |             | -100 | -90                               |               | *   | -94 | dB                 |
| Signal-to-(Noise+Distortion)                                                        | f <sub>IN</sub> = 20kHz          | 83          | 88   |                                   | 86            | *   |     | dB                 |
|                                                                                     | -60dB Input                      |             | 30   |                                   |               | 32  |     | dB                 |
| Signal-to-Noise                                                                     | f <sub>IN</sub> = 20kHz          | 83          | 88   |                                   | 86            | *   |     | dB                 |
| Full-Power Bandwidth <sup>(6)</sup>                                                 |                                  |             | 250  |                                   |               | *   |     | kHz                |
| SAMPLING DYNAMICS                                                                   |                                  |             |      |                                   |               |     |     |                    |
| Aperture Delay                                                                      |                                  |             | 40   |                                   |               | *   |     | ns                 |
| Transient Response                                                                  | FS Step                          |             |      | 2                                 |               | *   | *   | μs                 |
| Overvoltage Recovery <sup>(7)</sup>                                                 |                                  |             | 150  |                                   |               | *   |     | ns                 |
| REFERENCE                                                                           |                                  |             |      |                                   |               |     |     |                    |
| Internal Reference Voltage                                                          | No Load                          | 2.48        | 2.5  | 2.52                              | *             | *   | *   | V                  |
| Internal Reference Source Current<br>(Must use external buffer)                     |                                  |             | 1    |                                   |               | *   |     | μA                 |
| External Reference Voltage Range<br>For Specified Linearity                         |                                  | 2.3         | 2.5  | 2.7                               | *             | *   | *   | V                  |
| External Reference Current Drain                                                    | Ext. 2.5000V Ref                 |             |      | 100                               |               |     | *   | μA                 |
| DIGITAL INPUTS                                                                      |                                  |             |      |                                   |               |     |     |                    |
| Logic Levels                                                                        |                                  |             |      |                                   |               |     |     |                    |
| V <sub>IL</sub>                                                                     |                                  | -0.3        |      | +0.8                              | *             |     | *   | V                  |
| V <sub>IH</sub>                                                                     |                                  | +2.0        |      | V <sub>D</sub> +0.3V              | *             |     | *   | V                  |
| I <sub>IL</sub>                                                                     | V <sub>IL</sub> = 0V             |             |      | ±10                               |               |     | *   | μA                 |
| I <sub>IH</sub>                                                                     | V <sub>IH</sub> = 5V             |             |      | ±10                               |               |     | *   | μA                 |

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## ELECTRICAL

| PARAMETER                                                                                                                                                           | CONDITIONS                                                                                                                             | ADS7809P, U       |                                 |                               | ADS7809PB, UB      |                  |                 | UNITS                          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|-------------------|---------------------------------|-------------------------------|--------------------|------------------|-----------------|--------------------------------|
|                                                                                                                                                                     |                                                                                                                                        | MIN               | TYP                             | MAX                           | MIN                | TYP              | MAX             |                                |
| DIGITAL OUTPUTS<br>Data Format<br>Data Co<br>Pipeline Delay<br>Data Clock<br>Internal<br>(Output Only When Transmitting Data)<br>External<br>(Can Run Continually)  | EXT/ $\overline{\text{INT}}$ LOW                                                                                                       |                   |                                 |                               |                    |                  |                 | MHz                            |
| V <sub>OL</sub><br>V <sub>OH</sub><br>Leakage Current                                                                                                               | EXT/ $\overline{\text{INT}}$ HIGH                                                                                                      | 0.1               |                                 | 10                            | *                  | *                | *               | MHz                            |
| Output Capacitance                                                                                                                                                  | I <sub>SINK</sub> = 1.6mA<br>I <sub>SOURCE</sub> = 500μA<br>High-Z State,<br>V <sub>OUT</sub> = 0V to V <sub>DIG</sub><br>High-Z State | +4                |                                 | +0.4                          | *                  | *                | *               | V<br>V<br>μA                   |
|                                                                                                                                                                     |                                                                                                                                        |                   |                                 | ±5                            |                    |                  | *               | pF                             |
|                                                                                                                                                                     |                                                                                                                                        |                   |                                 | 15                            |                    |                  | *               |                                |
| POWER SUPPLIES<br>Specified Performance<br>V <sub>DIG</sub><br>V <sub>ANA</sub><br>I <sub>DIG</sub><br>I <sub>ANA</sub><br>Power Dissipation: PWRD LOW<br>PWRD HIGH | Must be ≤ V <sub>ANA</sub>                                                                                                             | +4.75<br>+4.75    | +5<br>+5<br>0.3<br>16<br><br>50 | +5.25<br>+5.25<br><br><br>100 | *<br>*<br><br><br> | *<br>*<br>*<br>* | *<br>*<br><br>* | V<br>V<br>mA<br>mA<br>mW<br>μW |
| TEMPERATURE RANGE<br>Specified Performance<br>Derated Performance<br>Storage<br>Thermal Resistance ( $\theta_{JA}$ )<br>Plastic DIP<br>SOIC                         |                                                                                                                                        | -40<br>-55<br>-65 |                                 | +85<br>+125<br>+150           | *<br>*<br>*        |                  | *<br>*<br>*     | °C<br>°C<br>°C<br>°C/W<br>°C/W |

NOTES: (1) LSB means Least Significant Bit. For the  $\pm 10\text{V}$  input range, one LSB is  $305\mu\text{V}$ . (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of  $- \text{Full Scale}$  or  $+ \text{Full Scale}$  untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale  $\pm 10\text{V}$  input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB. (7) Recovers to specified performance after  $2 \times \text{FS}$  input overvoltage.

|                                               |                                                                   |
|-----------------------------------------------|-------------------------------------------------------------------|
| Analog Inputs: R1 <sub>IN</sub> .....         | ±25V                                                              |
| R2 <sub>IN</sub> .....                        | ±25V                                                              |
| R3 <sub>IN</sub> .....                        | ±25V                                                              |
| CAP .....                                     | V <sub>ANA</sub> +0.3V to AGND2 -0.3V                             |
| REF .....                                     | Indefinite Short to AGND2,<br>Momentary Short to V <sub>ANA</sub> |
| Ground Voltage Differences: DGND, AGND2 ..... | ±0.3V                                                             |
| V <sub>ANA</sub> .....                        | 7V                                                                |
| V <sub>DIG</sub> to V <sub>ANA</sub> .....    | +0.3                                                              |
| V <sub>DIG</sub> .....                        | 7V                                                                |
| Digital Inputs .....                          | -0.3V to V <sub>DIG</sub> +0.3V                                   |
| Maximum Junction Temperature .....            | +165°C                                                            |
| Internal Power Dissipation .....              | 700mW                                                             |
| Lead Temperature (soldering, 10s) .....       | +300°C                                                            |



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

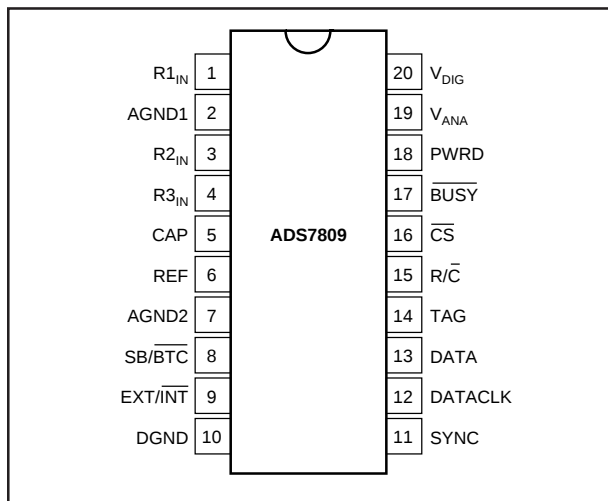
| PRODUCT   | MAXIMUM<br>LINEARITY<br>ERROR (LSB) | GUARANTEED<br>NO MISSING<br>CODE LEVEL<br>(LSB) | MINIMUM<br>SIGNAL-TO-<br>(NOISE + DISTORTION)<br>RATIO (dB) | SPECIFICATION<br>TEMPERATURE<br>RANGE (°C) | PACKAGE            | PACKAGE<br>DRAWING<br>NUMBER <sup>(1)</sup> |
|-----------|-------------------------------------|-------------------------------------------------|-------------------------------------------------------------|--------------------------------------------|--------------------|---------------------------------------------|
| ADS7809P  | ±3                                  | 15                                              | 83                                                          | −40 to +85                                 | 20-Pin Plastic DIP | 222                                         |
| ADS7809PB | ±2                                  | 16                                              | 86                                                          | −40 to +85                                 | 20-Pin Plastic DIP | 222                                         |
| ADS7809U  | ±3                                  | 15                                              | 83                                                          | −40 to +85                                 | 20-Lead SOIC       | 221                                         |
| ADS7809UB | ±2                                  | 16                                              | 86                                                          | −40 to +85                                 | 20-Lead SOIC       | 221                                         |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## PIN ASSIGNMENTS

| PIN # | NAME             | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | R1 <sub>IN</sub> | Analog Input. See Table I and Figure 4 for input range connections.                                                                                                                                                                                                                                                                                                                                                                                              |
| 2     | AGND1            | Analog Ground. Used internally as ground reference point. Minimal current flow.                                                                                                                                                                                                                                                                                                                                                                                  |
| 3     | R2 <sub>IN</sub> | Analog Input. See Table I and Figure 4 for input range connections.                                                                                                                                                                                                                                                                                                                                                                                              |
| 4     | R3 <sub>IN</sub> | Analog Input. See Table I and Figure 4 for input range connections.                                                                                                                                                                                                                                                                                                                                                                                              |
| 5     | CAP              | Reference Buffer Capacitor. 2.2μF Tantalum to ground.                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6     | REF              | Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF Tantalum capacitor.                                                                                                                                                                                                                                                                                       |
| 7     | AGND2            | Analog Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8     | SB/BTC           | Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.                                                                                                                                                                                                                                                                 |
| 9     | EXT/INT          | Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.                                                                                                                                                                               |
| 10    | DGND             | Digital Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11    | SYNC             | Sync Output. If EXT/INT is HIGH, either a rising edge on R/C with CS LOW or a falling edge on CS with R/C HIGH will output a pulse on SYNC synchronized to the external DATACLK.                                                                                                                                                                                                                                                                                 |
| 12    | DATACLK          | Either an input or an output depending on the EXT/INT level. Output data will be synchronized to this clock. If EXT/INT is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.                                                                                                                                                                                                                                  |
| 13    | DATA             | Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16 bits of data, the ADS7809 will output the level input on TAG as long as CS is LOW and R/C is HIGH (see Figure 3.) If EXT/INT is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started. |
| 14    | TAG              | Tag Input for use in external clock mode. If EXT/INT is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as CS is LOW and R/C is HIGH. See Figure 3.                                                                                                                                                                                                                                                             |
| 15    | R/C              | Read/Convert Input. With CS LOW, a falling edge on R/C puts the internal sample/hold into the hold state and starts a conversion. When EXT/INT is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is HIGH, a rising edge on R/C with CS LOW, or a falling edge on CS with R/C HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.                        |
| 16    | CS               | Chip Select. Internally OR'ed with R/C.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 17    | BUSY             | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. CS or R/C must be HIGH when BUSY rises, or another conversion will start without time for signal acquisition.                                                                                                                                                                                         |
| 18    | PWRD             | Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.                                                                                                                                                                                                                                                                           |
| 19    | V <sub>ANA</sub> | Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF Tantalum capacitors.                                                                                                                                                                                                                                                                                                                          |
| 20    | V <sub>DIG</sub> | Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V <sub>ANA</sub> .                                                                                                                                                                                                                                                                                                                                                                    |

## PIN CONFIGURATION



| ANALOG INPUT RANGE | CONNECT R1 <sub>IN</sub> VIA 200Ω TO | CONNECT R2 <sub>IN</sub> VIA 100Ω TO | CONNECT R3 <sub>IN</sub> TO | IMPEDANCE |
|--------------------|--------------------------------------|--------------------------------------|-----------------------------|-----------|
| ±10V               | V <sub>IN</sub>                      | AGND                                 | CAP                         | 22.9kΩ    |
| ±5V                | AGND                                 | V <sub>IN</sub>                      | CAP                         | 13.3kΩ    |
| ±3.33V             | V <sub>IN</sub>                      | V <sub>IN</sub>                      | CAP                         | 10.7kΩ    |
| 0V to 10V          | AGND                                 | V <sub>IN</sub>                      | AGND                        | 13.3kΩ    |
| 0V to 5V           | AGND                                 | AGND                                 | V <sub>IN</sub>             | 10.0kΩ    |
| 0V to 4V           | V <sub>IN</sub>                      | AGND                                 | V <sub>IN</sub>             | 10.7kΩ    |

TABLE I. Input Range Connections. See Figure 4 for complete information.

| SYMBOL      | DESCRIPTION                                                         | MIN | TYP | MAX          | UNITS         |
|-------------|---------------------------------------------------------------------|-----|-----|--------------|---------------|
| $t_1$       | Convert Pulse Width                                                 | 40  |     | 6000         | ns            |
| $t_2$       | $\overline{\text{BUSY}}$ Delay                                      |     |     | 65           | ns            |
| $t_3$       | $\overline{\text{BUSY}}$ LOW                                        |     |     | 8            | $\mu\text{s}$ |
| $t_4$       | $\overline{\text{BUSY}}$ Delay after End of Conversion              |     | 220 |              | ns            |
| $t_5$       | Aperture Delay                                                      |     | 40  |              | ns            |
| $t_6$       | Conversion Time                                                     |     | 7.6 | 8            | $\mu\text{s}$ |
| $t_7$       | Acquisition Time                                                    |     |     | 2            | $\mu\text{s}$ |
| $t_6 + t_7$ | Throughput Time                                                     |     | 9   | 10           | $\mu\text{s}$ |
| $t_8$       | $\text{R}/\overline{\text{C}}$ LOW to DATACLK Delay                 |     | 450 |              | ns            |
| $t_9$       | DATACLK Period                                                      |     | 440 |              | ns            |
| $t_{10}$    | Data Valid to DATACLK HIGH Delay                                    | 20  | 75  |              | ns            |
| $t_{11}$    | Data Valid after DATACLK LOW Delay                                  | 100 | 125 |              | ns            |
| $t_{12}$    | External DATACLK                                                    | 100 |     |              | ns            |
| $t_{13}$    | External DATACLK HIGH                                               | 20  |     |              | ns            |
| $t_{14}$    | External DATACLK LOW                                                | 30  |     |              | ns            |
| $t_{15}$    | DATACLK HIGH Setup Time                                             | 20  |     | $t_{12} + 5$ | ns            |
| $t_{16}$    | $\text{R}/\overline{\text{C}}$ to $\overline{\text{CS}}$ Setup Time | 10  |     |              | ns            |
| $t_{17}$    | SYNC Delay After DATACLK HIGH                                       | 15  |     | 35           | ns            |
| $t_{18}$    | Data Valid Delay                                                    | 25  |     | 55           | ns            |
| $t_{19}$    | $\overline{\text{CS}}$ to Rising Edge Delay                         | 25  |     |              | ns            |
| $t_{20}$    | Data Available after $\overline{\text{CS}}$ LOW                     | 6   |     |              | $\mu\text{s}$ |

TABLE II. Conversion and Data Timing.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

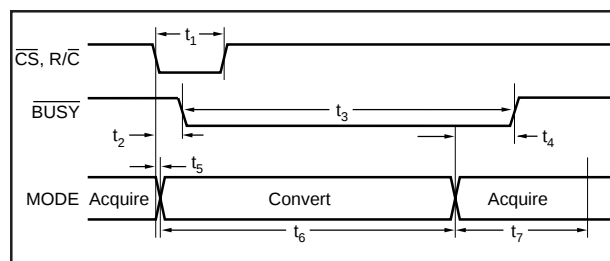


FIGURE 1. Basic Conversion Timing.

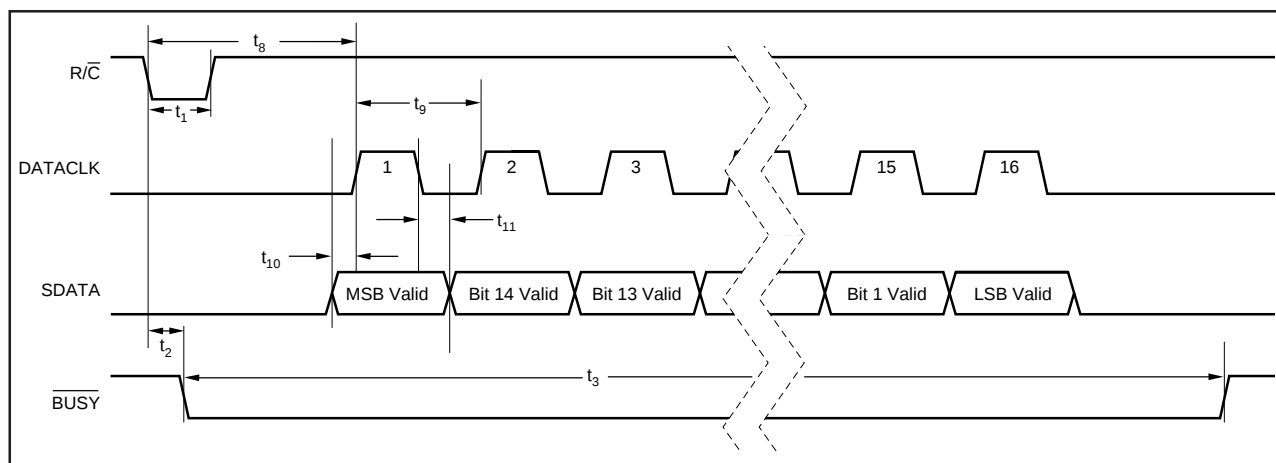


FIGURE 2. Serial Data Timing Using Internal Clock. ( $\overline{\text{CS}}$ ,  $\text{EXT}/\overline{\text{INT}}$  and  $\text{TAG}$  Tied LOW.)

| SPECIFIC FUNCTION                                        | $\overline{\text{CS}}$ | $\text{R}/\overline{\text{C}}$ | $\overline{\text{BUSY}}$ | $\overline{\text{EXT}}/\overline{\text{INT}}$ | DATACLK | PWRD | SB/BTC | OPERATION                                                                                                                                              |
|----------------------------------------------------------|------------------------|--------------------------------|--------------------------|-----------------------------------------------|---------|------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| Initiate Conversion and Output Data Using Internal Clock | 1>0                    | 0                              | 1                        | 0                                             | Output  | 0    | x      | Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.                            |
|                                                          | 0                      | 1>0                            | 1                        | 0                                             | Output  | 0    | x      | Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.                            |
| Initiate Conversion and Output Data Using External Clock | 1>0                    | 0                              | 1                        | 1                                             | Input   | 0    | x      | Initiates conversion "n".                                                                                                                              |
|                                                          | 0                      | 1>0                            | 1                        | 1                                             | Input   | 0    | x      | Initiates conversion "n".                                                                                                                              |
|                                                          | 1>0                    | 1                              | 1                        | 1                                             | Input   | x    | x      | Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.                                             |
|                                                          | 1>0                    | 1                              | 0                        | 1                                             | Input   | 0    | x      | Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. <sup>(1)</sup> Conversion "n" in process. |
|                                                          | 0                      | 0>1                            | 0                        | 1                                             | Input   | 0    | x      | Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. <sup>(1)</sup> Conversion "n" in process. |
| Incorrect Conversions                                    | 0                      | 0                              | 0>1                      | x                                             | x       | 0    | x      | $\overline{\text{CS}}$ or $\text{R}/\overline{\text{C}}$ must be HIGH or a new conversion will be initiated without time for acquisition.              |
| Power Down                                               | x                      | x                              | x                        | x                                             | x       | 0    | x      | Analog circuitry powered. Conversion can proceed.                                                                                                      |
|                                                          | x                      | x                              | x                        | x                                             | x       | 1    | x      | Analog circuitry disabled. Data from previous conversion maintained in output registers.                                                               |
| Selecting Output Format                                  | x                      | x                              | x                        | x                                             | x       | x    | 0      | Serial data is output in Binary Two's Complement format.                                                                                               |
|                                                          | x                      | x                              | x                        | x                                             | x       | x    | 1      | Serial data is output in Straight Binary format.                                                                                                       |

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

TABLE III. Control Truth Table.

| DESCRIPTION                 | ANALOG INPUT |           |           |           |           |           | DIGITAL OUTPUT                       |          |                               |          |
|-----------------------------|--------------|-----------|-----------|-----------|-----------|-----------|--------------------------------------|----------|-------------------------------|----------|
|                             |              |           |           |           |           |           | BINARY TWO'S COMPLEMENT (SB/BTC LOW) |          | STRAIGHT BINARY (SB/BTC HIGH) |          |
|                             |              |           |           |           |           |           | BINARY CODE                          | HEX CODE | BINARY CODE                   | HEX CODE |
| Full-Scale Range            | ±10          | ±5        | ±3.33V    | 0V to 10V | 0V to 5V  | 0V to 4V  |                                      |          |                               |          |
| Least Significant Bit (LSB) | 305μV        | 153μV     | 102μV     | 153μV     | 76μV      | 61μV      |                                      |          |                               |          |
| +Full Scale (FS – 1LSB)     | 9.999695V    | 4.999847V | 3.333231V | 9.999847V | 4.999924V | 3.999939V | 0111 1111 1111 1111                  | 7FFF     | 1111 1111 1111 1111           | FFFF     |
| Midscale                    | 0V           | 0V        | 0V        | 5V        | 2.5V      | 2V        | 0000 0000 0000 0000                  | 0000     | 1000 0000 0000 0000           | 8000     |
| One LSB Below Midscale      | -305μV       | -153μV    | -102μV    | 4.999847V | 2.499924V | 1.999939V | 1111 1111 1111 1111                  | FFFF     | 0111 1111 1111 1111           | 7FFF     |
| -Full Scale                 | -10V         | -5V       | -3.33333V | 0V        | 0V        | 0V        | 1000 0000 0000 0000                  | 8000     | 0000 0000 0000 0000           | 0000     |

TABLE IV. Output Codes and Ideal Input Voltages.

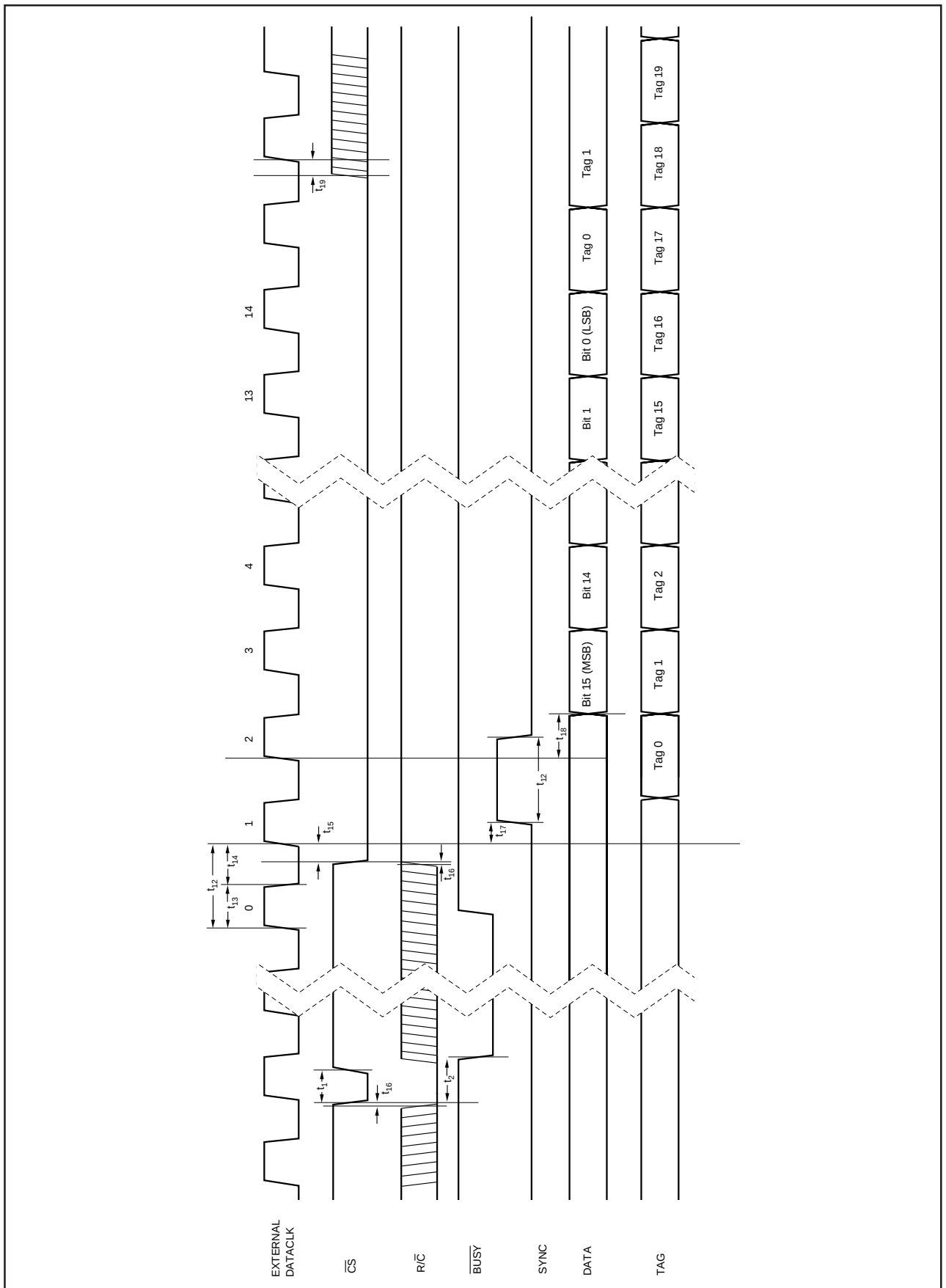


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH.) Read After Conversion.

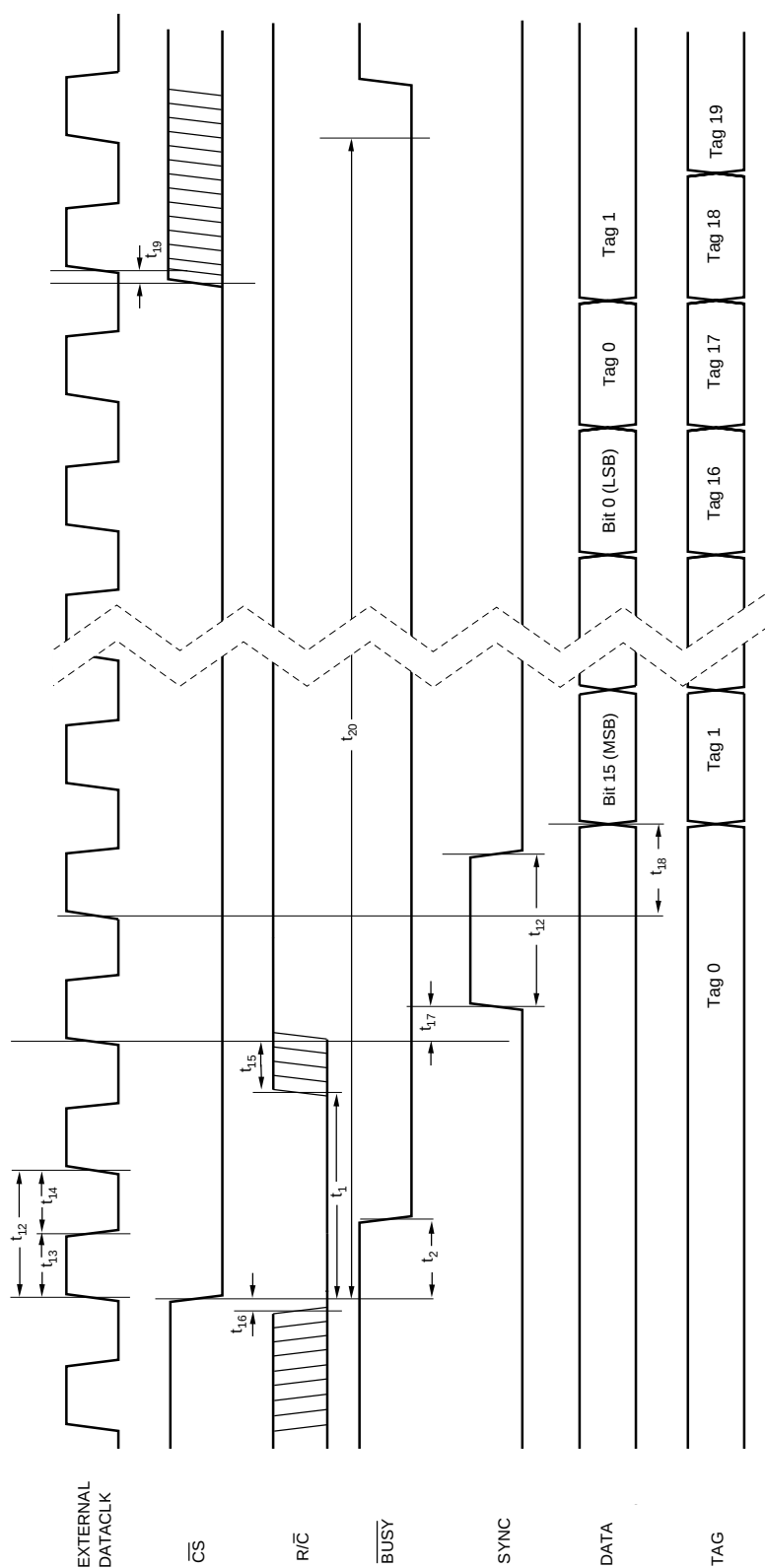


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH.) Read During Conversion (Previous Conversion Results).

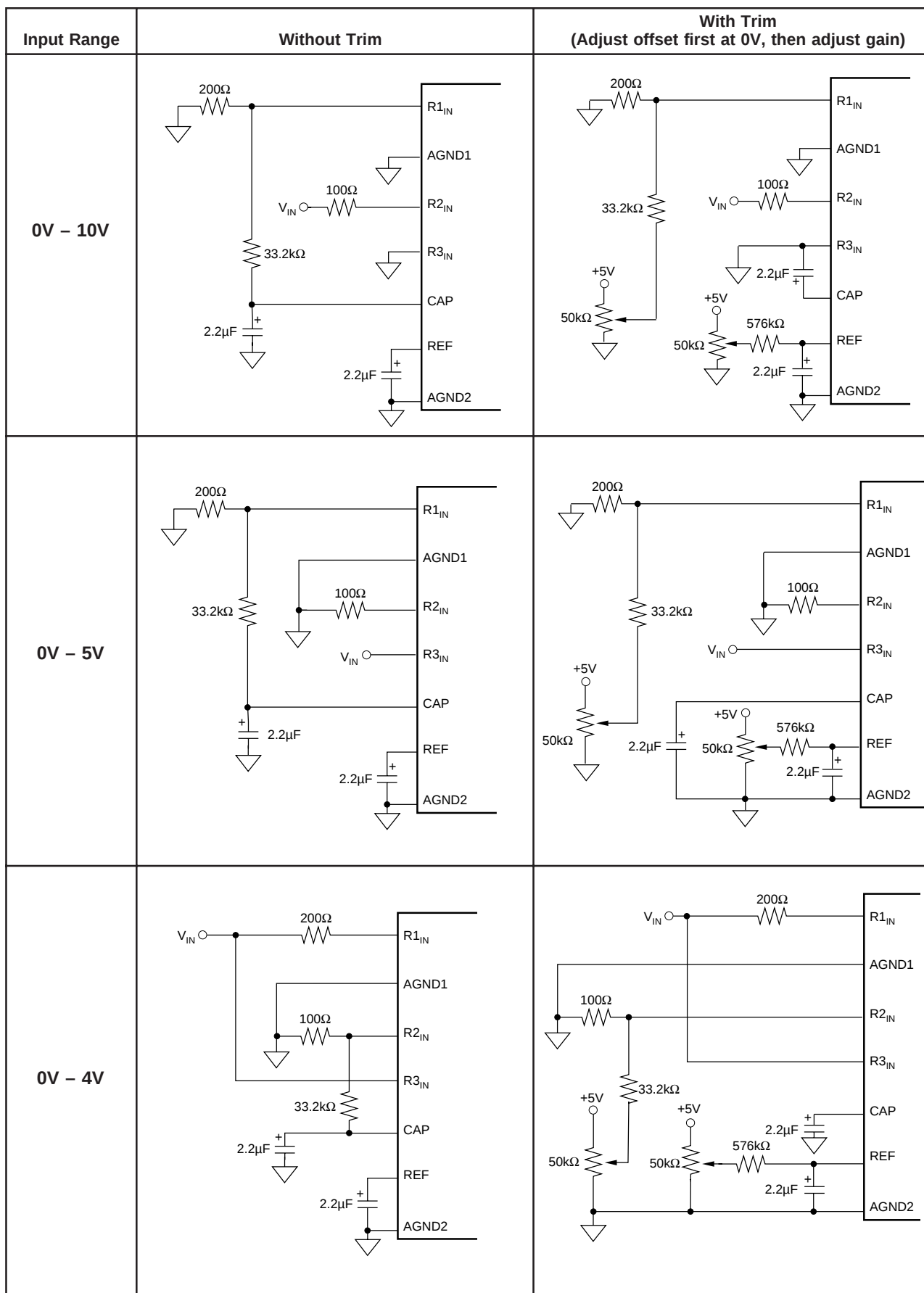


FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

| Input Range | Without Trim | With Trim<br>(Adjust offset first at 0V, then adjust gain) |
|-------------|--------------|------------------------------------------------------------|
| $\pm 10V$   |              |                                                            |
| $\pm 5V$    |              |                                                            |
| $\pm 3.33V$ |              |                                                            |

FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.