BURR-BROWN®

ADS902

SpeedPLUS™ 10-Bit, 30MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SNR: 57dB
- EXTERNAL REFERENCE
- LOW POWER: 140mW
- ADJUSTABLE FULL SCALE RANGE
- POWER DOWN
- 28-PIN SSOP PACKAGE

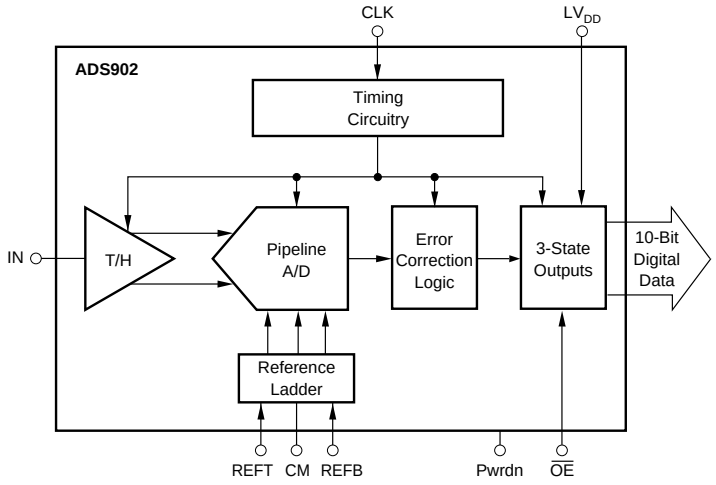
APPLICATIONS

- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- PORTABLE TEST EQUIPMENT
- COMPUTER SCANNERS
- COMMUNICATIONS

DESCRIPTION

The ADS902 is a high speed pipelined analog-to-digital converter that is specified to operate from a single +5V supply. This converter includes a wide bandwidth track/hold and a 10-bit quantizer. The performance is specified with a single-ended input range of 2.25V to 3.25V, or 2V to 4V. The input range is set by the external reference values.

The ADS902 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. This high performance A/D converter is specified to operate at a 30MHz sampling rate. The ADS902 is available in a 28-pin SSOP package.



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SPECIFICATIONS

At T_A = +25°C, V_S = LV_{DD} = +5V, REFB = +2.25V, REFT = +3.25V, Sampling Rate = 30MHz, unless otherwise specified.

PARAMETER	CONDITIONS	TEMP	ADS902E 1Vp-p MIN	ADS902E 1Vp-p TYP	ADS902E 1Vp-p MAX	ADS902E 2Vp-p MIN	ADS902E 2Vp-p TYP	ADS902E 2Vp-p MAX	UNITS
Resolution				10			10		Bits
Specified Temperature Range	Ambient Air		–40		+85	–40		+85	°C
ANALOG INPUT									
Specified Full Scale Input Range[1]				1			2		Vp-p
Common-Mode Voltage (Midscale)				+2.75			3		V
Track-Mode Input Bandwidth				350			*		MHz
Analog Input Bias Current				1			*		µA
Input Impedance				1.25 || 5			*		MΩ || pF
DIGITAL INPUTS									
Logic Family				TTL/HCT Compatible CMOS			TTL/HCT Compatible CMOS		
High Input Voltage, V_{IH}			+2.0		$+V_S$	*		*	V
Low Input Voltage, V_{IL}					+0.8			*	V
High Input Current, I_{IH}				±10			*		µA
Low Input Current, I_{IL}				±10			*		µA
Input Capacitance				5			*		pF
CONVERSION CHARACTERISTICS									
Sample Rate		Full	10k		30M	*		*	Samples/s
Data Latency				5			*		Clk Cyc
DYNAMIC CHARACTERISTICS									
Differential Linearity Error (Largest Code Error)									
f = 500kHz		Full		±0.3	±1.0		*	*	LSB
f = 12.5MHz		Full		±0.3	±1.0		*	*	LSB
No Missing Codes		Full		Guaranteed			Guaranteed		
Spurious-Free Dynamic Range									
f = 12.5MHz (–1dBFS[2] input)		Full		53		50	58		dB
Integral Nonlinearity Error, f = 500kHz		Full		±2.0	±4.5		*	*	LSB
Signal-to-Noise Ratio (SNR)	Referred to Sinewave Input Signal								
f = 500kHz (–1dBFS input)		Full	48	53					dB
f = 12.5MHz (–1dBFS input)		Full	48	53		52	57		dB
Maximum SNR	Referred to DC FS Input Signal								
f = 9MHz (–1dBFS input)				62			66		dB
Signal-to-(Noise + Distortion) (SINAD)									
f = 500kHz (–1dBFS input)		Full	46	50					dB
f = 3.58MHz (–1dBFS input)		Full	45	50					dB
f = 12.5MHz (–1dBFS) input)		Full	45	49		47	53		dB
Effective Number of Bits[3], f =12.5MHz				7.8					Bits
Output Noise	Input Grounded			0.2			*		LSB rms
Aperture Delay Time				4			*		ns
Aperture Jitter				7			*		ps rms
DIGITAL OUTPUTS	C_L = 15pF								
Logic Family				TTL/HCT Compatible CMOS			TTL/HCT Compatible CMOS		
Logic Coding				Straight Offset Binary			Straight Offset Binary		
High Output Voltage, V_{OH}			+2.4		LV_{DD}	*		*	V
Low Output Voltage, V_{OL}					+0.4			*	V
3-State Enable Time	OE = L			20	40		*	*	ns
3-State Disable Time	$\overline{OE}$ = H			18	10		*	*	ns
OE Internal Pull-Down to Gnd				50			*		kΩ
Power-Down Enable Time	$\overline{Pwrdn}$ = L			133			*		ns
Power-Down Disable Time	Pwrdn = H			18			*		ns
Power-Down Internal Pull-Down to Gnd				50			*		kΩ
ACCURACY									
Gain Error		Full		0.5			1		%FS
Input Offset Error[4]		Full		1.4			*		%FS
Power Supply Rejection (Gain)	ΔV_S = ±5%	Full	42	56		*	*		dB
Power Supply Rejection (Offset)	ΔV_S = ±5%	Full	42	68		*	*		dB
External REFT Voltage Range		Full	REFB +0.5	+3.25	V_S–0.8	*	+4	*	V
External REFB Voltage Range		Full	+0.8	+2.25	REFT –0.5	*	+2	*	V
Reference Input Resistance	REFT to REFB			4			*		kΩ

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = LV_{DD} = +5V, REFB = +2.25V, REFT = +3.25V, Sampling Rate = 30MHz, unless otherwise specified.

PARAMETER	CONDITIONS	TEMP	ADS902E						UNITS
			1Vp-p			2Vp-p			
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS									
Supply Voltage: $+V_S$		Full	+4.25	+5.0	+5.25	*	*	*	V
Supply Current: $+I_S$		Full		28			*		mA
Power Dissipation		Full		140	160		*	*	mW
Power Dissipation (Power Down)		Full		15			*		mW
Thermal Resistance, θ_{JA}									
28-Pin SSOP				50			*		°C/W

* Specification same as 1Vp-p.

NOTES: (1) The single-ended input range is set by REFB and REFT values. (2) dBFS means dB relative to Full Scale. (3) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (4) Offset deviation from ideal negative full scale.

ABSOLUTE MAXIMUM RATINGS

$+V_S$, LV_{DD} ..... +6V
Analog Input ..... $+V_S$ +0.3V
Logic Input ..... $+V_S$ +0.3V
Case Temperature ..... +100°C
Junction Temperature ..... +150°C
Storage Temperature ..... +150°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
ADS902E	28-Pin SSOP	324	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

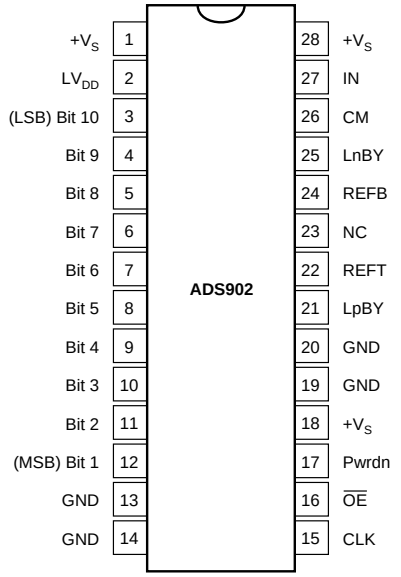
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

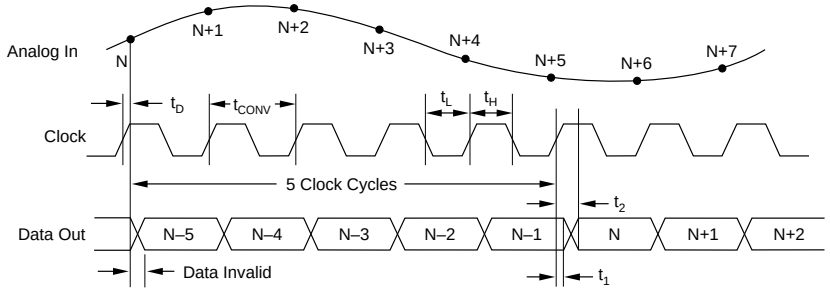
Top View **SSOP**



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	$+V_S$	Analog Supply
2	LV_{DD}	Output Logic Driver Supply Voltage
3	Bit 10	Data Bit 10 (D0, LSB)
4	Bit 9	Data Bit 9 (D1)
5	Bit 8	Data Bit 8 (D2)
6	Bit 7	Data Bit 7 (D3)
7	Bit 6	Data Bit 6 (D4)
8	Bit 5	Data Bit 5 (D5)
9	Bit 4	Data Bit 4 (D6)
10	Bit 3	Data Bit 3 (D7)
11	Bit 2	Data Bit 2 (D8)
12	Bit 1	Data Bit 1 (D9, MSB)
13	GND	Analog Ground
14	GND	Analog Ground
15	CLK	Convert Clock Input
16	$\overline{OE}$	Output Enable, Active Low
17	Pwrdn	Power Down Pin
18	$+V_S$	Analog Supply
19	GND	Analog Ground
20	GND	Analog Ground
21	LpBy	Positive Ladder Bypass
22	REFT	Top Reference
23	NC	No Connection
24	REFB	Bottom Reference
25	LnBy	Negative Ladder Bypass
26	CM	Common-Mode Voltage Output
27	IN	Analog Input
28	$+V_S$	Analog Supply

TIMING DIAGRAM

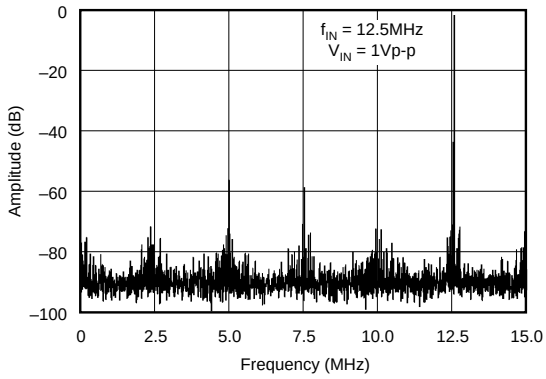


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	33		100µs	ns
t_L	Clock Pulse Low	15.5	16.5		ns
t_H	Clock Pulse High	15.5	16.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	4			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

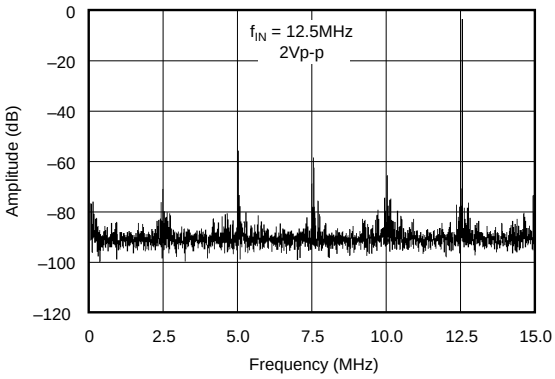
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = LV_{DD} = +5V, REFB = +2.25V, REFT = +3.25V, and Sampling Rate = 30MHz, unless otherwise specified.

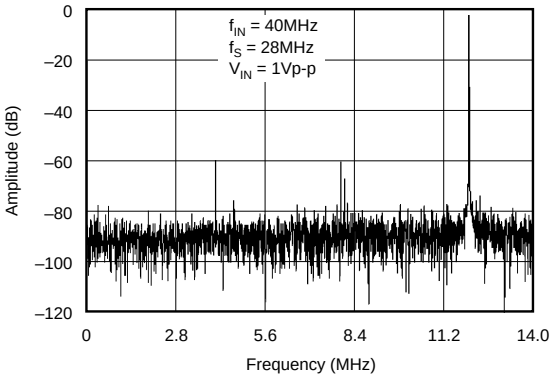
SPECTRAL PERFORMANCE



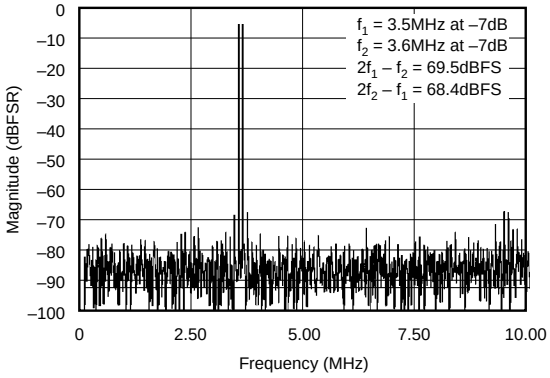
SPECTRAL PERFORMANCE



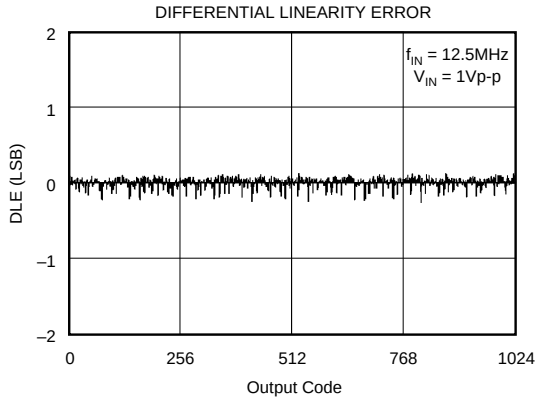
UNDERSAMPLING



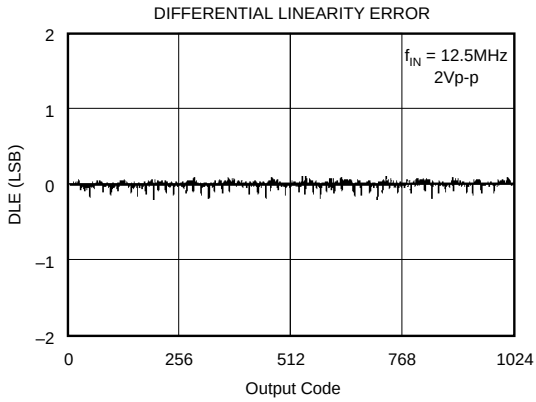
FREQUENCY SPECTRUM



DIFFERENTIAL LINEARITY ERROR



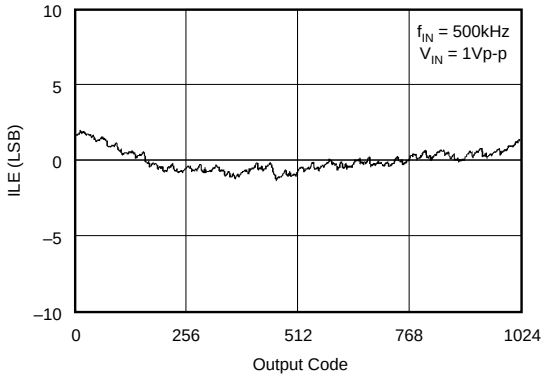
DIFFERENTIAL LINEARITY ERROR



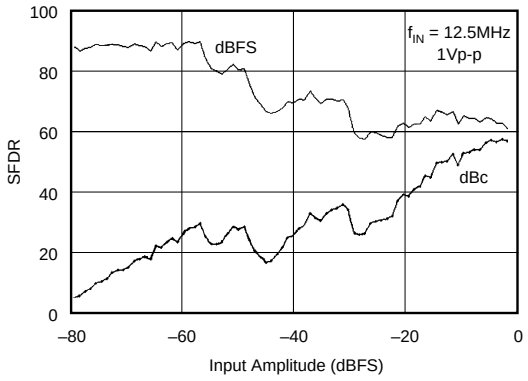
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = Logic V_{DD} = +5V, REFB = 2.25V, REFT = 3.25V, Sampling Rate = 30MHz, unless otherwise specified.

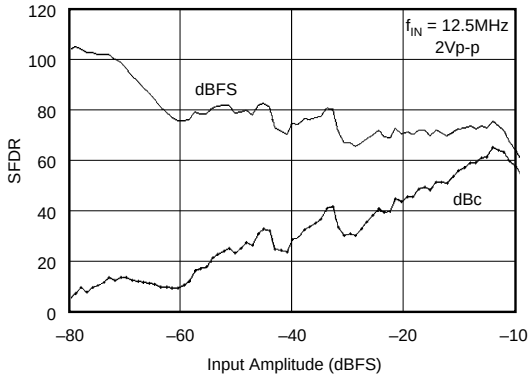
INTEGRAL LINEARITY ERROR



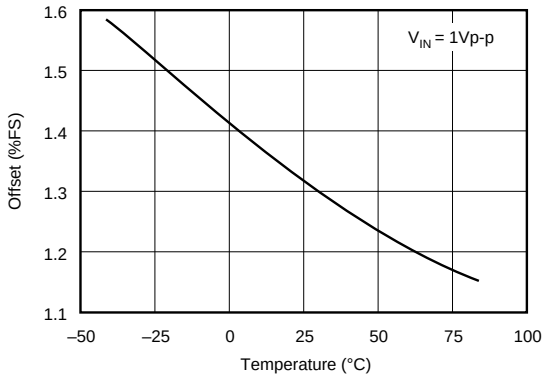
SWEPT POWER SFDR



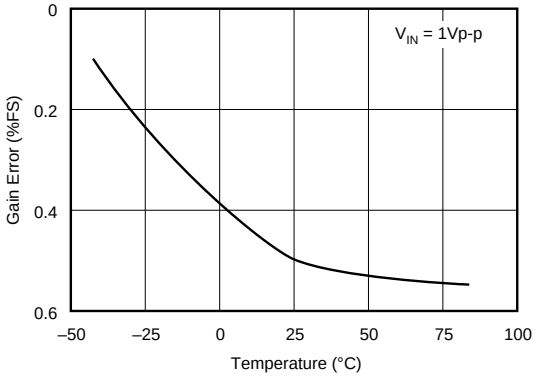
SWEPT POWER SFDR



OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



THEORY OF OPERATION

The ADS902 is a high speed sampling analog-to-digital converter that utilizes a pipeline architecture. The fully differential topology and digital error correction guarantee 10-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi1$ and $\phi2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors (C_1). In the next clock phase, $\phi1$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one acquisition cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit also converts the single-ended input signal into a fully differential signal for the subsequent quantizer. Consequently, the input signal-to-noise performance. Other parameters such as small-signal and full-power bandwidth, and wideband noise are also defined in this stage.

The pipelined quantizer architecture has 9 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit

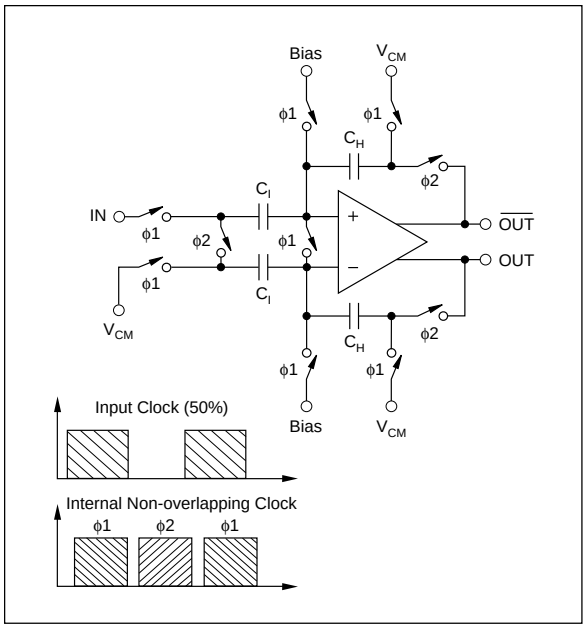


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

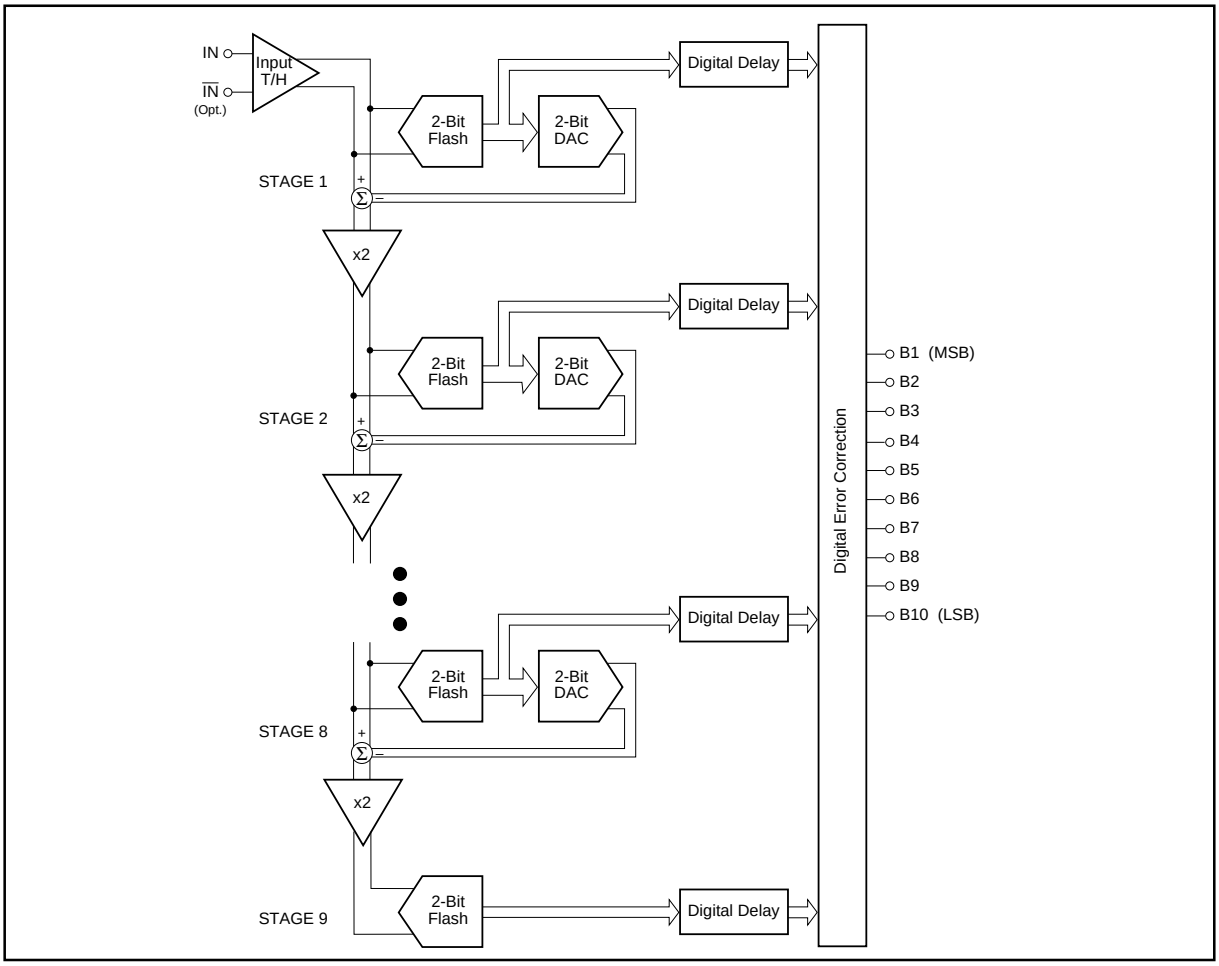


FIGURE 2. Pipeline A/D Architecture.

quantizer stage converts on the edge of the sub-clock, which is the same frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique provides the ADS902 with excellent differential linearity and guarantees no missing codes at the 10-bit level.

As a result of this pipeline architecture, there is a 5.0 clock cycle data delay (latency) from the start convert signal to the corresponding valid output data.

To accommodate a bipolar signal swing, the ADS902 operates with a common-mode voltage (V_{CM}) which is derived from the external references. Due to the symmetric resistor ladder inside the ADS902, the V_{CM} is situated between the top and bottom reference voltage. Equation (1) can be used for calculating the common-mode voltage level.

$$V_{CM} = (REFT + REFB)/2 \quad (1)$$

At the same time, the two external reference voltages define the full-scale input range for the ADS902. This makes it possible for the input range to be adapted to the signal swing of the front end.

APPLICATIONS

SIGNAL SWING AND COMMON-MODE CONSIDERATIONS

The ADS902 is designed to operate on a +5V single supply voltage. The nominal input signal swing is 1Vp-p, situated between +2.25V and +3.25V. This means that the signal swings ±0.5V around a common-mode voltage of +2.75V. In some applications it might be advantageous to increase the input signal swing to 2Vp-p which will improve the achievable ac-performance. However, consideration should be given to keeping the signal swing within the linear region of operation of the driving circuitry to avoid any excessive distortion. In extreme situations, the performance of the converter will start to degrade due to variations of the input's switch-on resistance over the input voltage. Therefore, the signal swing should remain approximately 0.5V away from each rail during normal operation.

DRIVING THE ANALOG INPUTS

AC-COUPLED DRIVER

Figure 3 shows an example of an ac-coupled, single-ended interface circuit using a high-speed op amp that operates on dual supplies (OPA650, OPA658). The mid-point reference voltage, V_{CM}, biases the bipolar, ground-referenced input signal. The capacitor C_1 and resistor R_1 form a high-pass filter with the –3dB frequency set at

$$f_{-3dB} = 1/(2\ \pi\ R_1\ C_1) \quad (2)$$

The values for C_1 and R_1 are not critical in most applications and can be set freely, e.g. the shown values correspond to a frequency of 1.6kHz.

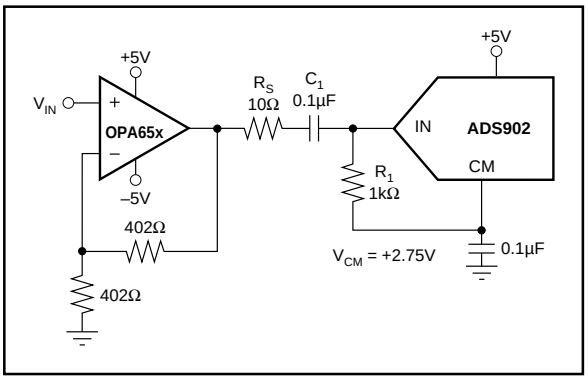


FIGURE 3. Typical AC-Coupled Interface Circuit. (External references not shown.)

Figure 4 depicts a circuit that can be used in single-supply applications. The mid-reference voltage biases the op amp up to the appropriate common-mode voltage, for example V_{CM} = +2.75V. With the use of capacitor C_G the DC gain for the non-inverting op amp input is set to +1V/V. As a result the transfer function is modified to

$$V_{OUT} = V_{IN}\ \{(1 + R_F/R_G) + V_{CM}\} \quad (3)$$

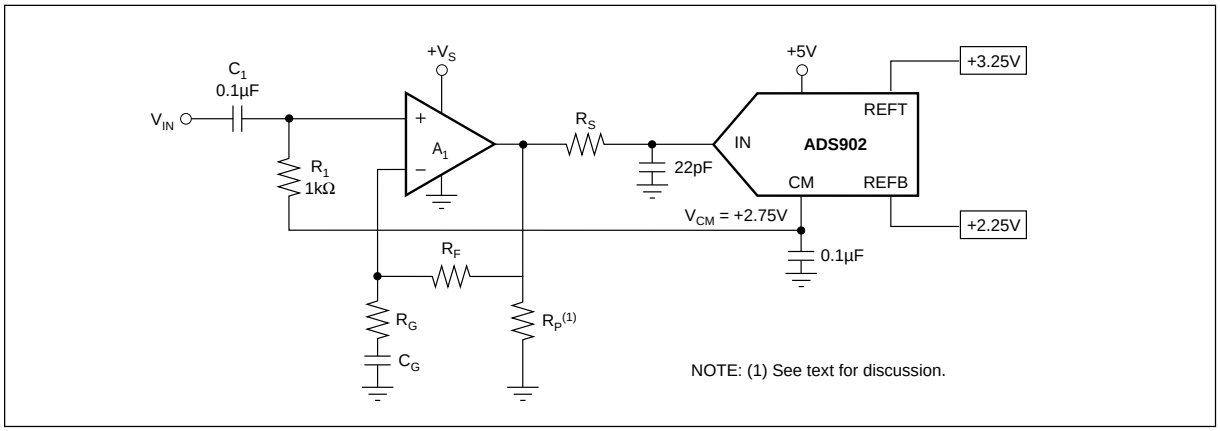


FIGURE 4. AC-Coupled, Single-Supply Interface Circuit.

Again, the input coupling capacitor C_1 and resistor R_1 form a high-pass filter. At the same time, the input impedance is defined by R_1. Possible op amps for A_1 are CLC452, EL2180 or LM6152. Depending on the selected amplifier, the use of a pull-up/pull-down resistor (R_P), located directly at its output, may considerably improve its distortion performance. Resistor R_S isolates the op amp's output from the capacitive load to avoid gain peaking or even oscillation. It can also be used to establish a defined bandwidth to reduce the wideband noise. Its value is usually between 10Ω and 100Ω.

DC-COUPLED INTERFACE CIRCUIT

Shown in Figure 5 is a single-supply, DC-coupled circuit which can be set in a gain of –1V/V or higher. Depending on the gain determined by R_F/R_{IN}, the divider ratio set by resistors R_1 and R_2 must be adjusted to yield the correct common-mode voltage for the ADS902. With a +5V supply, the nominal signal input range of the ADS902 is 1Vp-p, typically centered around the common-mode voltage of +2.75V.

EXTERNAL REFERENCE

The ADS902 requires an external top and bottom reference on pin 22 (REFT) and 24 (REFB). Internally those pins are connected through a resistor ladder, which has a nominal resistance of 4kΩ (±15%). In order to establish a correct voltage drop across the ladder the external reference circuit must be able to supply typically 250µA of current. With this current the full-scale input range of the ADS902 is set between +2.25V and +3.25V. In general, the voltage drop across REFT and REFB determines the input full-scale range (FSR) of the ADS902. Equation (4) can be used to calculate the span.

$$FSR = REFT - REFB \quad (4)$$

Depending on the application several options exist how to supply the external reference voltages to the ADS902 without degrading the typical performance.

LOW-COST REFERENCE SOLUTION

The easiest way to achieve the required reference voltages is to place the reference ladder of the ADS902 between the supply rails. Two additional resistors (R_T, R_B) are necessary to set the correct current through the ladder (see Figure 6). However, depending on the desired full-scale swing and supply voltage, different resistor values might be selected.

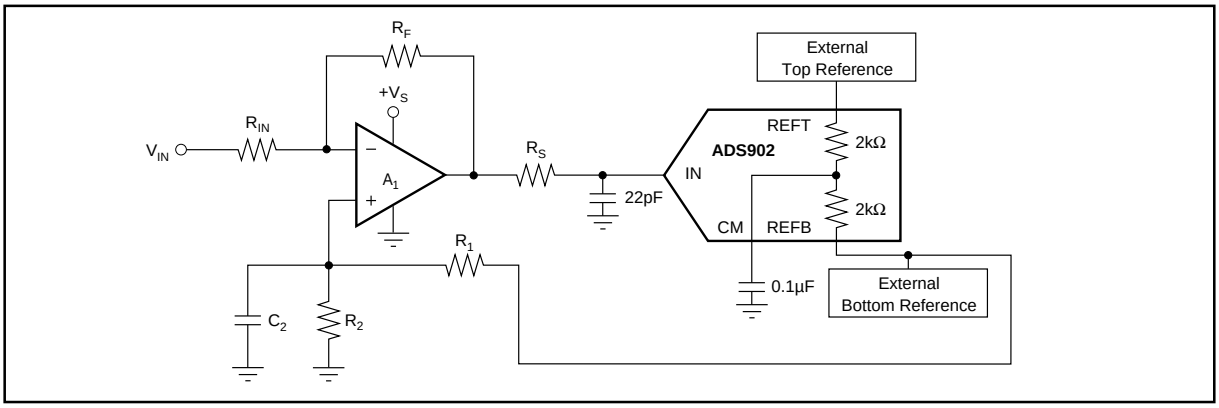


FIGURE 5. DC-Coupled, Single-Supply Interface Circuit.

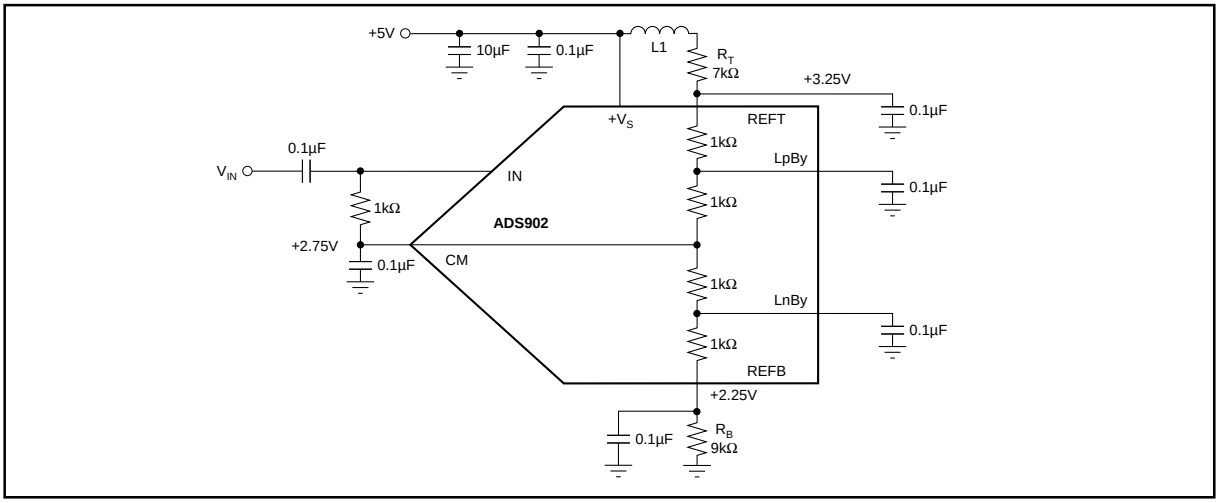


FIGURE 6. Low Cost Solution to Supply External Reference Voltages.

When selecting this reference circuit, the trade-offs are variations in the reference voltages due to component tolerances and power supply variations. In either case, it is recommended to bypass the reference ladder with at least 0.1µF ceramic capacitors as shown in Figure 6. The purpose of the capacitors is twofold; they will bypass most of the high frequency transient noise which results from feedthrough of the clock and switching noise from the S/H stages and secondly, they serve as a charge reservoir to supply instantaneous current to internal nodes.

PRECISE REFERENCE SOLUTION

For those applications requiring a higher level of dc accuracy and drift, a reference circuit with a precision reference element might be used (see Figure 7). A stable +2.5V reference voltage is established by a two terminal bandgap reference diode, the REF1004-2.5. Using a general-purpose single-supply dual operational amplifier (A1), like an OPA2237, OPA2234 or MC34072, the two required reference voltages for the ADS902 can be generated by setting each op amp to the appropriate gain. For example, set REFT to +3.25V and REFB to +2.25V.

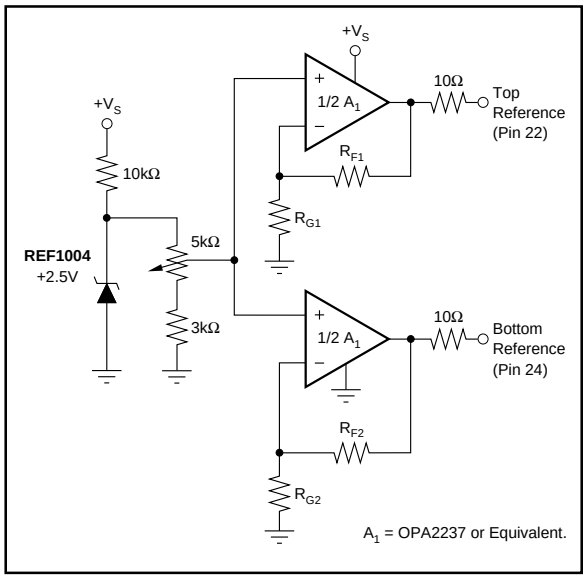


FIGURE 7. Precise Solution to Supply External Reference Voltages to the ADS902.

CLOCK INPUT

The clock input of the ADS902 is designed to accommodate either +5V or +3V CMOS logic levels. To drive the clock input with a minimum amount of duty cycle variation and support maximum sampling rates (30MSPS), high speed or advanced CMOS logic should be used (HC/HCT, AC/ACT). When digitizing at high sampling rates, a 50% duty cycle along with fast rise and fall times (2ns or less) are recommended to meet the rated performance specifications. However, the ADS902 performance is tolerant of duty-cycle variations of as much as ±5%, which should not affect performance. For applications operating with input frequencies up to Nyquist or undersampling applications, special consideration must be made to provide a clock with very low jitter. Clock jitter leads to aperture jitter (t_A) which can be the ultimate limitation to achieving good SNR performance. Equation (5) shows the relationship between aperture jitter, input frequency and the signal-to-noise ratio:

$$SNR = 20\log_{10}[1/(2\pi f_{IN} t_A)] \quad (5)$$

For example, with a 5MHz full-scale input signal and an aperture jitter of t_A = 20ps rms, the SNR is clock jitter limited to 54dB.

DIGITAL OUTPUTS

The digital outputs of the ADS902 are standard CMOS stages and designed to be compatible with both high speed TTL and CMOS logic families. The logic thresholds are for low-voltage CMOS: V_{OL} = 0.4V, V_{OH} = 2.4V, which allows the ADS902 to directly interface to 3V-logic. The digital outputs of the ADS902 uses a dedicated digital supply pin (see Figure 8). By adjusting the voltage on LV_{DD}, the digital output levels will vary respectively. In any case, it is recommended to limit the fan-out to one, in order to keep the capacitive loading on the data lines below the specified 15pF. If necessary, external buffers or latches may be used which provide the added benefit of isolating the A/D converter from any digital activities on the bus from coupling back high frequency noise and degrading the performance. The standard output coding is Straight Offset Binary where the full scale input signal corresponds to all "1"s at the output (see Table I). The digital outputs of the ADS902 can be set to a high impedance state by driving the $\overline{OE}$ (pin 16) with a logic "H". Normal operation is achieved with a "L" at $\overline{OE}$ or left unconnected due to the internal pull-down resistor.

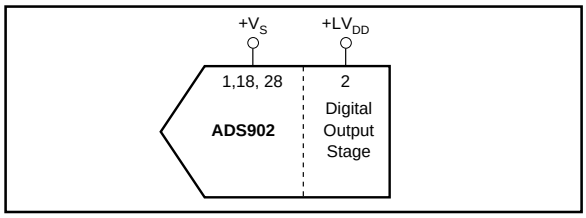


FIGURE 8. Independent Supply Connection for Output Stage.

SINGLE-ENDED INPUT	STRAIGHT OFFSET BINARY (SOB) PIN 12 FLOATING or LO
+FS (IN = +3.25V)	1111111111
+FS –1LSB	1111111111
+FS –2LSB	1111111110
+3/4 Full Scale	1110000000
+1/2 Full Scale	1100000000
+1/4 Full Scale	1010000000
+1LSB	1000000001
Bipolar Zero (IN +2.75V)	1000000000
–1LSB	0111111111
–1/4 Full Scale	0110000000
–1/2 Full Scale	0100000000
–3/4 Full Scale	0010000000
–FS +1LSB	0000000001
–FS (IN = +2.25V)	0000000000

TABLE I. Coding Table for the ADS902.

POWER-DOWN MODE

The ADS902's low power consumption can be reduced even further by initiating a power-down mode. To do so, the Pwrdn-Pin (Pin 17) must be tied to a logic "High" reducing the current drawn from the supply by about 88%. In normal operation the power-down mode is disabled by an internal pull-down resistor (50kΩ).

During power-down, the digital outputs are set into the high-impedance condition (3-state). With the clock applied, the converter does not accurately process the sampled signal. After removing the power-down condition the output data from the following 5 clock cycles is invalid (data latency).

DECOUPLING AND GROUNDING CONSIDERATIONS

The ADS902 converter has several supply pins, one of which is dedicated to supply only the output driver. The remaining supply pins are not, as is often the case, divided into analog and digital supply pins since they are internally connected on the chip. For this reason it is recommended to treat the converter as an analog component and to power it from the analog supply only. Digital supply lines often carry high levels of noise which can couple back into the converter and limit the achievable performance.

Because of the pipeline architecture, the converter also generates high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the analog supplies. In most cases 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible.

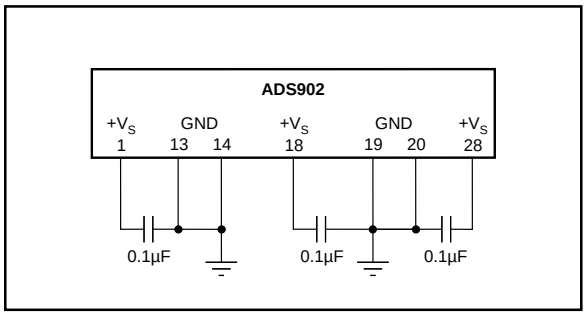


FIGURE 9. Recommended Bypassing for Analog Supply Pins.