

OPA2107

Precision Dual *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: $8\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
- LOW V_{os} : 1mV max
- LOW DRIFT: $10\mu\text{V}/^\circ\text{C}$ max
- LOW I_{B} : 10pA max
- FAST SETTLING TIME: $2\mu\text{s}$ to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

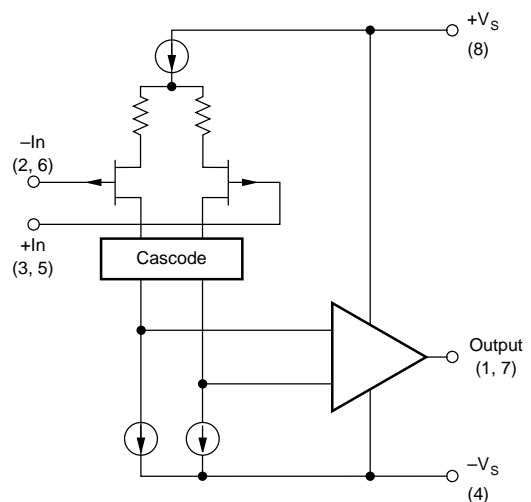
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision *Difet* performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET[®] type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (*Difet*) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP and SOIC packages. Industrial temperature range versions are available.



Difet[®] Burr-Brown Corp.
BIFET[®] National Semiconductor

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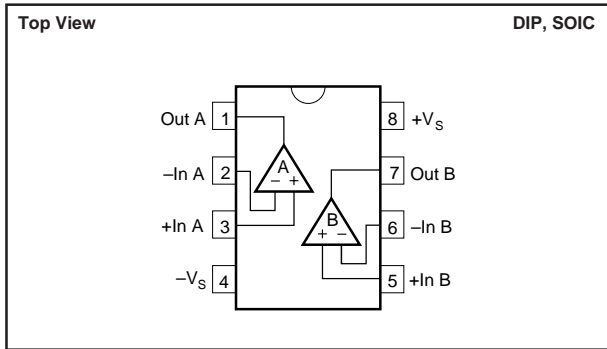
SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	CONDITION	OPA2107AP, AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Over Specified Temperature Average Drift Over Specified Temperature Power Supply Rejection	$V_{CM} = 0\text{V}$ $V_S = \pm 10$ to $\pm 18\text{V}$		100 0.5 3 96	1 2 10	mV mV $\mu\text{V}/^\circ\text{C}$ dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Over Specified Temperature Input Offset Current Over Specified Temperature	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		4 0.25 1	10 1.5 8 1	pA nA pA nA
INPUT NOISE Voltage: $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ BW = 0.1 to 10Hz BW = 10 to 10kHz Current: $f = 0.1\text{Hz}$ thru 20kHz BW = 0.1Hz to 10Hz	$R_S = 0$		30 12 9 8 1.2 0.85 1.2 23		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ μVrms $\text{fA}/\sqrt{\text{Hz}}$ fAp-p
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 2$ $10^{14} \parallel 4$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	$V_{CM} = \pm 10\text{V}$	± 10.5 ± 10.2 80	± 11 ± 10.5 94		V V dB
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	82 80	96 94		dB dB
DYNAMIC RESPONSE Slew Rate Settling Time: 0.1% 0.01% Gain Bandwidth Product THD + Noise Channel Separation	$G = +1$ $G = -1$, 10V Step $G = 100$ $G = +1$, $f = 1\text{kHz}$ $f = 100\text{Hz}$, $R_L = 2\text{k}\Omega$	13	18 1.5 2 4.5 0.001 120		V/ μs μs μs MHz % dB
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 15 ± 4.5		V V mA
OUTPUT Voltage Output Over Specified Temperature Short Circuit Current Output Resistance, Open-Loop Capacitive Load Stability	$R_L = 2\text{k}\Omega$ 1MHz $G = +1$	± 11 ± 10.5 ± 10	± 12 ± 11.5 ± 40 70 1000		V V mA Ω pF
TEMPERATURE RANGE Specification Operating Storage Thermal Resistance (θ_{JA}) 8-Pin DIP 8-Lead Surface Mount		-25 -25 -40		+85 +85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

NOTE: (1) Specified with devices fully warmed up.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	±18V
Input Voltage Range	±V _S ±2V
Differential Input Voltage	Total V _S ±4V
Operating Temperature	
P and U Packages	-25°C to +85°C
Storage Temperature	
P and U Packages	-40°C to +125°C
Output Short Circuit to Ground (T _A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
P Package (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

NOTE: Stresses above these ratings may cause permanent damage.

PACKAGE/ORDERING INFORMATION

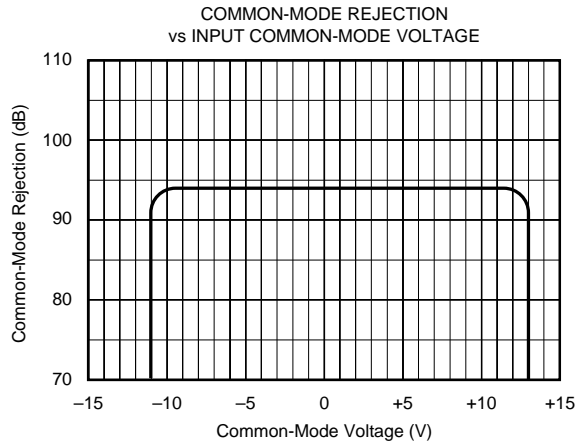
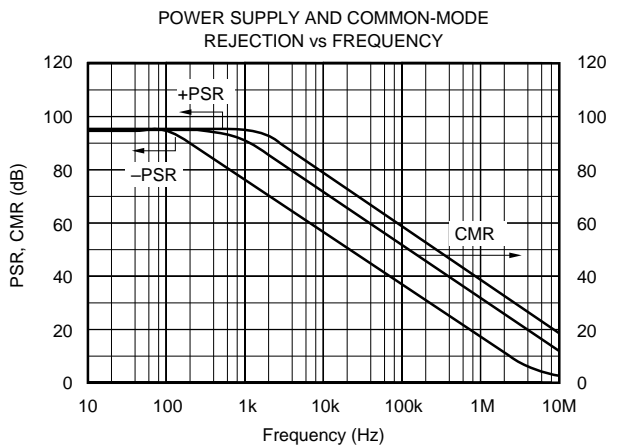
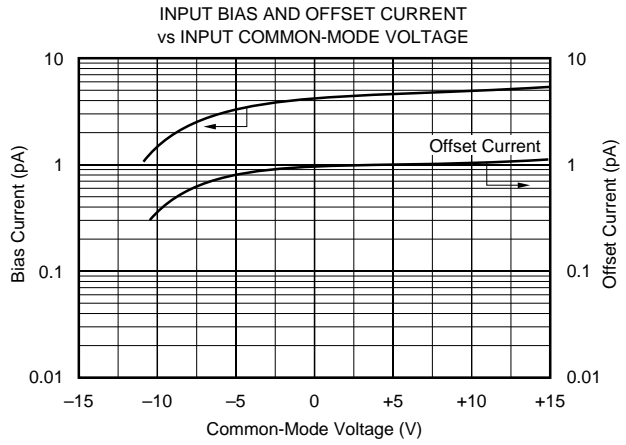
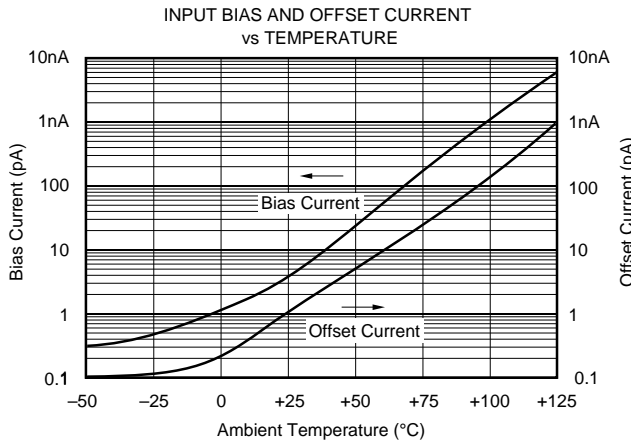
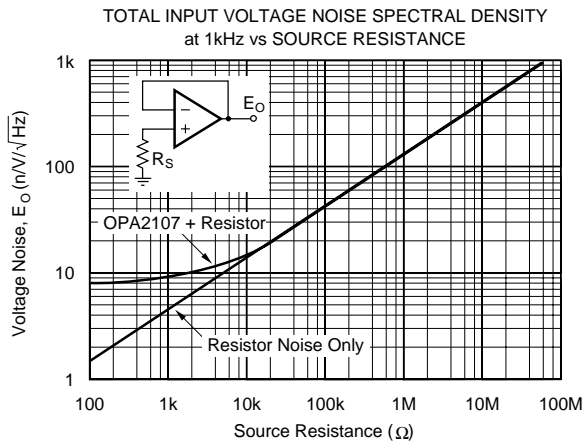
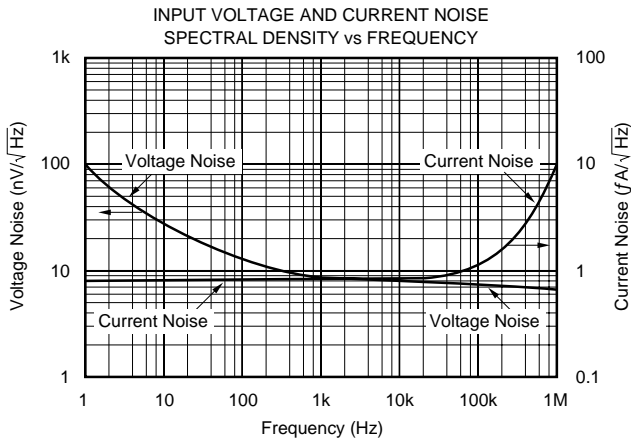
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
OPA2107AP	Plastic DIP	006	-25 to +85°C
OPA2107AU	SO-8 SOIC	182	-25 to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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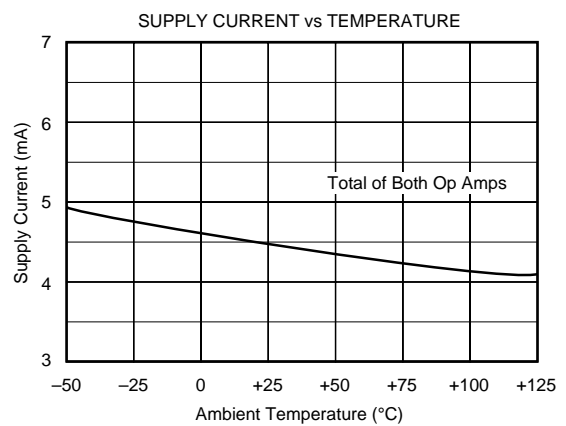
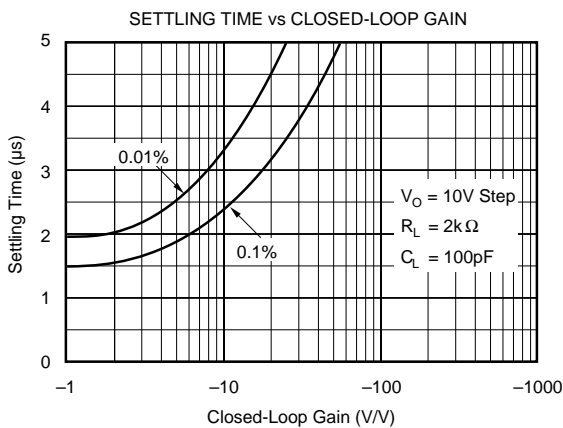
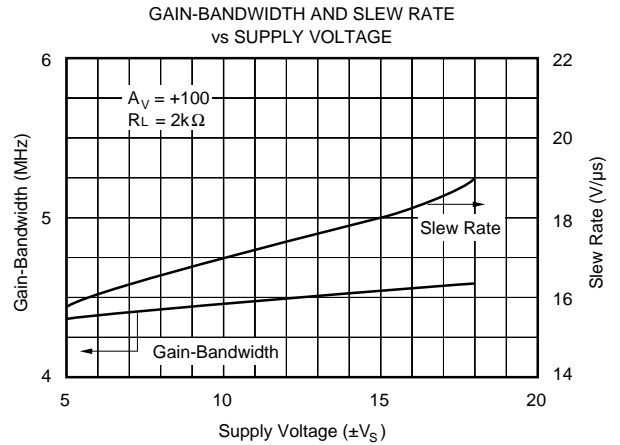
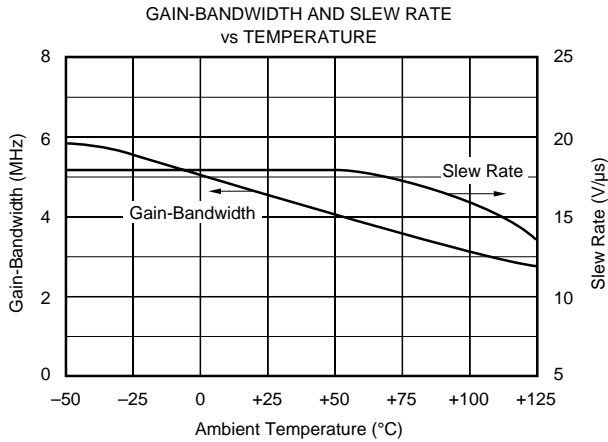
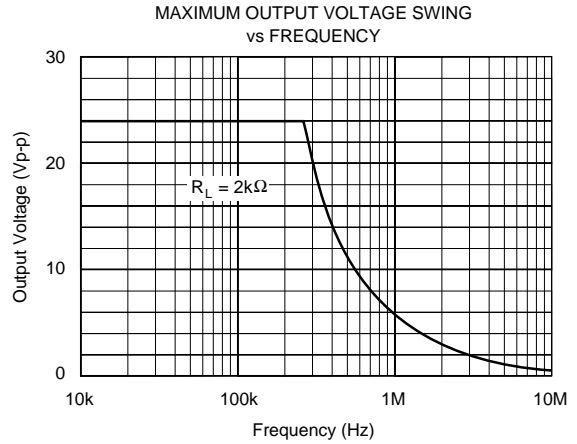
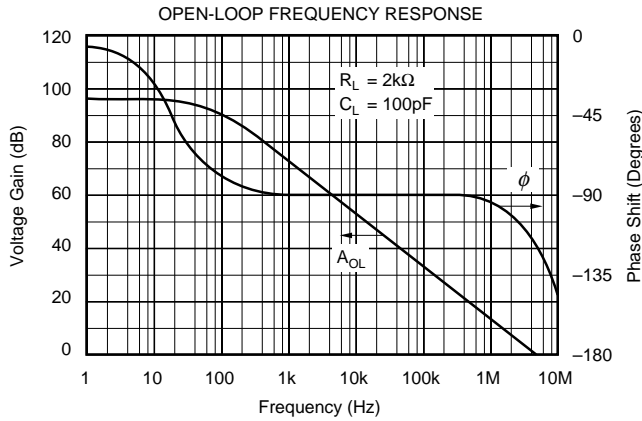
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



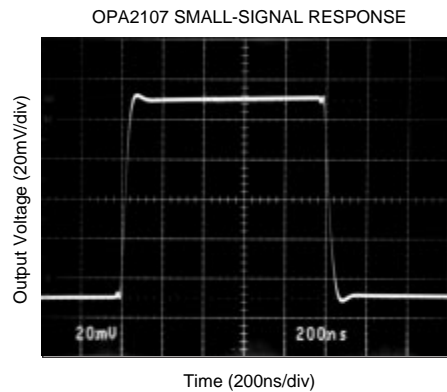
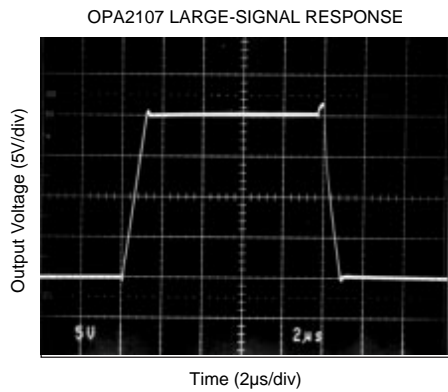
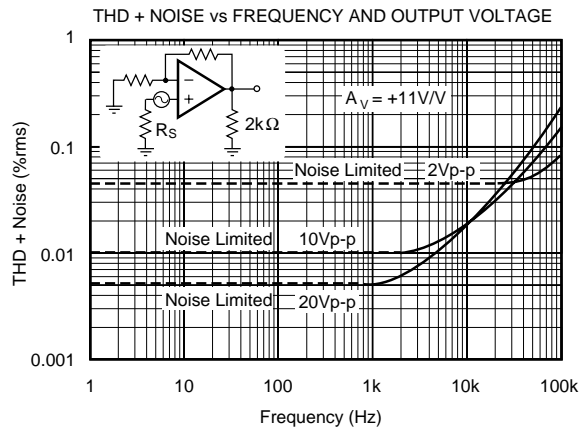
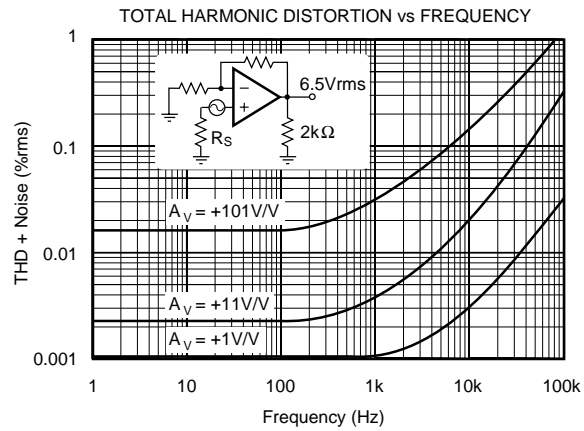
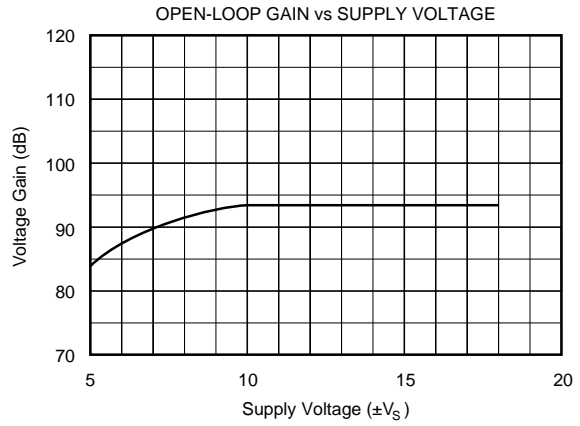
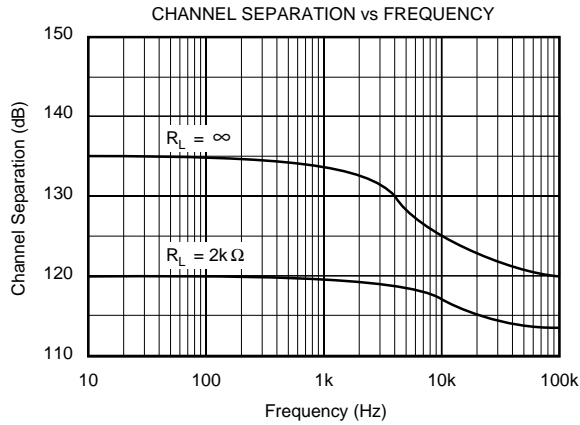
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's *Difet* input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

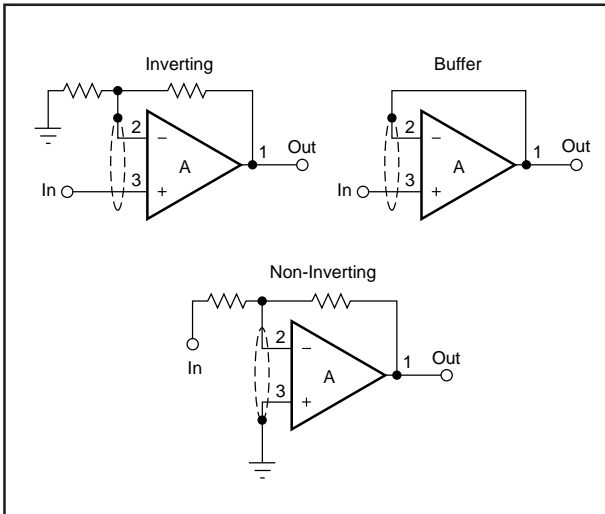


FIGURE 1. Connection of Input Guard.

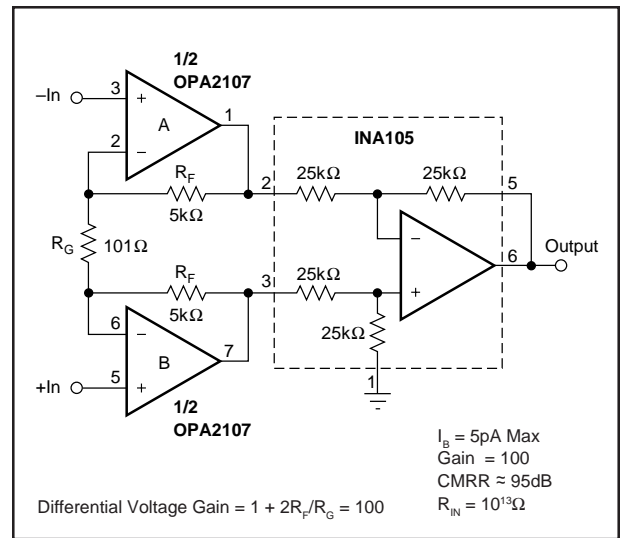


FIGURE 2. FET Input Instrumentation Amplifier.

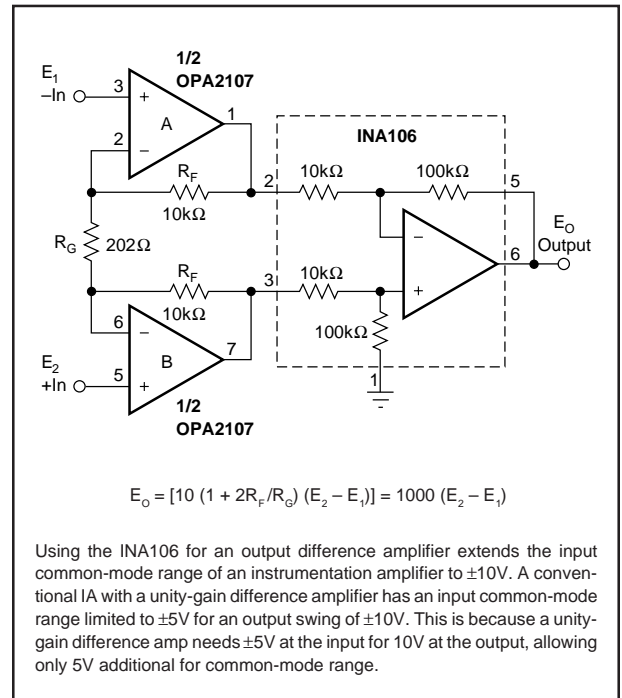


FIGURE 3. Precision Instrumentation Amplifier.