



OPA502

High Current, High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 10A
- WIDE POWER SUPPLY VOLTAGE:
 $\pm 10V$ to $\pm 45V$
- USER-SET CURRENT LIMIT
- SLEW RATE: $10V/\mu s$
- FET INPUT: $I_B = 200pA$ max
- CLASS A/B OUTPUT STAGE
- QUIESCENT CURRENT: 25mA max
- HERMETIC TO-3 PACKAGE —
ISOLATED CASE

DESCRIPTION

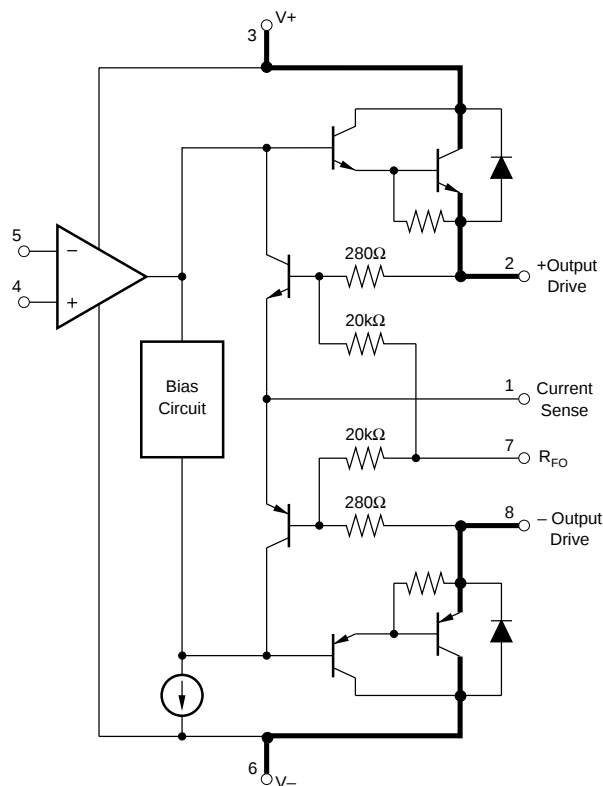
The OPA502 is a high output current operational amplifier designed to drive a wide range of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from crossover distortion. Resistor-programmable current limits provide protection for both the amplifier and the load during abnormal operating conditions. An adjustable foldover current limit can also be used to protect against potentially damaging conditions.

The OPA502 employs a custom monolithic op amp/driver circuit and rugged complementary output transistors, providing excellent DC and dynamic performance.

The industry-standard 8-pin TO-3 package is electrically isolated from all circuitry. This allows the OPA502 to be mounted directly to a heat sink without cumbersome insulating hardware which degrade thermal performance. The OPA502 is available in $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.

APPLICATIONS

- MOTOR DRIVER
- SERVO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- ACTUATOR DRIVER
- AUDIO AMPLIFIER
- TEST EQUIPMENT



SPECIFICATIONS

T_{CASE} = +25°C, V_S = ±40V, unless otherwise noted.

PARAMETER	CONDITION	OPA502BM			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply	Specified Temp. Range V _S = ±10V to ±45V	74	±0.5 ±5 92	±5	mV μV/°C dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current	V _{CM} = 0V V _{CM} = 0V		12 ±3	200	pA pA
NOISE Input Voltage Noise Noise Density, Current Noise Density,	f = 1kHz f = 1kHz		25 3		nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-Mode Input Range, Positive Negative Common-Mode Rejection	Linear Operation Linear Operation V _{CM} = ±35V	(V+) –5 (V–) +5 74	(V+) –4 (V–) +4 106		V V dB
INPUT IMPEDANCE Differential Common-Mode			10 ¹² 5 10 ¹² 4		Ω pF Ω pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	V _O = ±34V, R _L = 6Ω	92	103		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Full-Power Bandwidth Total Harmonic Distortion Capacitive Load	G = +10, R _L = 50Ω 68Vp-p, R _L = 6Ω G = +3, f = 20kHz V _O = 20V, R _L = 8Ω	5	2.0 10 See Typical Curves 0.06 See Figure 6		MHz V/μs %
OUTPUT Voltage Output, Positive Negative Positive Negative Current Output Short Circuit Current	I _O = 10A I _O = 10A I _O = 1A I _O = 1A	(V+) –6 (V–) +6	(V+) –3.5 (V–) +3.6 (V+) –2.5 (V–) +3.1 See SOA Curves Resistor Programmed		V V V V
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	I _O = 0	±10	±40 ±20	±45 ±25	V V mA
TEMPERATURE RANGE Specification Storage Thermal Resistance, θ _{JC} θ _{JA}	DC AC f ≥ 50Hz No Heat Sink	–40 –55	1.25 0.8 30	+85 +125 1.4 0.9	°C °C °C/W °C/W °C/W

NOTE: (1) High-speed test at T_J = 25°C.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V–	90V
Output Current	See SOA Curve
Input Voltage	(V–) –1V to (V+) +1V
Case Temperature, Operating	150°C
Junction Temperature	200°C

NOTE: (1) Stresses above these ratings may cause permanent damage.

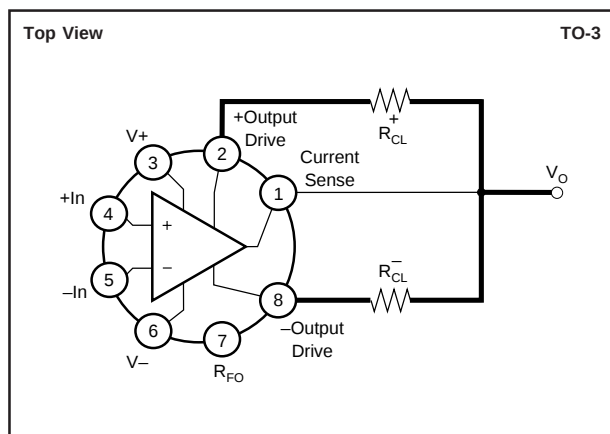
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
OPA502BM	8-Pin TO-3	030	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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PIN CONFIGURATION



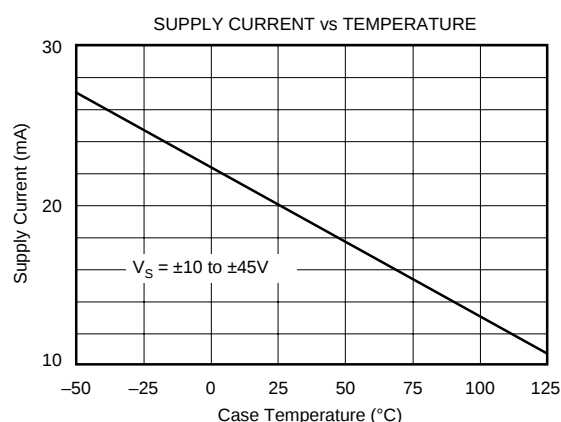
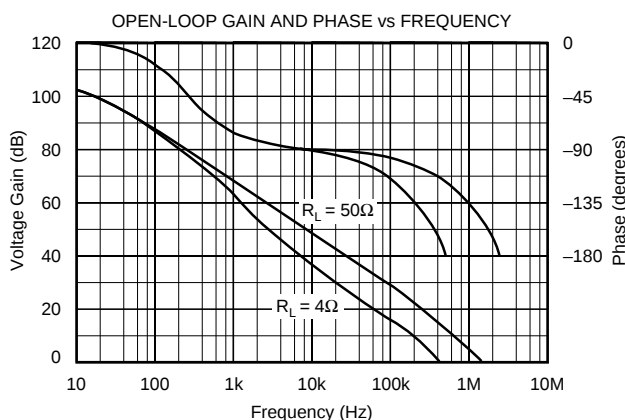
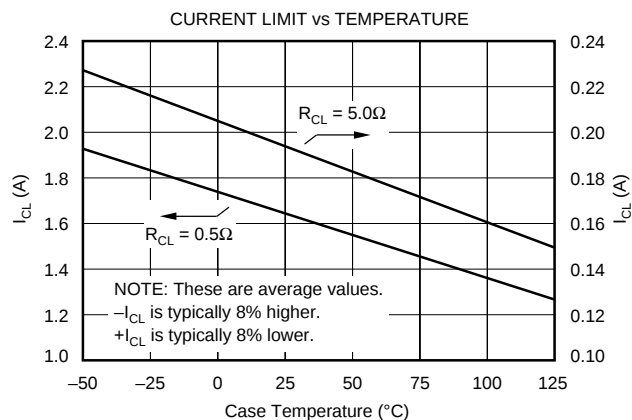
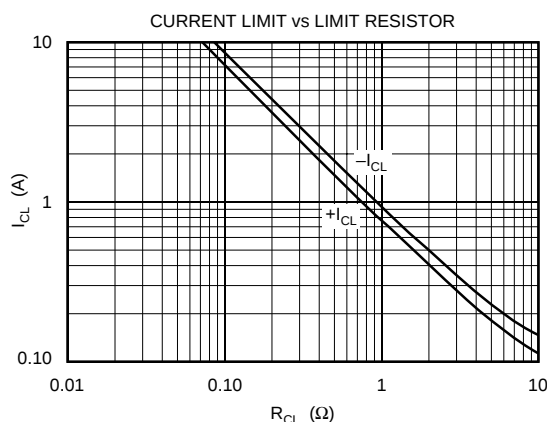
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

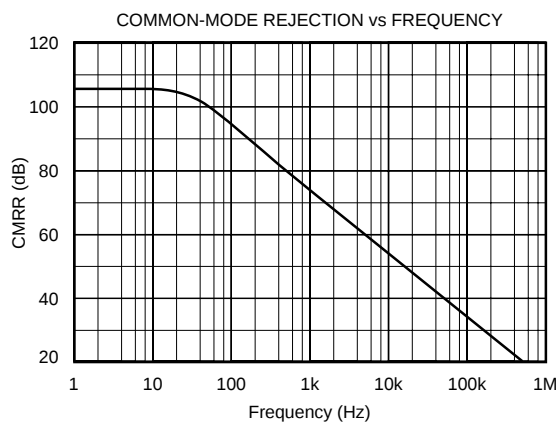
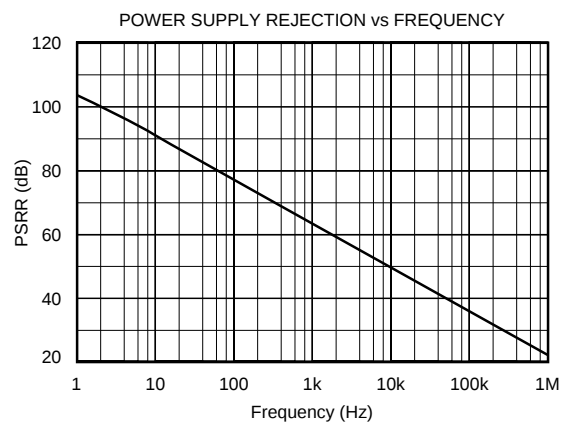
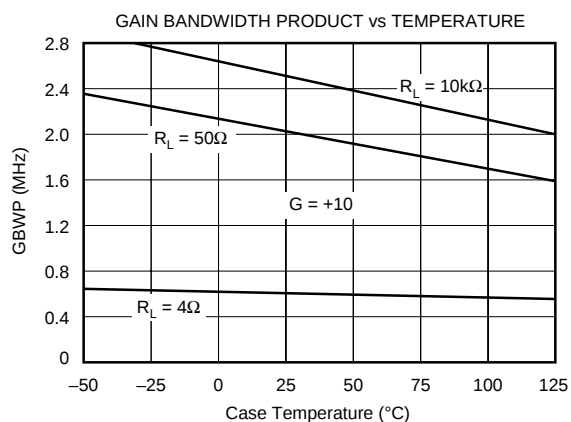
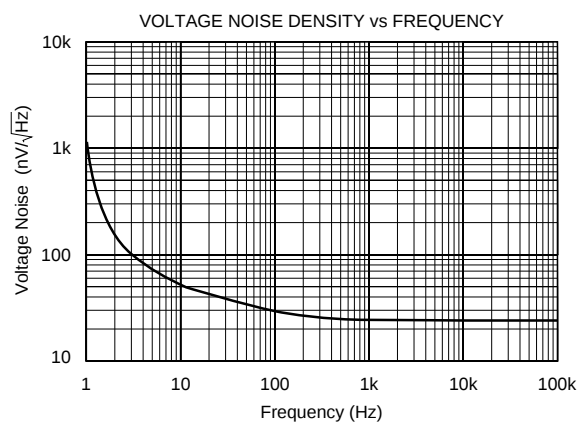
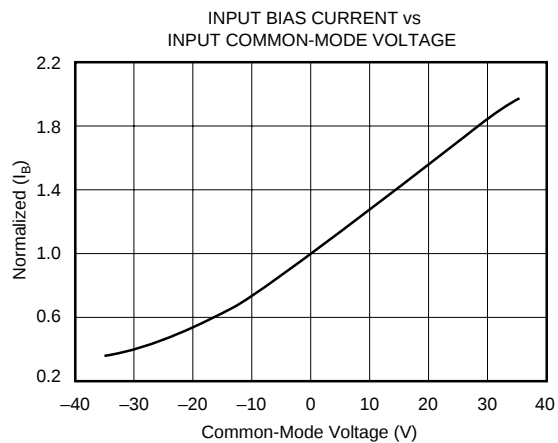
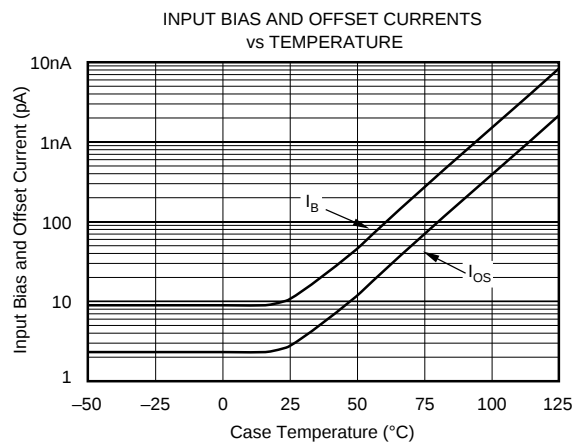
TYPICAL PERFORMANCE CURVES

$T_{CASE} = +25^{\circ}\text{C}$, $V_S = \pm 40\text{V}$, unless otherwise noted.



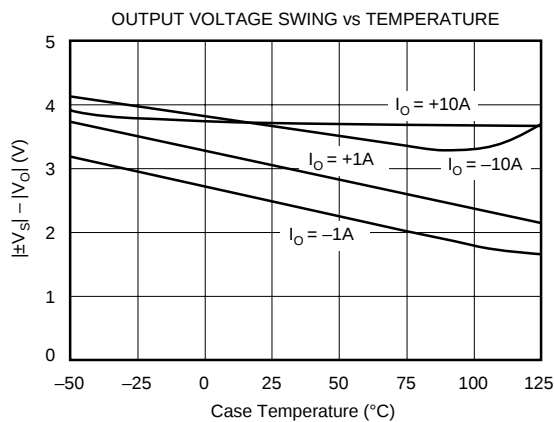
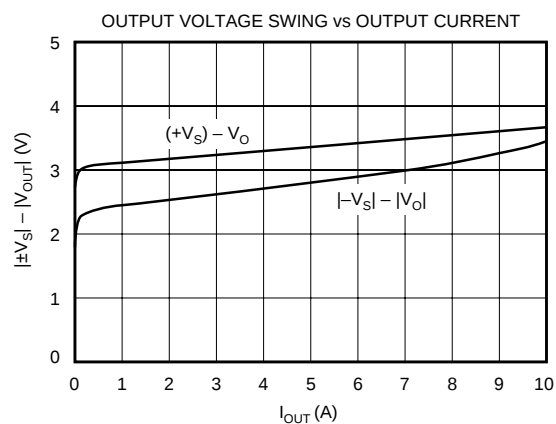
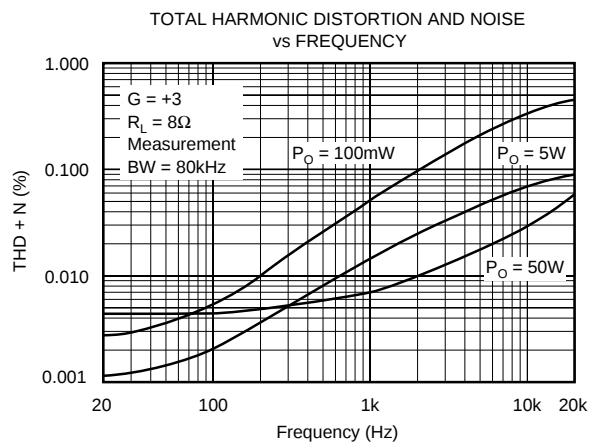
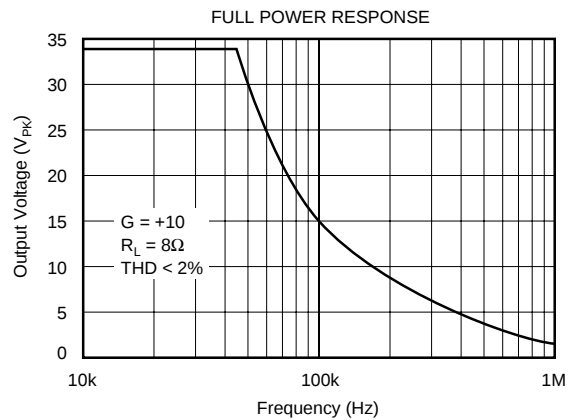
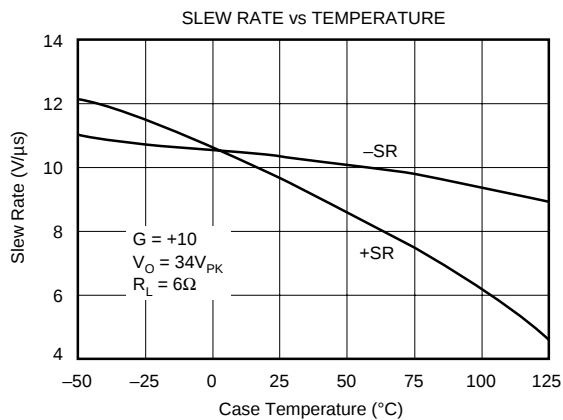
TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}\text{C}$, $V_S = \pm 40\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

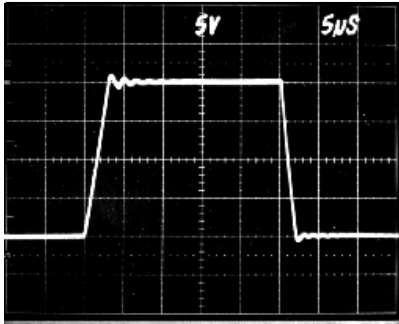
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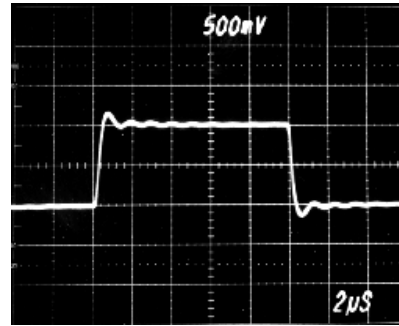
TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}\text{C}$, $V_S = \pm 40\text{V}$, unless otherwise noted.

LARGE SIGNAL RESPONSE
 $G = +3$, $R_L = 4\Omega$



SMALL SIGNAL RESPONSE
 $G = +3$, $C_L = 1000\text{pF}$



APPLICATIONS INFORMATION

Power supply terminals should be bypassed with low series impedance capacitors such as ceramic or tantalum close to the device pins. Power supply wiring should have low series impedance and inductance. Figure 1 indicates the high current connections in bold lines.

Current limit is set with two external resistors—one for positive output current and one for negative output current (see Figure 1). For conventional current limit, independent of output voltage, pin 7 should be left open (see “Foldback Current Limit”). Limiting occurs when the output current causes sufficient voltage drop across R_{CL} to turn on the respective current limit transistor. The limit current decreases at high temperature (see typical performance curve “Current Limit vs Temperature”).

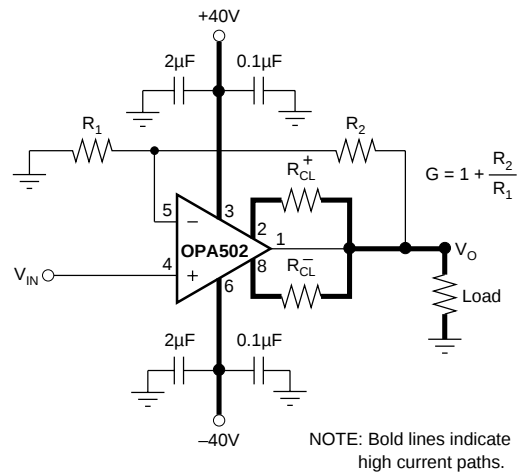
Figure 1 also shows nominal current limit produced by standard resistor values. See also the typical performance curve “Current Limit vs Limit Resistance”. The output current must flow through this resistor, so its power rating must be chosen accordingly. The table in Figure 1 shows the power dissipation of the current limit resistor during continuous current limit (room temperature). Connections from the current limit resistors to the device pins can typically add 0.02Ω to 0.05Ω to the effective value of R_{CL} . This significantly affects the current limit value for high output currents.

The current limit resistors can be chosen from a variety of types. Most common wire-wound types are satisfactory, although some physically large types may have excessive inductance which can cause problems. You should test your circuits with the exact resistor type planned for production use.

You can set different current limits for positive and negative current. Resistors are chosen with the same table of values in Figure 1.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transis-



R_{CL} (Ω)	I_{CL} at 25°C (A)	Power Dissipation ¹ of R_{CL} (W)
10	0.11	0.12
5	0.19	0.18
2	0.44	0.39
1	0.78	0.61
0.68	1.22	1.0
0.5	1.65	1.4
0.3	2.73	2.2
0.2	4.0	3.2
0.15	5.4	4.4
0.1	8.1	6.6

NOTE 1: Power dissipation during continuous current limit at $T_{CASE} = +25^{\circ}\text{C}$.

FIGURE 1. Basic Circuit Connections.

tor. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE} . The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

The safe output current decreases as V_{CE} increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage ($V+$ or $V-$) across the conducting transistor. With $V_S = \pm 40V$ the current limit must be set for 3A (25°C) to be safe for continuous short-circuit to ground. For further insight on SOA, consult AB-039.

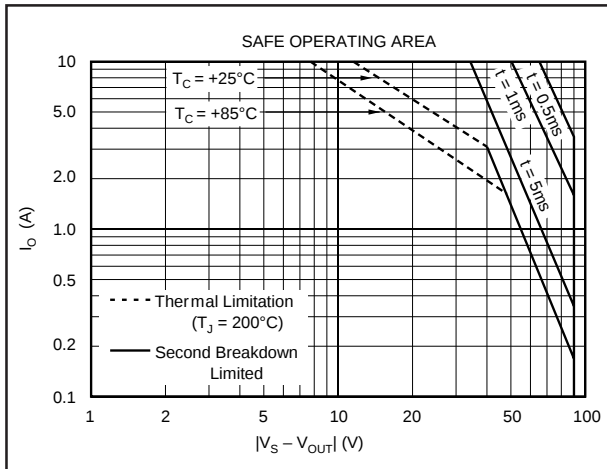


FIGURE 2. Safe Operating Area (SOA).

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA502 do not need to be equal. Figure 3 shows a circuit designed for a positive output voltage and current. The $-5V$ power supply voltage assures that the inputs of the OPA502 are operated within their linear common-mode range. The $V+$ power supply could range from 15V to 85V. The total voltage ($V-$ to $V+$) can range from 20V to 90V.

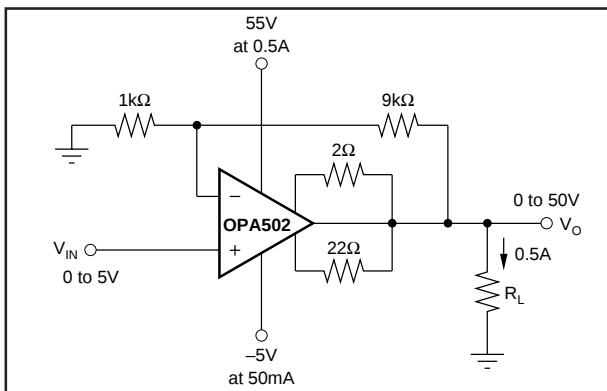


FIGURE 3. Unbalanced Power Supplies.

FOLDOVER CURRENT LIMIT

By connecting a resistor from pin 7 to ground, you can make the limit current vary with output voltage. The foldover limit

circuit can be set to allow high output current when V_{CE} is low (high output voltage). Output current limits at a lower value under the more stressful condition when V_{CE} is high, (output voltage is low).

The behavior of this voltage-dependant current limit is described by the following equation.

$$I_{LIMIT} = \frac{0.81 + \left(\frac{0.28 V_O}{R_{FO} + 20} \right)}{R_{CL}} + 0.03$$

where: V_O is the output voltage measured with respect to ground.

R_{FO} is the resistor connected from pin 7 to ground (in k ohms).

R_{CL} is the current limit resistor (in ohms).

The foldover limit circuitry can be set to allow large voltage and current to resistive loads, yet limit output current to a safe value with an output short circuit.

Reactive or EMF-generating loads can produce unexpected behavior with the foldover circuit driven into limiting. With a reactive load, peak output current occurs at low or zero output voltage. Compared to a resistive load, a reactive load with the same total impedance will be more likely to activate the foldover limit circuitry.

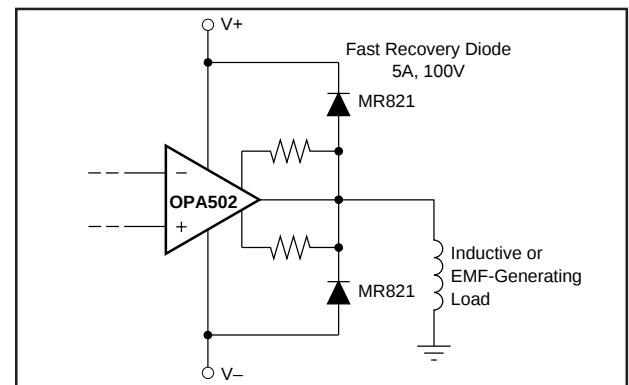


FIGURE 4. Diode Protection of Output.

OUTPUT PROTECTION

The output stage of the OPA502 is protected by internal diode clamps to the power supply terminals. These internal diodes are similar to common silicon rectifier types and may not be fast enough for adequate protection. For loads that can deliver large reverse kickback current (greater than 5A) to the output, external fast-recovery clamp diodes are recommended (Figure 4). For these diodes (internal or external) to provide the intended protection, the power supplies must provide a low impedance to a reverse current.

COMPENSATION AND STABILITY

Capacitance at the inverting input causes a high frequency pole in the feedback path. This reduces phase margin, causing pulse response ringing, and in severe cases, oscillations. A low value feedback capacitor can reduce or eliminate this effect by maintaining a constant feedback factor at high frequency (see Figure 5).

Depending on the load conditions, precautions may be required when using the OPA502 in low gains. Gains less than +3V/V or -2V/V may cause oscillations, particularly with capacitive loads. Figure 6 shows several circuits for low gain and capacitive loads.

Large value feedback capacitors used to limit the closed-loop bandwidth or form an integrator may also produce instability because the closed-loop gain approaches unity at high frequency.

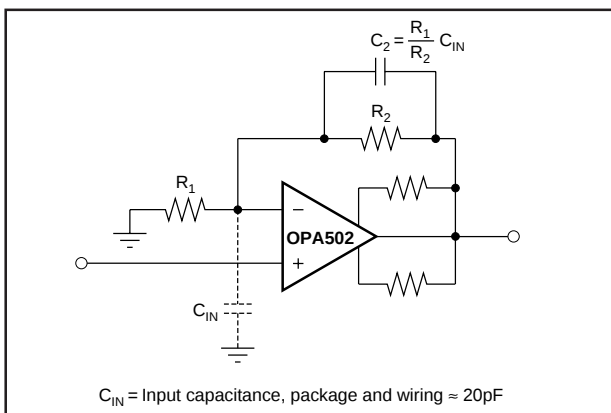


FIGURE 5. Compensating Input Capacitance.

MOUNTING AND HEAT SINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The case of the OPA502 is isolated from all circuitry and can be fastened directly to a heat sink. This eliminates cumbersome insulating hardware that degrades thermal performance. Consult Application Bulletin AB-037 for proper mounting techniques and procedures for TO-3 power products.

SOCKET

A mating socket, 0804MC is available for the OPA502 and can be purchased from Burr-Brown. Although not required, this socket makes interchanging parts easy, especially during design and testing.

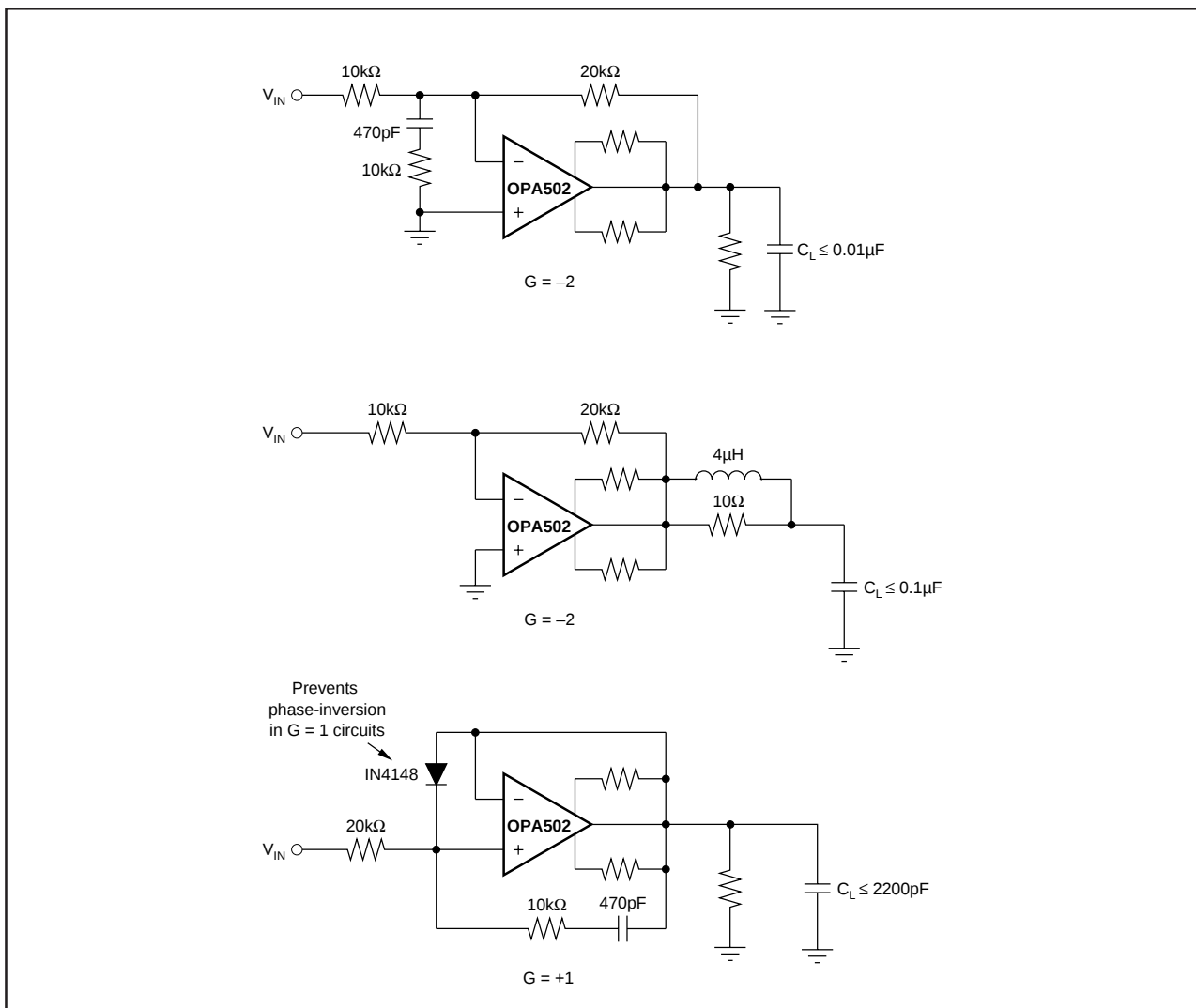


FIGURE 6. Compensation Circuits.

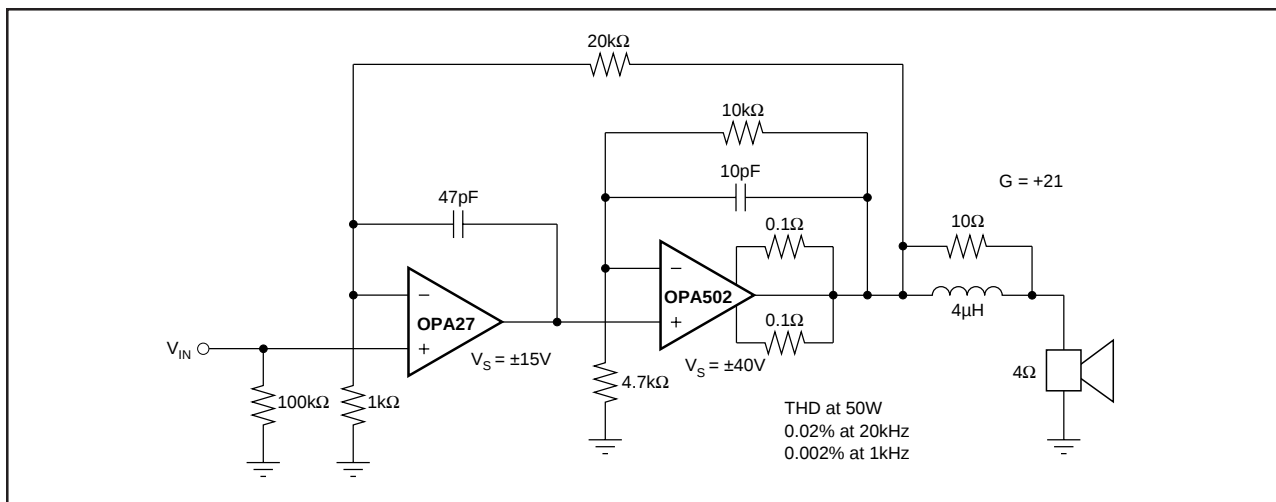


FIGURE 7. Low Distortion Composite Amplifier.

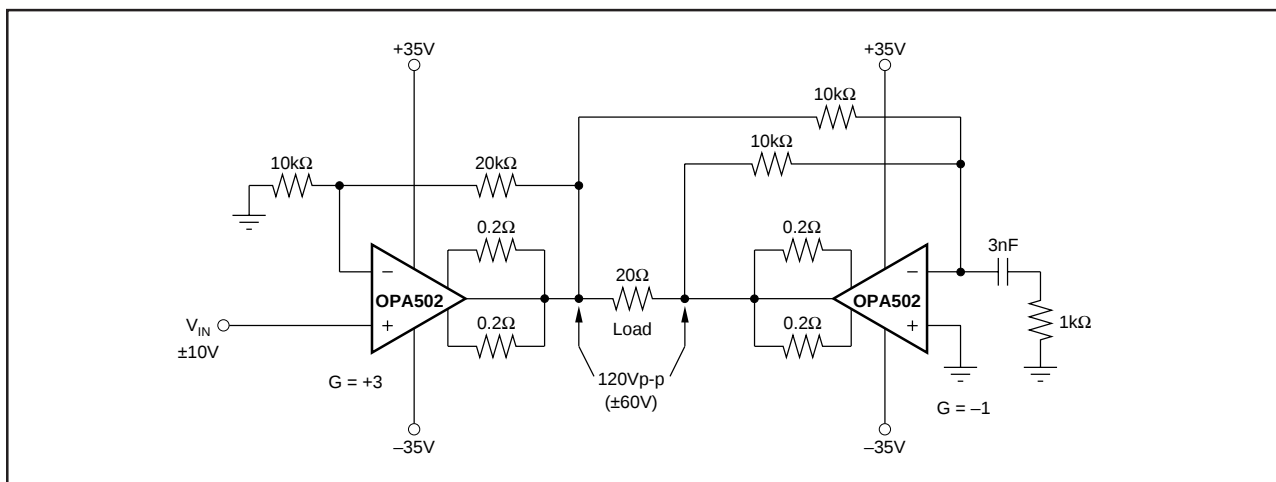


FIGURE 8. Bridge Drive Circuit.

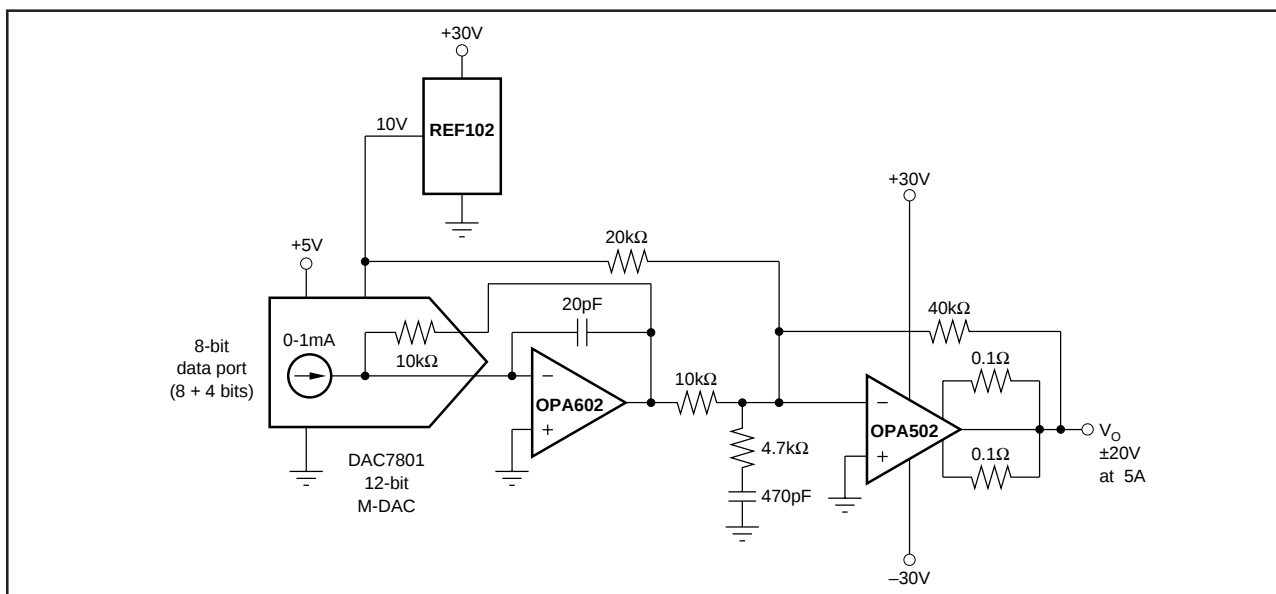


FIGURE 9. Digitally Programmable Power Supply.