

OPA671

Wide Bandwidth, Fast Settling *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN-BANDWIDTH: 35MHz
- LOW INPUT NOISE: $10\text{nV}/\sqrt{\text{Hz}}$
- HIGH SLEW RATE: $100\text{V}/\mu\text{s}$
- FAST SETTLING: 240ns to 0.01%
- FET INPUT: $I_b = 50\text{pA max}$
- HIGH OUTPUT CURRENT: 50mA
- WIDE SUPPLY RANGE: $V_s = \pm 4.5$ to $\pm 18\text{V}$

APPLICATIONS

- HIGH-SPEED DATA ACQUISITION
- OPTOELECTRONICS
- TRANSIMPEDANCE AMPLIFIER
- LINE DRIVER
- CCD BUFFER AMPLIFIER

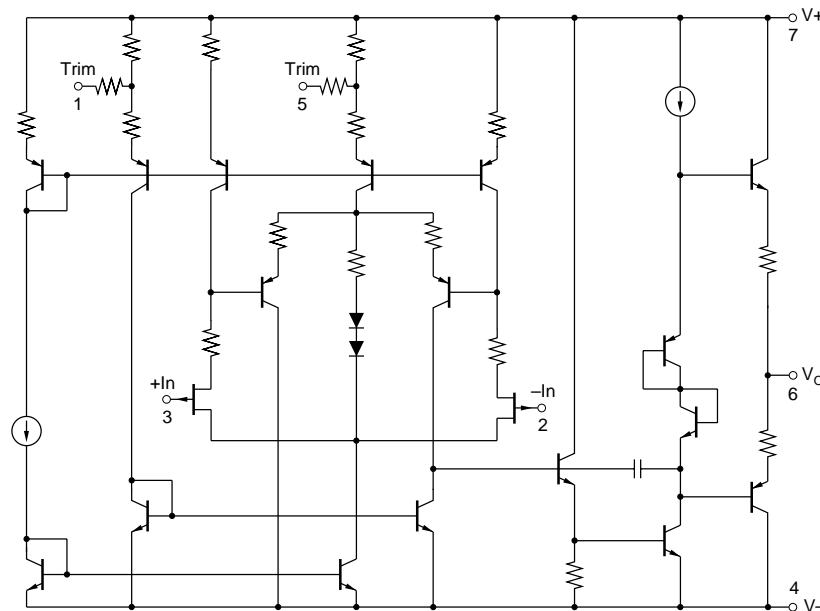
DESCRIPTION

The OPA671 is a FET-input monolithic operational amplifier featuring wide bandwidth and fast settling time. Fabricated using Burr-Brown's *Difet*, complementary bipolar process, it provides an excellent combination of high speed, accuracy, and high output current.

The OPA671 is versatile, operating from $\pm 4.5\text{V}$ to $\pm 18\text{V}$ power supplies. It can deliver $\pm 10\text{V}$ signals into a 200Ω load at slew rates of $100\text{V}/\mu\text{s}$. OPA671's *Difet* input provides input bias current thousands of times lower than bipolar-input wideband op amps.

The OPA671 is internally compensated to be unity-gain stable, allowing use in the widest range of applications.

The OPA671 is available in an 8-pin plastic DIP, rated for the industrial temperature range.



Difet[®] Burr-Brown Corporation

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SPECIFICATIONS

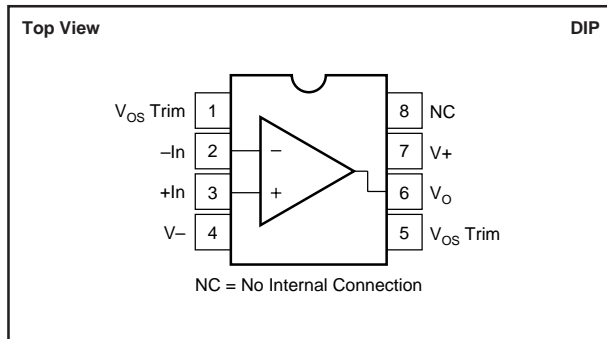
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

| PARAMETER | CONDITION | OPA671AP | | | UNITS |
|--|--|-------------------|--|----------------------|--|
| | | MIN | TYP | MAX | |
| OFFSET VOLTAGE Input Offset Voltage Average Drift Power Supply Rejection | $V_S = \pm 4.5$ to $\pm 16.5\text{V}$ | | ± 0.5 ± 10 94 | ± 5 | mV $\mu\text{V}/^\circ\text{C}$ dB |
| INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current | $V_{\text{CM}} = 0\text{V}$ $V_{\text{CM}} = 0\text{V}$ | | 5 2 | 50 | pA pA |
| NOISE Input Voltage Noise Noise Density, $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ $f = 100\text{kHz}$ Voltage Noise, $\text{BW} = 10\text{Hz}$ to 1MHz Input Bias Current Noise Current Noise Density, $f = 10\text{Hz}$ to 1MHz | | | 24 15 12 10 60 2 | | $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ $\text{fA}/\sqrt{\text{Hz}}$ |
| INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection | $V_{\text{CM}} = \pm 10\text{V}$ | ± 12 74 | ± 13 92 | | V dB |
| INPUT IMPEDANCE Differential Common-Mode | | | $10^{12} \parallel 4.5$ $10^{12} \parallel 6$ | | $\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$ |
| OPEN-LOOP GAIN Open-Loop Voltage Gain | $V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 200\Omega$ | 74 | 80 78 | | dB dB |
| FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% 0.1% 1% Total Harmonic Distortion | $G = -1$, 10V Step $G = -1$, 10V Step $G = -1$, 10V Step $G = -1$, 10V Step $G = 1$, $f = 100\text{kHz}$ $V_O = 3\text{V}$, $R_L = 200\Omega$ | | 35 107 240 150 85 0.0006 | | MHz V/ μs ns ns ns % |
| OUTPUT Voltage Output Current Output Short Circuit Current Output Resistance, Open-Loop | $R_L = 200\Omega$ $V_O = \pm 10\text{V}$ DC | ± 10.5 | ± 11.5 50 $-90/+105$ 20 | | V mA mA Ω |
| POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current | $V_S = \pm 15\text{V}$ | ± 4.5 | ± 15 ± 14.8 | ± 18 ± 17 | V V mA |
| TEMPERATURE RANGE Specification Operating Storage Thermal Resistance, θ_{JA} | Junction to Ambient | -25 -40 -40 | | +85 +100 +125 | $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ |

NOTE: (1) Tested without warm-up at $T_J = T_A = 25^\circ\text{C}$.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

| | |
|---|----------------------|
| Power Supply Voltage | ±18V |
| Input Voltage | (V+) +1V to (V-) -1V |
| Operating Temperature | -40°C to +100°C |
| Storage Temperature | -40°C to +125°C |
| Output Short-Circuit to Ground | 15s |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

ELECTROSTATIC DISCHARGE SENSITIVITY

An integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

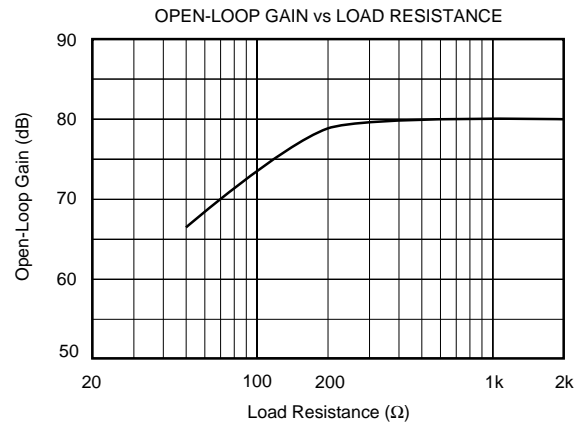
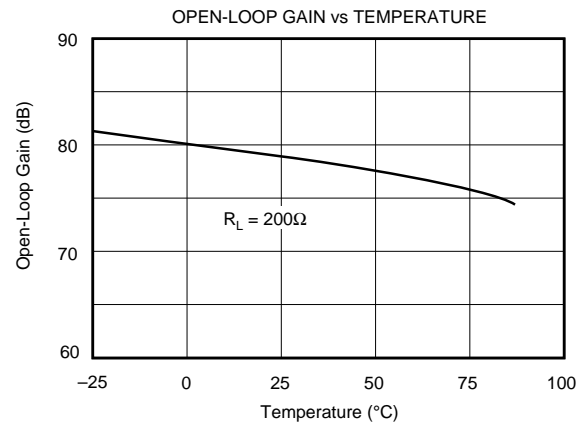
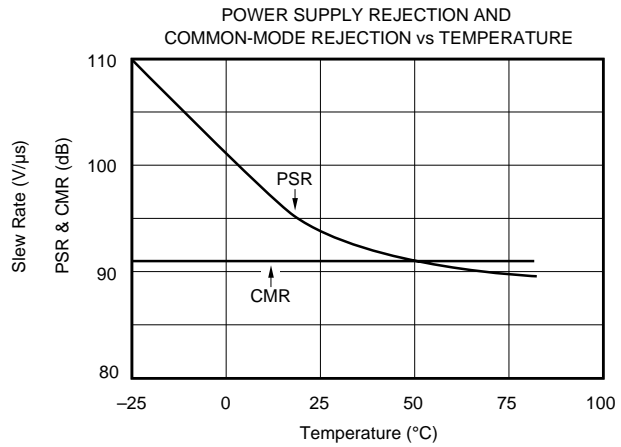
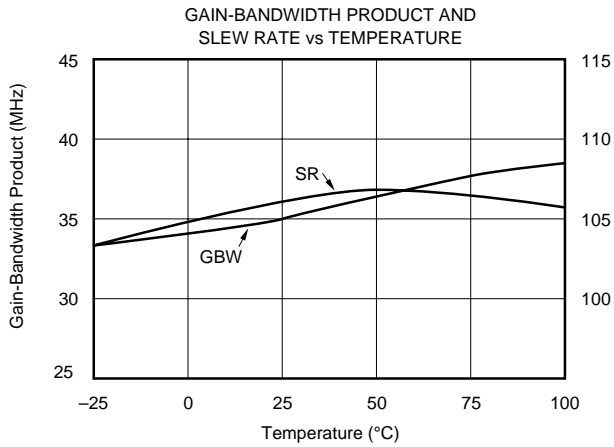
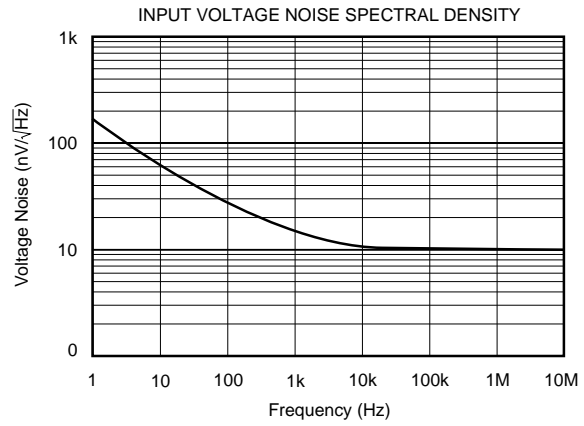
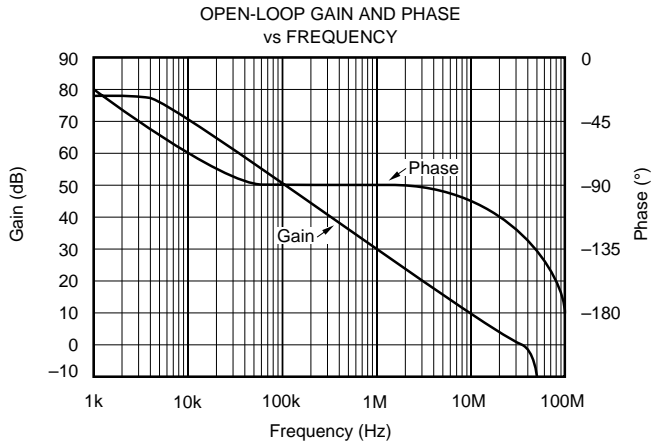
PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER ⁽¹⁾ | TEMPERATURE RANGE |
|----------|-------------------|---------------------------------------|-------------------|
| OPA671AP | 8-Pin Plastic DIP | 006 | -25°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

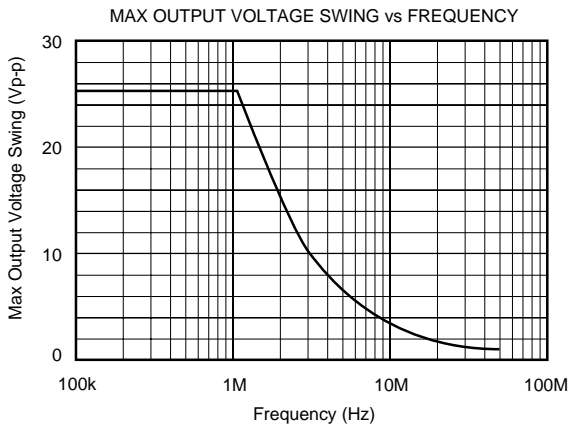
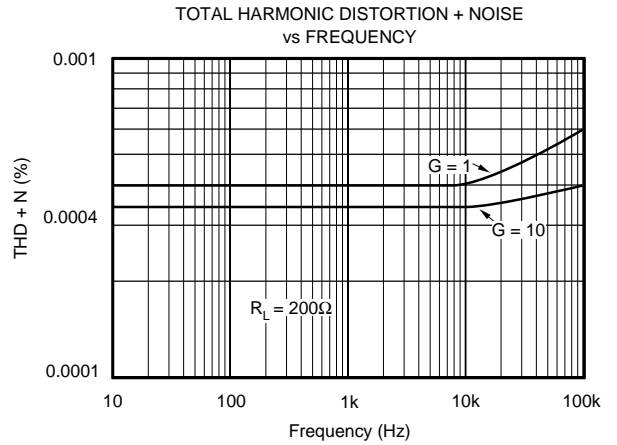
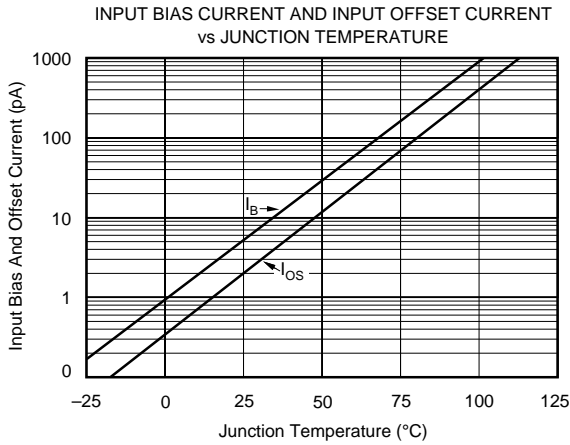
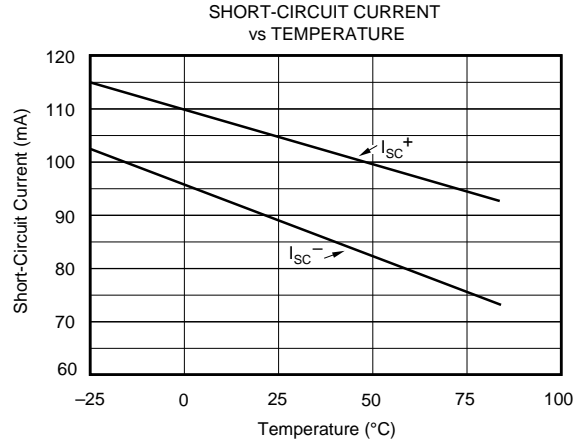
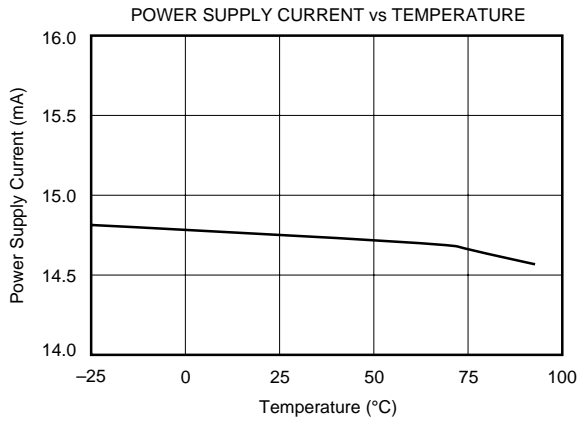
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

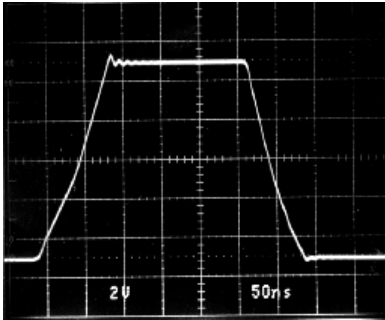
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



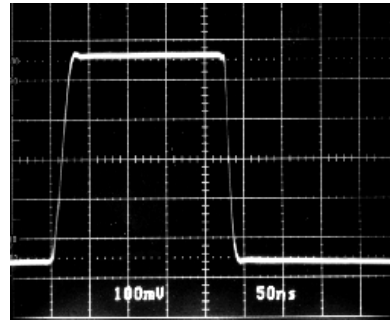
TYPICAL PERFORMANCE CURVES (CONT)

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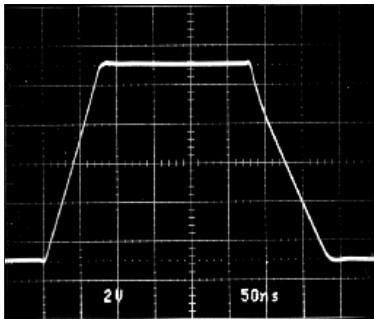
G = +1 LARGE SIGNAL RESPONSE



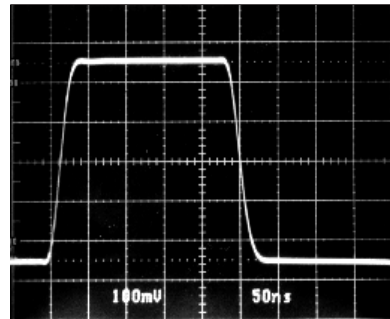
G = +1 SMALL SIGNAL RESPONSE



G = -1 LARGE SIGNAL RESPONSE



G = -1 SMALL SIGNAL RESPONSE



CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

The power supply connections should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, both a 1 μ F solid tantalum capacitor and a 0.1 μ F ceramic capacitor are required on each supply. The OPA671 can deliver peak load currents up to 100mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 4.7 μ F solid tantalum capacitors may improve dynamic performance in some applications.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1 shows an optional circuit for trimming the offset voltage. Do not use this offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage temperature drift.

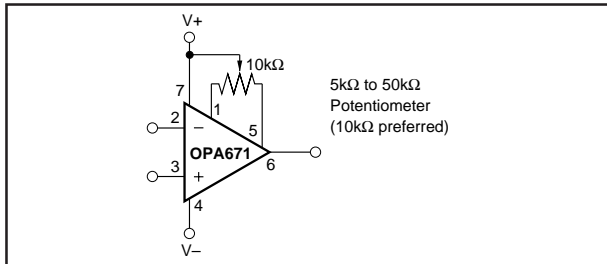


FIGURE 1. Optional Offset Voltage Trim Circuit.

CAPACITIVE LOADS

The OPA671 is internally compensated to be unity-gain stable with minimal capacitive load. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. With wideband op amps, load capacitance as low as 50pF can introduce enough phase shift to degrade dynamic performance. Figure 2 shows circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details on various compensation circuits and analysis techniques.

POWER DISSIPATION

High output current can cause large internal power dissipation in the OPA671. Copper leadframe construction improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces close to the device pins. Limit the ambient temperature, load and signal to

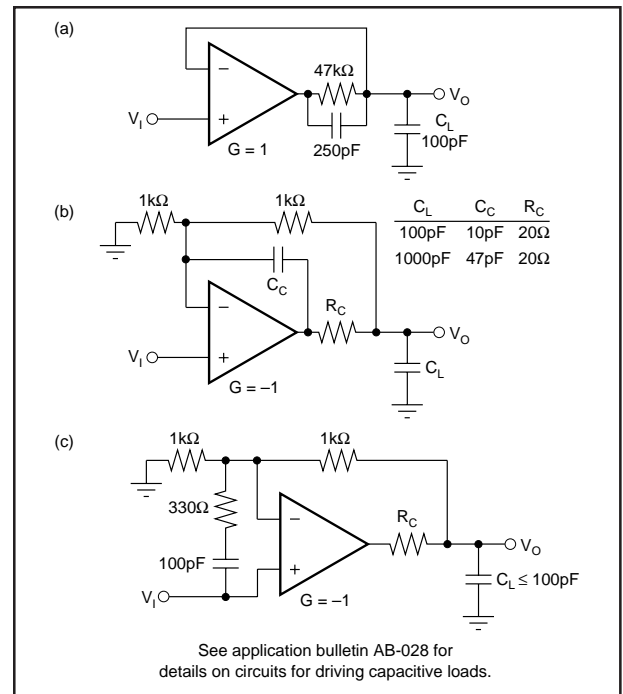


FIGURE 2. Compensation Circuits for Capacitive Loads.

assure that the maximum junction temperature is not exceeded. The OPA671 may be operated at reduced power supply voltage to minimize power dissipation.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 90mA at 25°C. The short-circuit limit current decreases with increasing junction temperature as shown in the typical curves. The current limit will protect the device from inadvertent short-circuits to ground. The internal power dissipation under this condition, however, is quite high so short-circuits should be avoided.

INPUT BIAS CURRENT

The OPA671 is fabricated with Burr-Brown's dielectrically isolated *Difet* process, giving it extremely low input bias current. As with other FET-input amplifiers, input bias current approximately doubles with every 10°C increase in junction temperature. Input bias current can be minimized by soldering the device to the circuit board to provided best heat dissipation. Reduced power supply voltage will also minimize input bias current by reducing internal power dissipation.

DEMONSTRATION BOARD

The OPA671 may be evaluated using a high frequency PC board developed for the OPA65x op amp family. This board may be ordered from your local Burr-Brown distribution as part # DEM-OPA65xP. It comes partially assembled but does not include the amplifier. Since this board was intended for \pm 5V amplifier, verify that any electrolytic capacitors loaded on the board can support the higher supply voltages possible with the OPA671.