ZXMP3A17DN8

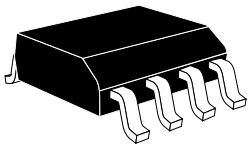
DUAL P-CHANNEL 30V ENHANCEMENT MODE MOSFET

SUMMARY

$V_{(BR)DSS}$ = -30V; $R_{DS(ON)}$ = 0.070Ω; I_D= -4.4A

DESCRIPTION

This new generation of TRENCH MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.



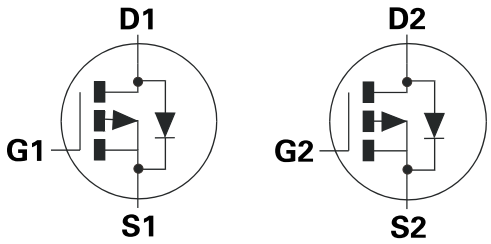
SO8

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- Low profile SOIC package

APPLICATIONS

- Motor Drive
- LCD backlighting



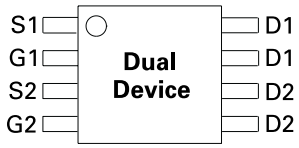
ORDERING INFORMATION

DEVICE	REEL	TAPE WIDTH	QUANTITY PER REEL
ZXMP3A17DN8TA	7''	12mm	500 units
ZXMP3A17DN8TC	13''	12mm	2500 units

DEVICE MARKING

ZXMP
3A17D

PINOUT



Top view

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DSS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current@V_{GS}=10V; T_A=25°C (b)(d) @V_{GS}=10V; T_A=70°C (b)(d) @V_{GS}=10V; T_A=25°C (a)(d)	I_D	-4.4 -3.6 -3.4	A A A
Pulsed Drain Current (c)	I_{DM}	-16.2	A
Continuous Source Current (Body Diode)(b)	I_S	-2.5	A
Pulsed Source Current (Body Diode)(c)	I_{SM}	-16.2	A
Power Dissipation at TA=25°C (a)(d) Linear Derating Factor	P_D	1.25 10	W mW/°C
Power Dissipation at TA=25°C (a)(e) Linear Derating Factor	P_D	1.8 14	W mW/°C
Power Dissipation at TA=25°C (b)(d) Linear Derating Factor	P_D	2.1 17	W mW/°C
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)(d)	$R_{\theta JA}$	100	°C/W
Junction to Ambient (b)(e)	$R_{\theta JA}$	70	°C/W
Junction to Ambient (b)(d)	$R_{\theta JA}$	60	°C/W

Notes

(a) For a dual device surface mounted on 25mm x 25mm FR4 PCB with coverage of single sided 1oz copper in still air conditions.

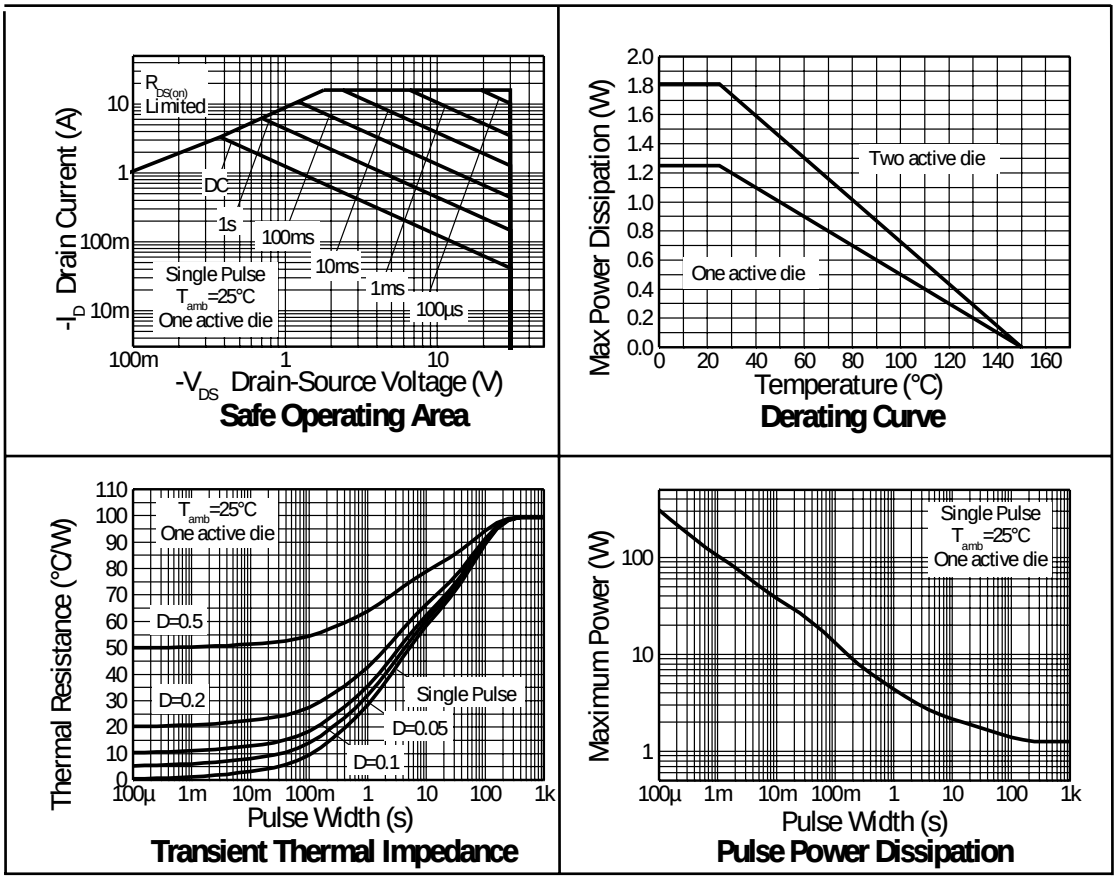
(b) For a dual device surface mounted on FR4 PCB measured at t ≤10 sec.

(c) Repetitive rating 25mm x 25mm FR4 PCB, D=0.05 pulse width=10µs - pulse width limited by maximum junction temperature.

(d) For a dual device with one active die.

(e) For dual device with 2 active die running at equal power.

CHARACTERISTICS



ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	-30			V	I_D=-250μA, V_{GS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			-1.0	μA	V_{DS}=-30V, V_{GS}=0V
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.0			V	I_D=-250μA, V_{DS}= V_{GS}
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.070 0.110	Ω Ω	V_{GS}=-10V, I_D=-3.2A V_{GS}=-4.5V, I_D=-2.5A
Forward Transconductance (1)(3)	g_{fs}		6.4		S	V_{DS}=-15V,I_D=-3.2A
DYNAMIC (3)						
Input Capacitance	C_{iss}		630		pF	V_{DS}=-15 V, V_{GS}=0V, f=1MHz
Output Capacitance	C_{oss}		113		pF	
Reverse Transfer Capacitance	C_{rss}		78		pF	
SWITCHING(2) (3)						
Turn-On Delay Time	$t_{d(on)}$		1.74		ns	V_{DD} =-15V, I_D=-1A R_G=6.0Ω, V_{GS}=-10V
Rise Time	t_r		2.87		ns	
Turn-Off Delay Time	$t_{d(off)}$		29.2		ns	
Fall Time	t_f		8.72		ns	
Gate Charge	Q_g		8.28		nC	V_{DS}=-15V,V_{GS}=-5V, I_D=-3.2A
Total Gate Charge	Q_g		15.8		nC	V_{DS}=-15V,V_{GS}=-10V, I_D=-3.2A
Gate-Source Charge	Q_{gs}		1.84		nC	
Gate-Drain Charge	Q_{gd}		2.80		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}		-0.85	-1.2	V	T_J=25°C, I_S=-2.5A, V_{GS}=0V
Reverse Recovery Time (3)	t_{rr}		19.5		ns	T_J=25°C, I_F=-1.7A, di/dt= 100A/μs
Reverse Recovery Charge (3)	Q_{rr}		16.3		nC	

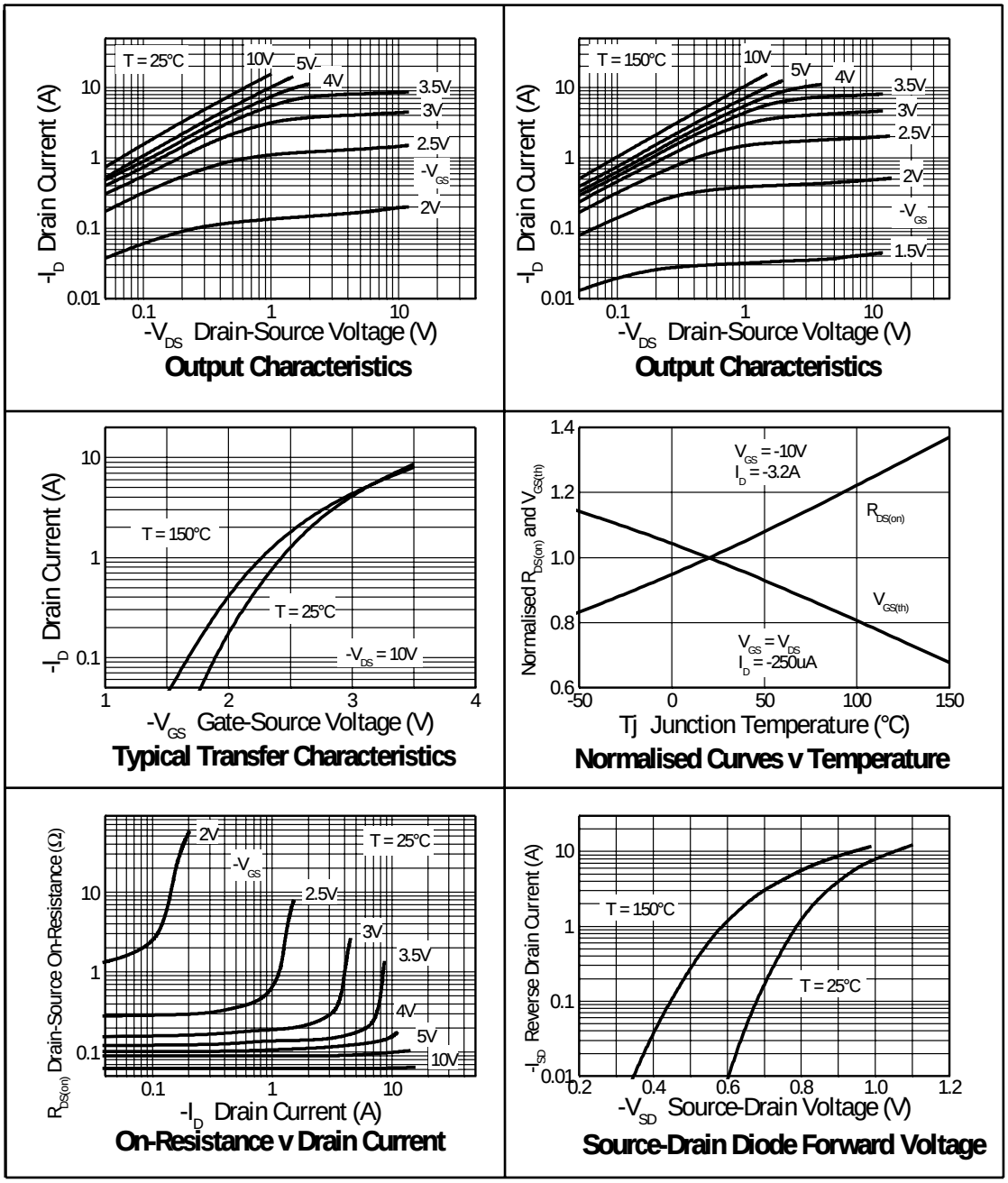
NOTES

(1) Measured under pulsed conditions. Width ≤300μs. Duty cycle ≤ 2% .

(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

TYPICAL CHARACTERISTICS



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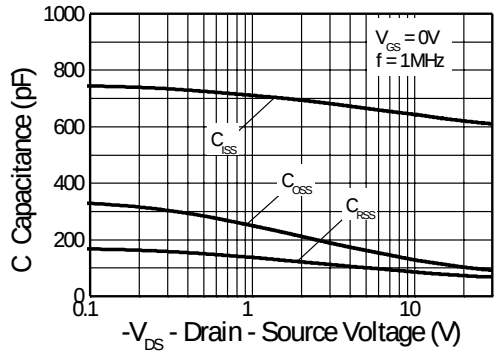
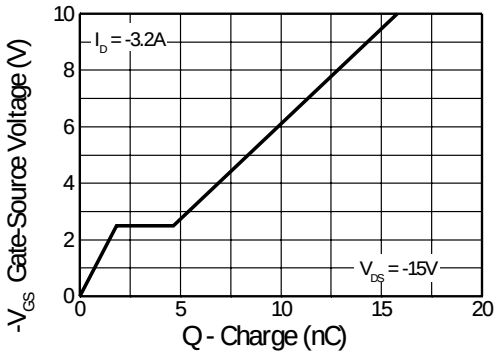
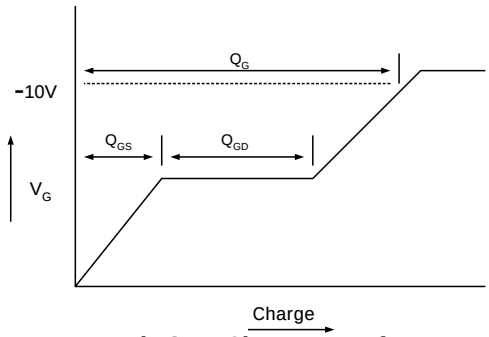


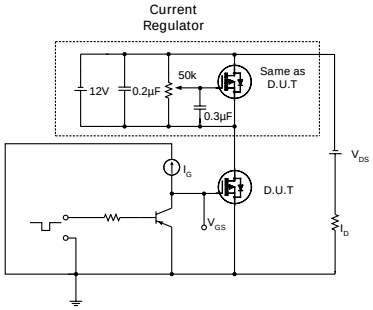
Capacitance v Drain-Source Voltage



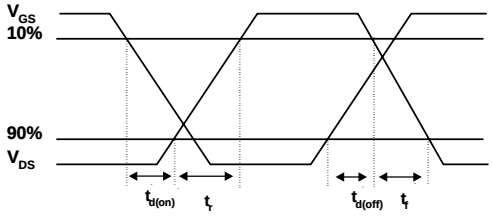
Gate-Source Voltage v Gate Charge



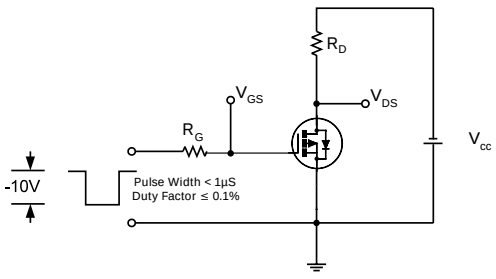
Basic Gate Charge Waveform



Gate Charge Test Circuit

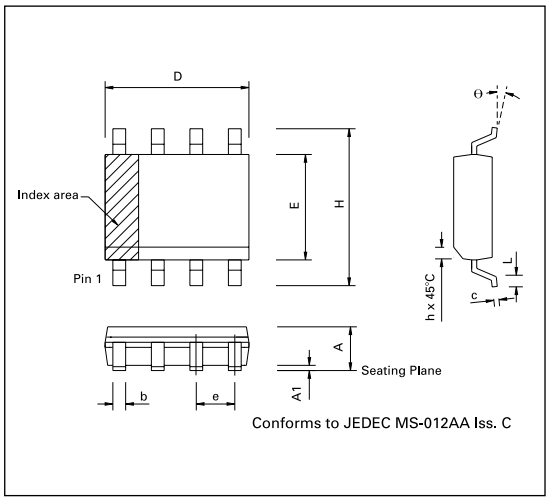


Switching Time Waveforms



Switching Time Test Circuit

PACKAGE OUTLINE



CONTROLLING DIMENSIONS ARE IN INCHES
APPROX IN MILLIMETRES

PACKAGE DIMENSIONS

DIM	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
D	0.189	0.197	4.80	5.00
H	0.228	0.244	5.80	6.20
E	0.150	0.157	3.80	4.00
L	0.016	0.050	0.40	1.27
e	0.050 BSC		1.27 BSC	
b	0.013	0.020	0.33	0.51
c	0.008	0.010	0.19	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50

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