8XC196NP COMMERCIAL CHMOS 16-BIT MICROCONTROLLER

- **25 MHz Operation at 4.5–5.5 Volts**
- **1 Mbyte of Linear Address Space**
- **Optional 4 Kbytes of ROM**
- **1000 Bytes of Register RAM**
- **Register-register Architecture**
- **32 I/O Port Pins**
- **16 Prioritized Interrupt Sources**
- **4 External Interrupt Pins and NMI Pin**
- **2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability**
- **3 Pulse-width Modulator (PWM) Outputs with High Drive Capability**
- **Full-duplex Serial Port with Dedicated Baud-rate Generator**
- **Peripheral Transaction Server**
- **Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels**
- **Chip-select Unit**
  - **— 6 Chip Select Pins**
  - **— Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select**
  - **— Programmable Wait States (0, 1, 2, or 3) for Each Chip Select**
  - **— Programmable Bus Width (8- or 16-bit) for Each Chip Select**
  - **— Programmable Address Range for Each Chip Select**
- **1.12 μs 16 × 16 Unsigned Multiplication**
- **1.92 μs 32/16 Unsigned Division**
- **100-pin SQFP or 100-pin QFP Package**
- **Complete System Development Support**
- **High-speed CHMOS Technology**

The 8XC196NP is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. When operating at 25 MHz in demultiplexed mode, the 8XC196NP can access a 100 ns memory device with zero wait states. The 8XC196NP is available without ROM (80C196NP) or with 4 Kbytes of ROM (83C196NP).

October 1995 **Order Number: 272459-005**

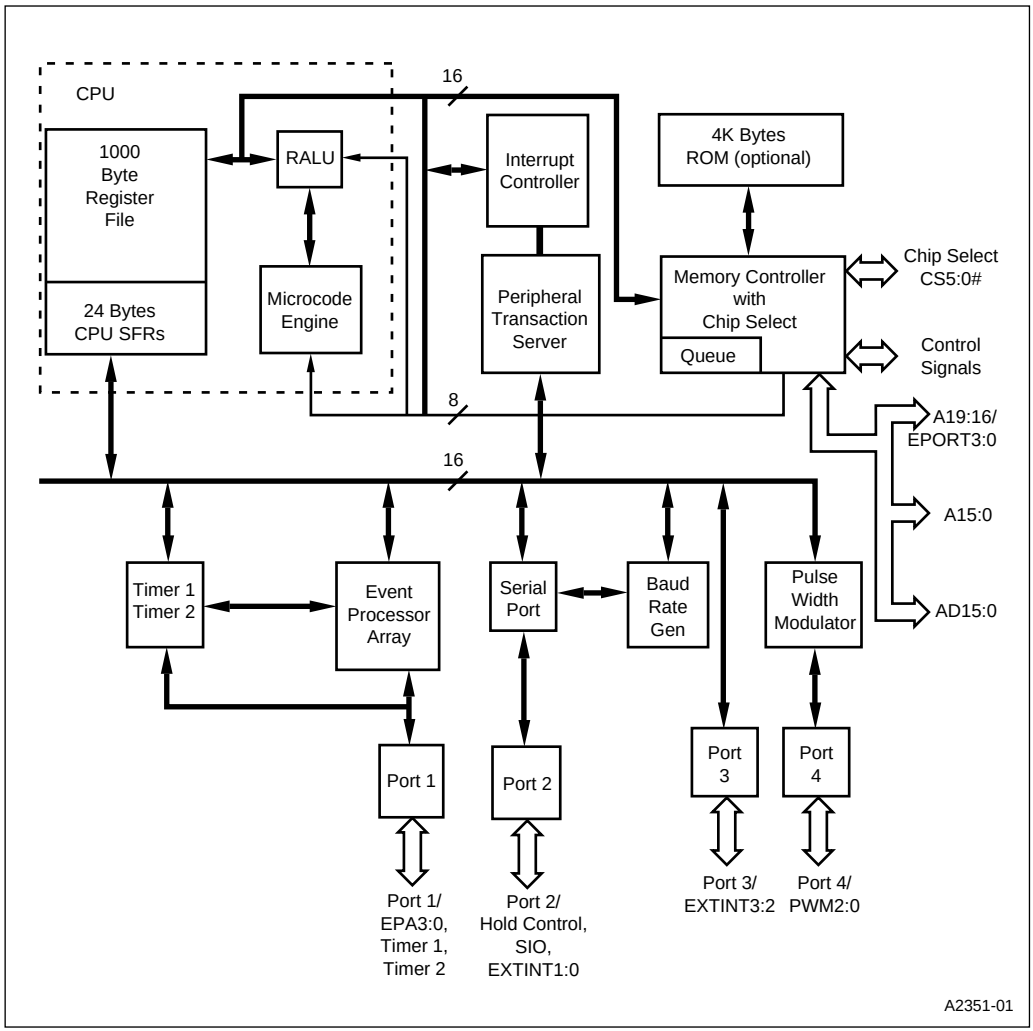


Figure 1. 8XC196NP Block Diagram

PROCESS INFORMATION

This device is manufactured on P648, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin SQFP	55°C/W	14°C/W
100-pin QFP	56°C/W	16°C/W

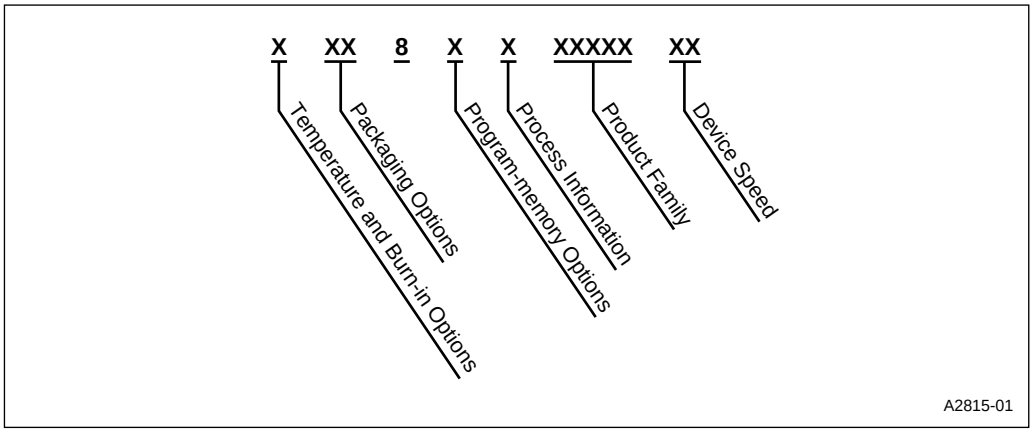


Figure 2. The 8XC196NP Family Nomenclature

Table 2. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	S SB	QFP SQFP
Program–memory Options	0 3	No ROM ROM
Process Information	C	CHMOS
Product Family	196NP	
Device Speed	no mark	25 MHz

Table 3. 8XC196NP Memory Map

Address (Note 1)	Description	Notes
FF FFFFH FF 3000H	External device (memory or I/O) connected to address/data bus	9
FF 2FFFH FF 2000H	Internal ROM or external device (memory or I/O) connected to address/data bus (determined by EA# pin)	2,9
FF 1FFFH FF 0000H	External device (memory or I/O) connected to address/data bus	3,9
FE FFFFH 0F 0000H	Overlaid memory (reserved for future devices)	3,9
0E FFFFH 01 0000H	896 Kbytes of external device (memory or I/O) connected to address/data bus	9
00 FFFFH 00 3000H	External device (memory or I/O) connected to address/data bus	9
00 2FFFH 00 2000H	External device (memory or I/O) connected to address/data bus or remapped internal ROM	5, 6,9
00 1FFFH 00 1FE0H	Memory-mapped peripheral special-function registers (SFRs)	4, 7,9
00 1FDFH 00 1F00H	Internal peripheral special-function registers (SFRs)	4, 7, 10
00 1EFFH 00 0400H	External device (memory or I/O) (reserved for future devices)	6
00 03FFH 00 0100H	Upper register file (general-purpose register RAM)	8, 10
00 00FFH 00 0018H	Lower register file (general-purpose register RAM and stack pointer)	8, 11
00 0017H 00 0000H	Lower register file (CPU SFRs)	4, 7, 8, 11

NOTES:
1. Internally, there are 24 address bits (A23:0); however, only 20 address lines (A19:0) are bonded out. The external address space is 1 Mbyte (00000–FFFFFH).
2. The 8XC196NP resets to internal address FF2080H (FF2080H in internal ROM or F2080H in external memory).
3. Do not locate code in addresses *x*F0000–*x*F00FFH. These addresses are reserved for the ICE in-circuit emulator. Unless otherwise noted, write 0FFH to reserved memory locations.
4. Unless otherwise noted, write 0 to reserved SFR bits.
5. These areas are mapped into internal ROM if the REMAP bit (CCB1.2) is set and EA# is at logic 1. Otherwise, they are mapped to external memory.
6. **WARNING**: The contents or functions of these memory locations may change with future device revisions, in which case a program that relies on one or more of these locations may not function properly.
7. Refer to the *8XC196NP User's Manual* or *8XC196NP Quick Reference* for SFR descriptions.
8. Code executed in locations 000000H to 0003FFH will be forced external.
9. Address with indirect, indexed, or extended modes.
10. Address with indirect, indexed, or extended modes or through register windows.
11. Address with direct, indirect, indexed, or extended modes.

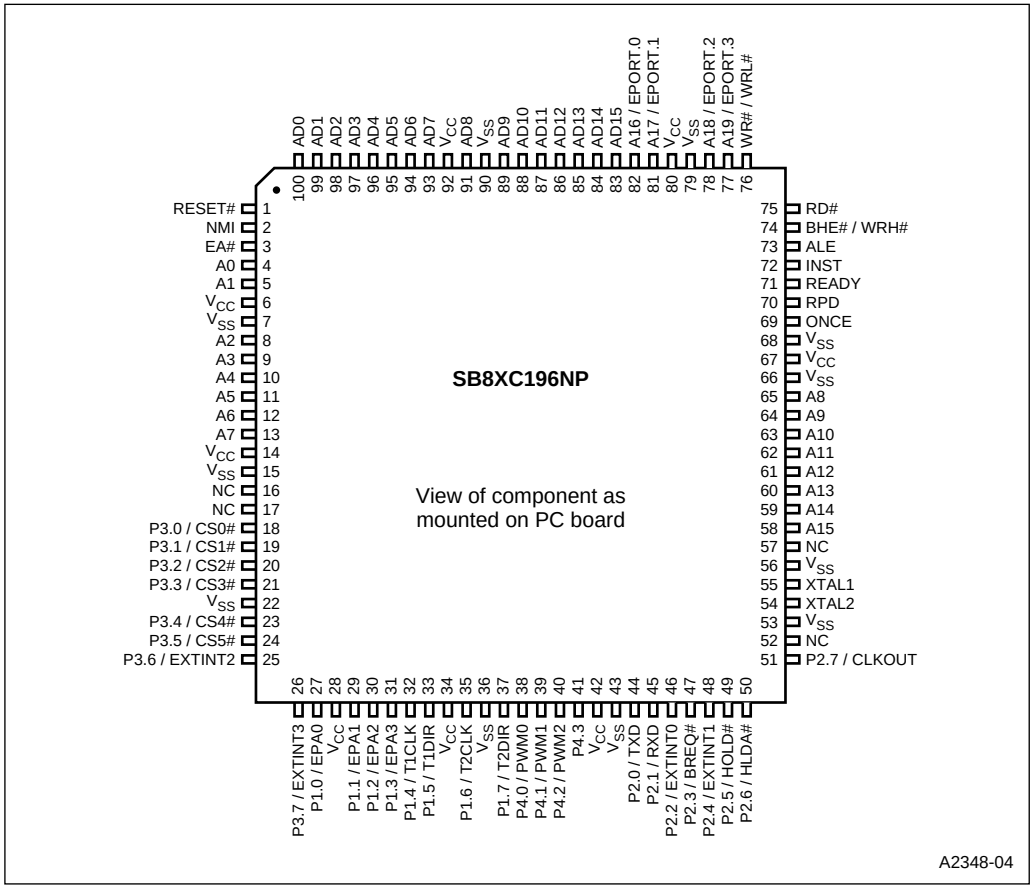


Figure 3. 8XC196NP 100-pin SQFP Package

Table 4. 8XC196NP 100-pin SQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	RESET#	26	EXTINT3/P3.7	51	CLKOUT/P2.7	76	WR#/WRL#
2	NMI	27	EPA0/P1.0	52	NC†	77	EPORT.3/A19
3	EA#	28	V_{CC}	53	V_{SS}	78	EPORT.2/A18
4	A0	29	EPA1/P1.1	54	XTAL2	79	V_{SS}
5	A1	30	EPA2/P1.2	55	XTAL1	80	V_{CC}
6	V_{CC}	31	EPA3/P1.3	56	V_{SS}	81	EPORT.1/A17
7	V_{SS}	32	T1CLK/P1.4	57	NC†	82	EPORT.0/A16
8	A2	33	T1DIR/P1.5	58	A15	83	AD15
9	A3	34	V_{CC}	59	A14	84	AD14
10	A4	35	T2CLK/P1.6	60	A13	85	AD13
11	A5	36	V_{SS}	61	A12	86	AD12
12	A6	37	T2DIR/P1.7	62	A11	87	AD11
13	A7	38	PWM0/P4.0	63	A10	88	AD10
14	V_{CC}	39	PWM1/P4.1	64	A9	89	AD9
15	V_{SS}	40	PWM2/P4.2	65	A8	90	V_{SS}
16	NC†	41	P4.3	66	V_{SS}	91	AD8
17	NC†	42	V_{CC}	67	V_{CC}	92	V_{CC}
18	CS0#/P3.0	43	V_{SS}	68	V_{SS}	93	AD7
19	CS1#/P3.1	44	TXD/P2.0	69	ONCE	94	AD6
20	CS2#/P3.2	45	RXD/P2.1	70	RPD	95	AD5
21	CS3#/P3.3	46	EXTINT0/P2.2	71	READY	96	AD4
22	V_{SS}	47	BREQ#/P2.3	72	INST	97	AD3
23	CS4#/P3.4	48	EXTINT1/P2.4	73	ALE	98	AD2
24	CS5#/P3.5	49	HOLD#/P2.5	74	BHE#/WRH#	99	AD1
25	EXTINT2/P3.6	50	HLDA#/P2.6	75	RD#	100	AD0

† To be compatible with future versions of the N*x* family, tie the no connection (NC) pins as follows: Pin 57 = V_{SS}, Pin 16 = V_{CC}, Pin 17 = V_{SS} (5 volts on this pin will enable a clock doubler on future devices), and Pin 52 = V_{CC}.

Table 5. 100-pin SQFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	4
A1	5
A2	8
A3	9
A4	10
A5	11
A6	12
A7	13
A8	65
A9	64
A10	63
A11	62
A12	61
A13	60
A14	59
A15	58
A16	82
A17	81
A18	78
A19	77
AD0	100
AD1	99
AD2	98
AD3	97
AD4	96
AD5	95
AD6	94
AD7	93
AD8	91
AD9	89
AD10	88
AD11	87
AD12	86

Address & Data (cont)	
Name	**Pin**
AD13	85
AD14	84
AD15	83

Bus Control & Status	
Name	**Pin**
ALE	73
BHE#/WRH#	74
BREQ#	47
HOLD#	49
HLDA#	50
INST	72
RD#	75
READY	71
WR#/WRL#	76

Processor Control	
Name	**Pin**
CLKOUT	51
EA#	3
EXTINT0	46
EXTINT1	48
EXTINT2	25
EXTINT3	26
NMI	2
ONCE	69
RESET#	1
RPD	70
XTAL1	55
XTAL2	54

Input/Output	
Name	**Pin**
CS0#/P3.0	18
CS1#/P3.1	19
CS2#/P3.2	20
CS3#/P3.3	21
CS4#/P3.4	23
CS5#/P3.5	24
EPA0/P1.0	27
EPA1/P1.1	29
EPA2/P1.2	30
EPA3/P1.3	31
EPORT.0	82
EPORT.1	81
EPORT.2	78
EPORT.3	77
P2.2	46
P2.3	47
P2.4	48
P2.5	49
P2.6	50
P2.7	51
P3.6	25
P3.7	26
P4.3	41
PWM0/P4.0	38
PWM1/P4.1	39
PWM2/P4.2	40
RXD/P2.1	45
T1CLK/P1.4	32
T1DIR/P1.5	33
T2CLK/P1.6	35
T2DIR/P1.7	37
TXD/P2.0	44

Power & Ground	
Name	**Pin**
V_{CC}	6
V_{CC}	14
V_{CC}	28
V_{CC}	34
V_{CC}	42
V_{CC}	67
V_{CC}	80
V_{CC}	92
V_{SS}	7
V_{SS}	15
V_{SS}	22
V_{SS}	36
V_{SS}	43
V_{SS}	53
V_{SS}	56
V_{SS}	66
V_{SS}	68
V_{SS}	79
V_{SS}	90

No Connection	
Name	**Pin**
NC	16
NC	17
NC	52
NC	57

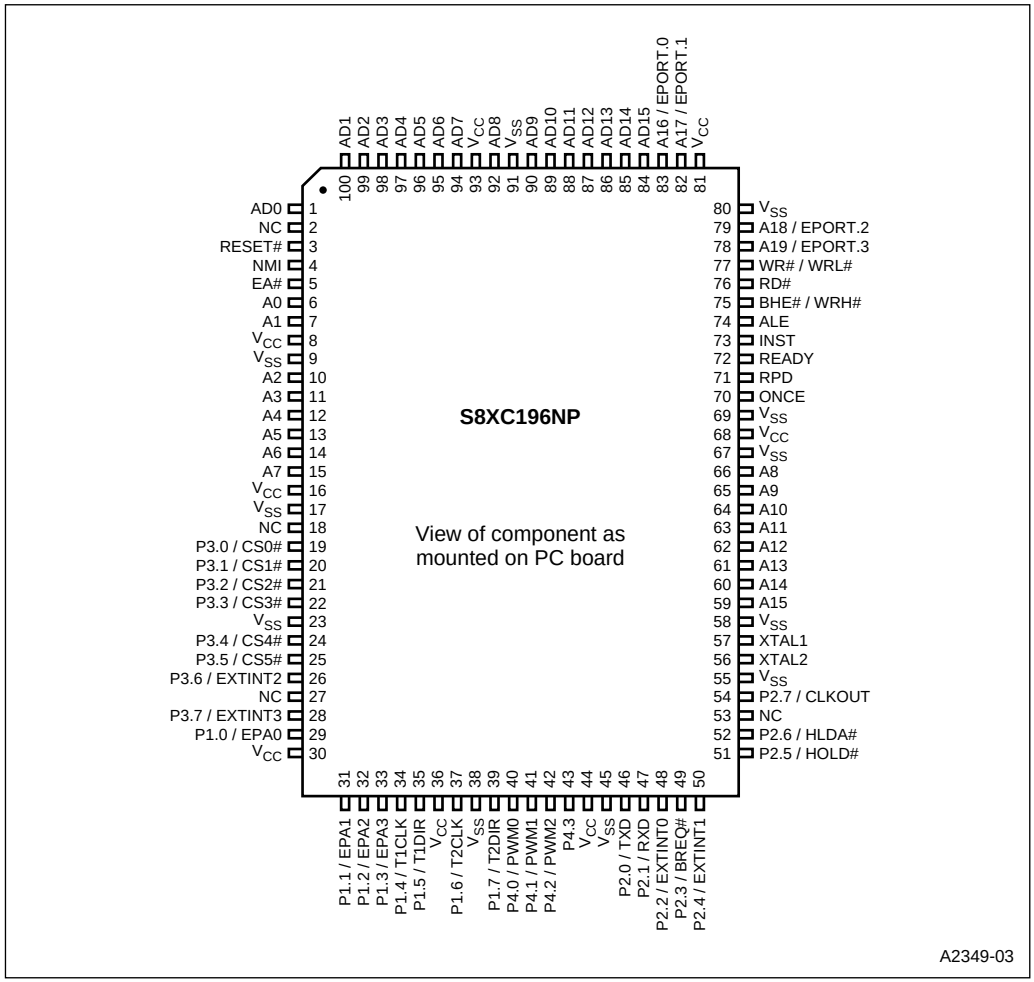


Figure 4. 8XC196NP 100-pin QFP Package

Table 6. 8XC196NP 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	No Connection	27	No Connection	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	No Connection	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	EA#	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	No Connection	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	V_{SS}	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

Table 7. 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88
AD12	87

Address & Data (cont)	
Name	**Pin**
AD13	86
AD14	85
AD15	84

Bus Control & Status	
Name	**Pin**
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	**Pin**
CLKOUT	54
EA#	5
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56

Input/Output	
Name	**Pin**
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	**Pin**
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	69
V_{SS}	80
V_{SS}	91

No Connection	
Name	**Pin**
NC	2
NC	18
NC	27
NC	53

PIN DESCRIPTIONS

Table 8. Pin Descriptions

Name	Type	Description	Multiplexed with
A15:0	I/O	System Address Bus These address lines provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.	—
A19:16	I/O	Address Lines 16–19 These address lines provide address bits 16–19 during the entire external memory cycle, supporting extended addressing of the 1-Mbyte address space. Internally, there are 24 address bits; however, only 20 address lines (A19:0) are bonded out. The external address space is 1 Mbyte (00000–FFFFFH) and the internal address space is 16 Mbytes (000000–FFFFFFH). The 8XC196NP resets to internal address FF2080H (FF2080H in internal ROM or F2080H in external memory).	EPORT.3:0
AD15:0	I/O	Address/Data Lines The function of these pins depends on the bus size and mode. **16-bit Multiplexed Bus Mode**: AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode**: AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode**: AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode**: AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus.	—
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). ALE differs from ADV# in that it does not remain active during the entire bus cycle. An external latch can use this signal to demultiplex the address bits 0–15 from the address/data bus in multiplexed mode.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
BHE#	O	Byte High Enable The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2=1 selects BHE#; CCR0.2=0 selects WRH#. During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with A0, to determine which memory byte is being transferred over the system bus: **BHE# A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only	WRH#
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. The device can assert BREQ# at the same time as or after it asserts HLDA#. Once it is asserted, BREQ# remains asserted until HOLD# is removed. You must enable the bus-hold protocol before using this signal.	P2.3
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (F_{XTAL1}). CLKOUT has a 50% duty cycle.	P2.7
CS5#:0	O	Chip-select Lines 0–5 The active-low output CS*x*# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select *x*. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values. Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH (F2000–F20FFH if external).	P3.5:0
EA#	I	External Access This input determines whether memory accesses to special-purpose and program memory partitions (FF2000–FF2FFFH) are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant. EA# is not latched and can be switched dynamically during normal operating mode. Be sure to thoroughly consider the issues, such as different access times for internal and external memory, before using this dynamic switching capability. On devices with no internal nonvolatile memory, always connect EA# to V_{SS}.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
EPA3:0	I/O	Event Processor Array (EPA) Input/Output pins These are the high-speed input/output pins for the EPA capture/compare channels. For high-speed PWM applications, the outputs of two EPA channels (either EPA0 and EPA1 or EPA2 and EPA3) can be remapped to produce a PWM waveform on a shared output pin.	P1.3:0
EPORT.3:0	I/O	Extended Addressing Port This is a 4-bit, bidirectional, memory-mapped I/O port. The pins are shared with the extended address bus A19:16.	A19:16
EXTINT0 EXTINT1 EXTINT2 EXTINT3	I	External Interrupts In normal operating mode, a rising edge on EXTINT*x* sets the EXTINT*x* interrupt pending bit. EXTINT*x* is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. In powerdown mode, asserting the EXTINT*x* signal for at least 1 state time causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINT*x* interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation.	P2.2 P2.4 P3.6 P3.7
HLDA#	O	Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#.	P2.6
HOLD#	I	Bus Hold Request An external device uses this active-low input signal to request control of the bus. This pin functions as HOLD# only if the pin is configured for its special function and the bus-hold protocol is enabled. Setting bit 7 of the window selection register enables the bus-hold protocol.	P2.5
INST	O	Instruction Fetch This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.	—
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
ONCE	I	On-circuit Emulation Holding ONCE high during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent accidental entry into ONCE mode, connect the ONCE pin to V_{SS}.	—
P1.3:0 P1.4 P1.5 P1.6 P1.7	I/O	Port 1 This is a standard, bidirectional port that is multiplexed with individually selectable special-function signals.	EPA3:0 T1CLK T1DIR T2CLK T2DIR
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	Port 2 This is a standard, bidirectional port that is multiplexed with individually selectable special-function signals.	TXD RXD EXTINT0 BREQ# EXTINT1 HOLD# HLDA# CLKOUT
P3.5:0 P3.6 P3.7	I/O	Port 3 This is an 8-bit, bidirectional, standard I/O port.	CS5:0# EXTINT2 EXTINT3
P4.2:0 P4.3	I/O	Port 4 This is a 4-bit, bidirectional, standard I/O port with high-current drive capability.	PWM2:0
PWM2:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable.	P4.2:0
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads.	—
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers, Register 0, or the chip-select *x* bus control register. READY is ignored for all internal memory accesses.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. After a device reset, the first instruction fetch is from FF2080H (or F2080H in external memory). For the 80C196NP, the program and special-purpose memory locations (FF2000–FF2FFFH) reside in external memory. For the 83C196NP, these locations can reside either in external memory or in internal ROM.	—
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if the internal oscillator is the clock source. The capacitor causes a delay that enables the oscillator to stabilize before the internal CPU and peripheral clocks are enabled. The capacitor is not required if your application uses powerdown mode and if an external clock input is the clock source. If your application does not use powerdown mode, leave this pin unconnected.	—
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data.	P2.1
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. and External clock for the serial I/O baud-rate generator input (program selectable).	P1.4
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. Also used in conjunction with T2DIR for quadrature counting mode.	P1.6
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode.	P1.5
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. Also used in conjunction with T2CLK for quadrature counting mode.	P1.7

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD is used to transmit serial port data. In mode 0, it is used as the serial clock output.	P2.0
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.	—
V_{SS}	GND	Digital Circuit Ground Connect each V_{SS} pin to ground through the lowest possible impedance path.	—
WR#	O	Write This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2=1 selects WR#; CCR0.2=0 selects WRL#.	WRL#
WRH#	O	Write High During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2=1 selects BHE#; CCR0.2=0 selects WRH#.	BHE#
WRL#	O	Write Low During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations. The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2=1 selects WR#; CCR0.2=0 selects WRL#.	WR#
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.	—
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.	—

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... –60°C to +150°C
Supply Voltage with Respect to V_{SS} ..... –0.5 V to +7.0 V
Power Dissipation ..... 1.5 W

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
F_{XTAL1} (Input frequency for V_{CC} = 4.5–5.5 V)
(Note 1) ..... 8 MHz to 25 MHz

NOTES:

1. This device is static and should operate below 1 Hz, but has been tested only down to 8 MHz.

NOTICE: This document contains information on products in the design phase of development. The specifications are subject to change without notice. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC Characteristics

Table 9. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		80	120	mA	XTAL1 = 25 MHz V_{CC} = 5.5 V Device in Reset
I_{IDLE}	Idle Mode Current		24	36	mA	XTAL1 = 25 MHz V_{CC} = 5.5 V
I_{PD}	Powerdown Mode Current (Note 2)		50	75	µA	V_{CC} = 5.5 V
I_{LI}	Input Leakage Current (all input pins except RESET)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	–0.5		0.8	V	
V_{IH}	Input High Voltage	0.2 V_{CC} +1		V_{CC} + 0.5	V	
V_{IL1}	Input Low Voltage XTAL1	–0.5		0.3 V_{CC}	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (output configured as complementary) (Note 3,6)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 6)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
V_{OL1}	Output Low Voltage on P4.*x* (output configured as complementary)			0.45 0.6	V V	I_{OL} = 10 mA I_{OL} = 15 mA

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
5. Pin capacitance is not tested. C_S is based on design simulations.
6. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL}(mA)	I_{OH}(mA)
P1	42	42
P2	42	42
P3	42	42
P4	45	21
EPORT	21	21
Individual		
P1, P2, P3	10	10
P4	18	10

Table 9. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Note 1) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OL2}	Output Low Voltage in RESET on ALE, INST, and NMI			0.45	V	I_{OL} = 3 µA
V_{OH1}	Output High Voltage in RESET (Note 4)	V_{CC} – 0.7			V	I_{OH} = –3 µA
V_{OL3}	Output Low Voltage in RESET for ONCE pin			0.45	V	I_{OL} = 30 µA
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45 1.5	V V V	I_{OL} = 100 µA I_{OL} = 700 µA I_{OL} = 3 mA
V_{OH2}	Output High Voltage on XTAL2	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –100 µA I_{OH} = –700 µA I_{OH} = –3 mA
V_{TH+} – $V_{TH–}$	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 5)			10	pF	
R_{RST}	RESET Pull-up Resistor	9		95	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0 V

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
5. Pin capacitance is not tested. C_S is based on design simulations.
6. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	**I_{OL}**(mA)	**I_{OH}**(mA)
P1	42	42
P2	42	42
P3	42	42
P4	45	21
EPORT	21	21
Individual		
P1, P2, P3	10	10
P4	18	10

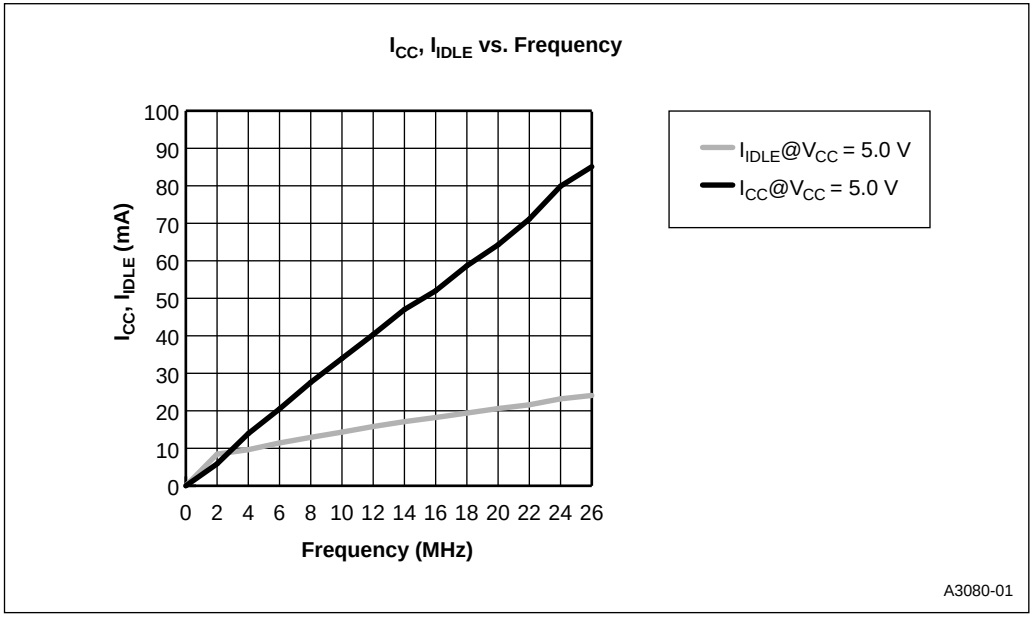


Figure 5. I_{CC}, I_{IDLE} versus Frequency

AC Characteristics — Multiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 10. AC Characteristics, Multiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications				
F_{XTAL1}	Input frequency on XTAL1	8	25	MHz
T_{XTAL1}	Period, $1/F_{XTAL1}$	40	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High/Low	10	110	ns
T_{CLCL}	CLKOUT Cycle Time	$2T_{XTAL1}$		ns
T_{CHCL}	CLKOUT High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVRL}	AD15:0 Valid to RD# Low	$2T_{XTAL1} - 20$		ns
T_{AVWL}	AD15:0 Valid to WR# Low	$2T_{XTAL1} - 10$		ns
T_{WHSH}	A19:16, CS*x*# Hold after WR# Rising Edge	0		
T_{RHSH}	A19:16, CS*x*# Hold after RD# Rising Edge	0		
T_{CLLH}	CLKOUT Low to ALE High	–10	10	ns
T_{LLCH}	ALE Low to CLKOUT High	–15	10	ns
T_{LHLH}	ALE Cycle Time	$4T_{XTAL1}$		ns (2)
T_{LHLL}	ALE High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVLL}	AD15:0 Valid to ALE Low	T_{XTAL1} –15		ns
T_{LLAX}	AD15:0 Hold after ALE Low	$T_{XTAL1} - 25$		ns
T_{LLRL}	ALE Low to RD# Low	$T_{XTAL1} - 15$		ns
T_{RLCL}	RD# Low to CLKOUT Low	0	20	ns
T_{RLRH}	RD# Low Period	T_{XTAL1}		ns (2)
T_{RHLH}	RD# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 15$	ns (3)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Low to WR# Low	$T_{XTAL1} - 15$		ns
T_{CLWL}	CLKOUT Low to WR# Low	–15	10	ns
T_{QVWH}	Data Valid before WR# High	$T_{XTAL1} - 15$		ns (2)
T_{CHWH}	CLKOUT High to WR# High	–10	10	ns
T_{WLWH}	WR# Low Period	$T_{XTAL1} - 5$		ns (2)

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

Table 10. AC Characteristics, Multiplexed Bus Mode (Continued)

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications				
T_{WHQX}	Data Hold after WR# High	T_{XTAL1} – 20		ns
T_{WHLH}	WR# High to ALE High	T_{XTAL1} – 12	T_{XTAL1} + 20	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# High	T_{XTAL1} – 10		ns
T_{WHAX}	AD15:8 Hold after WR# High	T_{XTAL1} – 10		ns (4)
T_{RHBX}	BHE#, INST Hold after RD# High	T_{XTAL1} – 10		ns
T_{RHAX}	AD15:8 Hold after RD# High	T_{XTAL1} – 10		ns (4)

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

Table 11. AC Characteristics, Multiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
The External Memory System Must Meet These Specifications				
T_{AVYV}	AD15:0 Valid to READY Setup		$2T_{XTAL1}$ – 50	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{XTAL1} – 10	ns (1)
T_{AVDV}	AD15:0 Valid to Input Data Valid		$3T_{XTAL1}$ – 40	ns (2)
T_{RLDV}	RD# Active to Input Data Valid		T_{XTAL1} – 20	ns (2)
T_{SLDV}	Chip-select Low, A19:16 Valid to Data Valid		$4T_{XTAL1}$ – 50	
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{XTAL1} – 35	ns
T_{RHDZ}	End of RD# to Input Data Float		T_{XTAL1} – 5	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.

SYSTEM BUS TIMINGS, MULTIPLEXED BUS

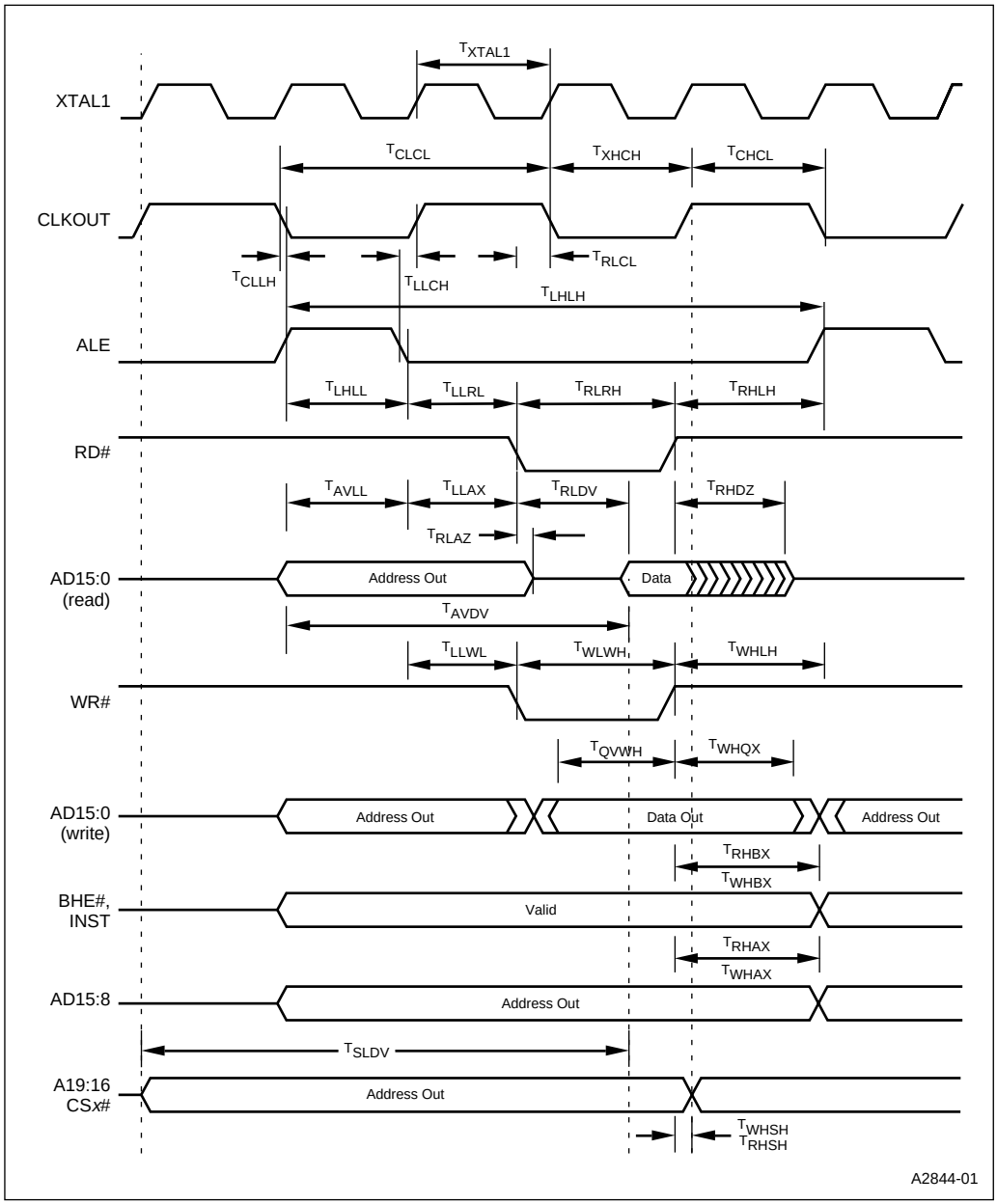


Figure 6. System Bus Timing Diagram (Multiplexed Bus Mode)

READY TIMING, MULTIPLEXED BUS

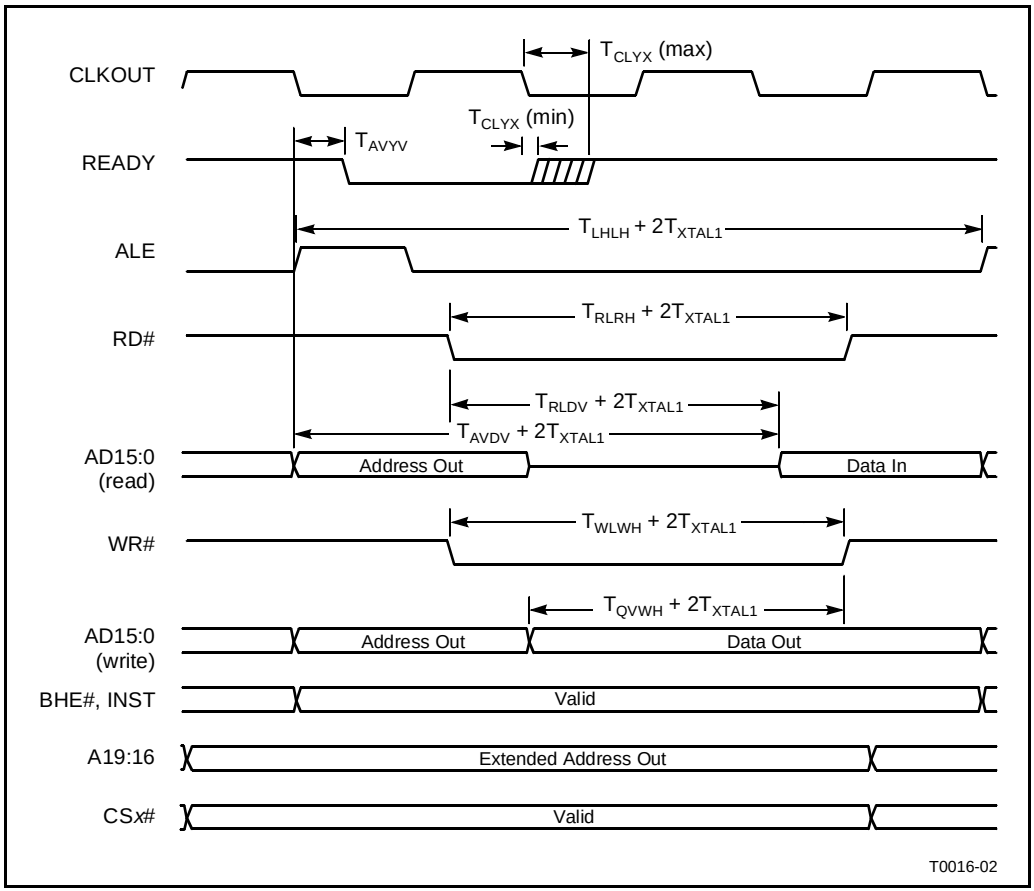


Figure 7. READY Timing Diagram (Multiplexed Bus Mode)

AC Characteristics — Demultiplexed Bus Mode

Test Coditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 12. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications				
F_{XTAL1}	Input frequency on XTAL1	8	25	MHz
T_{XTAL1}	Period, $1/F_{XTAL1}$	40	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High/Low	10	110	ns
T_{CLCL}	CLKOUT Cycle Time	$2T_{XTAL1}$		ns
T_{CHCL}	CLKOUT High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVRL}	A19:0, CS*x*# Valid to RD# Low	$2T_{XTAL1} - 30$		ns
T_{AVWL}	A19:0, CS*x*# Valid to WR# Low	$2T_{XTAL1} - 25$		ns
T_{CLLH}	CLKOUT Low to ALE High	– 10	10	ns
T_{LLCH}	ALE Low to CLKOUT High	– 15	10	ns
T_{LHLH}	ALE Cycle Time	$4T_{XTAL1}$		ns (2)
T_{LHLL}	ALE High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVLL}	Address Valid to ALE Low	NA		ns
T_{LLAX}	Address Hold after ALE Low	NA		ns
T_{LLRL}	ALE Low to RD# Low	NA		ns
T_{RLCH}	RD# Low to CLKOUT High	0	15	ns
T_{RLRH}	RD# Low Period	$2T_{XTAL1} - 10$		ns (2)
T_{RHLH}	RD# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 20$	ns (3)
T_{RLAZ}	RD# Low to Address Float		NA	ns
T_{LLWL}	ALE Low to WR# Low	NA		ns
T_{WLCH}	WR# Low to CLKOUT High	– 5	10	ns
T_{QVWH}	Data Valid before WR# High	$3T_{XTAL1} - 37$		ns (2)
T_{CHWH}	CLKOUT High to WR# High	– 15	5	ns
T_{WLWH}	WR# Low Period	$2T_{XTAL1} - 10$		ns (2)
T_{WHQX}	Data Hold after WR# High	$T_{XTAL1} - 20$		ns
T_{WHLH}	WR# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 20$	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{XTAL1} - 10$		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.

Table 12. AC Characteristics, Demultiplexed Bus Mode (Continued)

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications				
T_{WHAX}	A19:0, CS*x*# Hold after WR# High	0		ns
T_{RHBX}	BHE#, INST Hold after RD# High	T_{XTAL1} – 10		ns
T_{RHAX}	A19:0, CS*x*# Hold after RD# High	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.

Table 13. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
The External Memory System Must Meet These Specifications				
T_{AVYV}	A19:0, CS*x*# Valid to READY Setup		$3T_{XTAL1}$ – 60	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{XTAL1} – 10	ns (1)
T_{AVDV}	A19:0, CS*x*# Valid to Input Data Valid		$4T_{XTAL1}$ – 50	ns (2)
T_{RLDV}	RD# Active to Input Data Valid		$2T_{XTAL1}$ – 25	ns (2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{XTAL1} – 35	ns
T_{RHDZ}	End of RD# to Input Data Float		T_{XTAL1} – 5	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.

SYSTEM BUS TIMINGS, DEMULTIPLEXED BUS

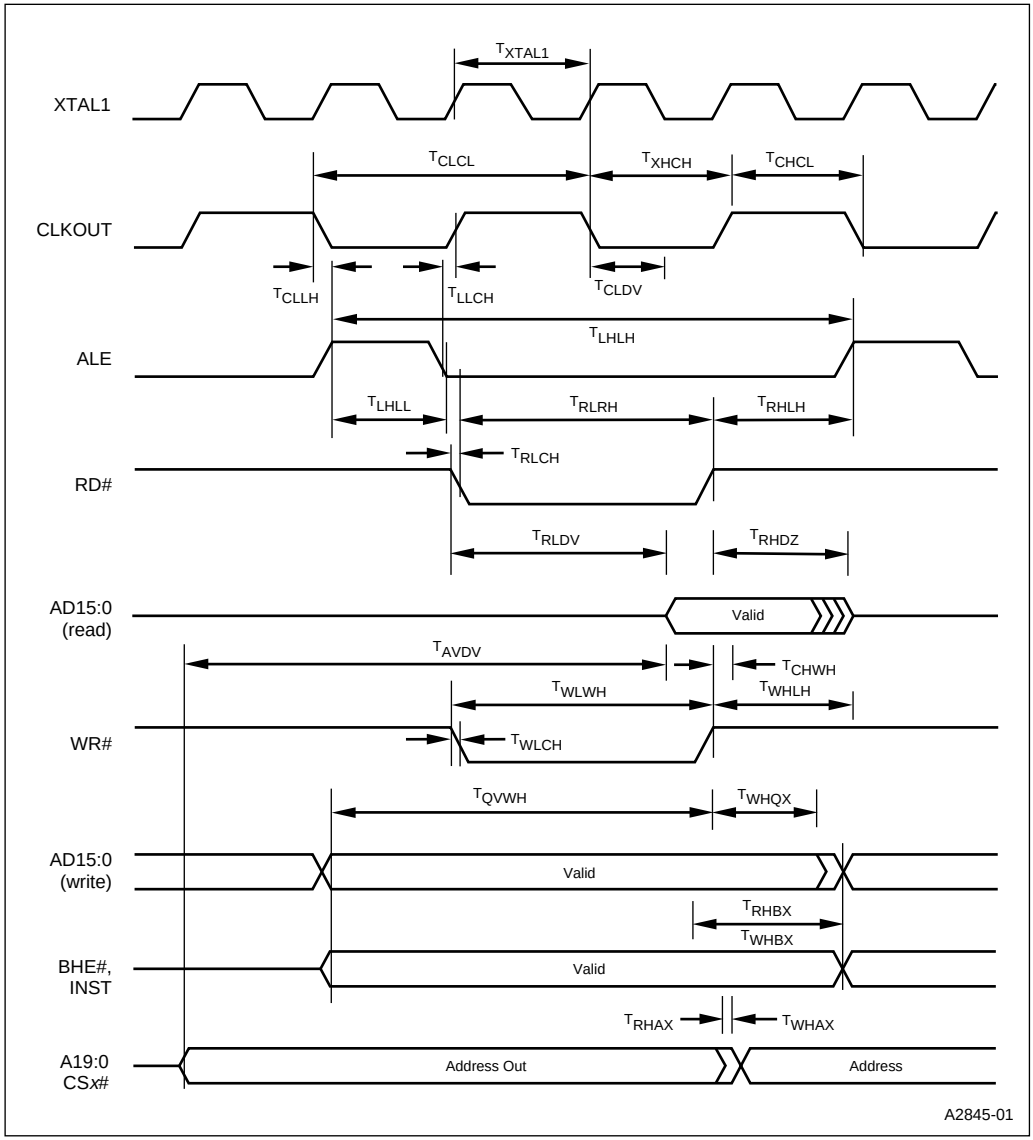


Figure 8. System Bus Timing Diagram (Demultiplexed Bus Mode)

READY TIMING, DEMULTIPLEXED BUS

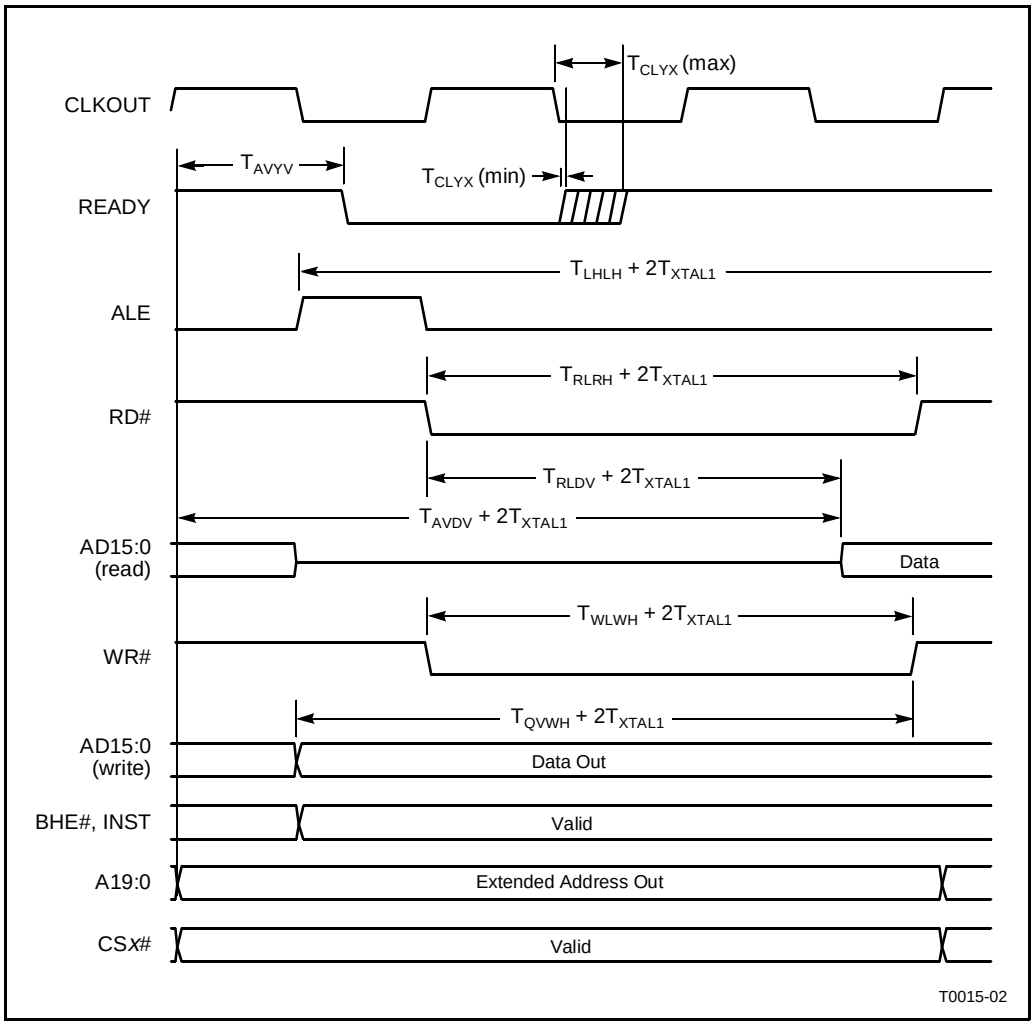


Figure 9. READY Timing Diagram (Demultiplexed Bus Mode)

HOLD#/HLDA# Timing

Table 14. HOLD#/HLDA# Timings

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
T_{HVCH}	HOLD# Setup Time	65		ns (1)
T_{CLHAL}	CLKOUT Low to HLDA# Low	–15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	–15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	–25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	–25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	–20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	–20		ns

NOTE:
1. To guarantee recognition at next clock.

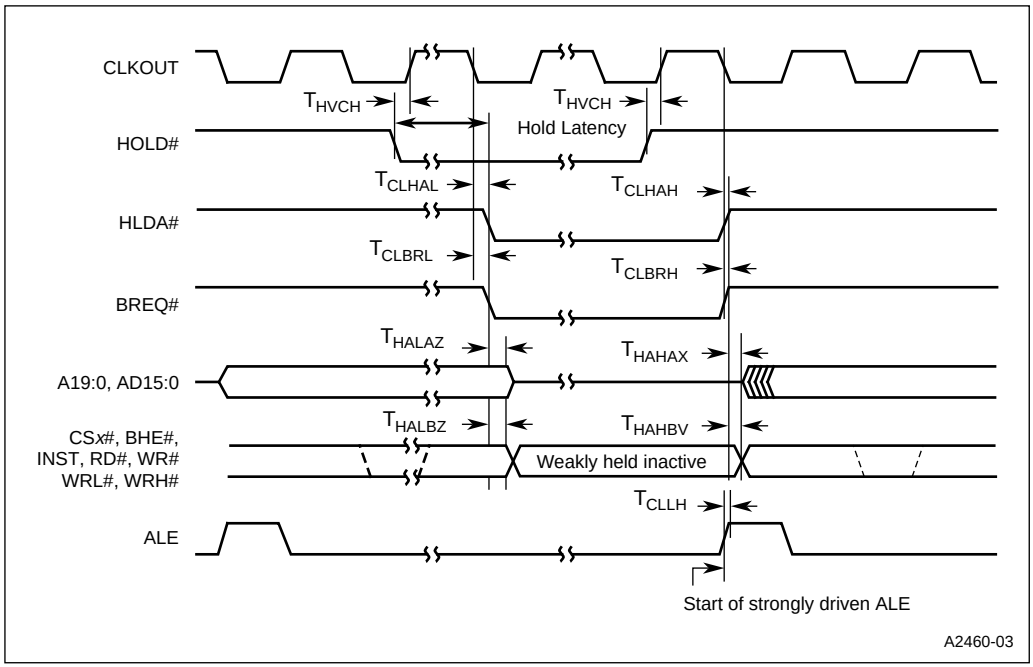


Figure 10. HOLD#/HLDA# Timing Diagram

AC Characteristics — Serial Port, Shift Register Mode

Table 15. Serial Port Timing — Shift Register Mode

Symbol	Parameter	V_{CC} = 4.5 V – 5.5 V		Units
		Min	Max	
T_{XLXL}	Serial Port Clock period (SP_BAUD ≥ *x*002H) (SP_BAUD = *x*001H) (Note 1)	 $6T_{XTAL1}$ $4T_{XTAL1}$		 ns ns
T_{QVXH}	Output data setup to clock high	$3T_{XTAL1}$		ns
T_{XHQX}	Output data hold after clock high	$2T_{XTAL1}$ – 50		ns
T_{XHQV}	Next output data valid after clock high		$2T_{XTAL1}$ + 50	ns
T_{DVXH}	Input data setup to clock high	$2T_{XTAL1}$ + 200		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		$5T_{XTAL1}$	ns

NOTE:
1. The minimum baud-rate register (SP_BAUD) value for receive is *x*002H and the minimum baud-rate register value for transmit is *x*001H.

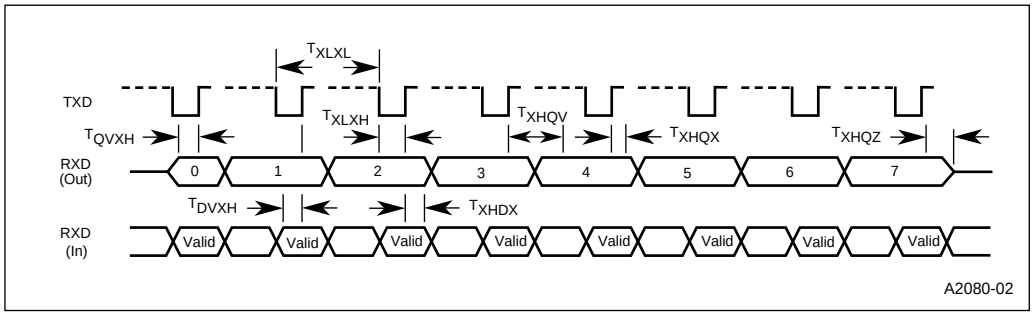


Figure 11. Serial Port Waveform — Shift Register Mode

External Clock Drive

Table 16. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Input frequency	8	25	MHz
T_{XLXL}	Period (T_{XTAL1})	40	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

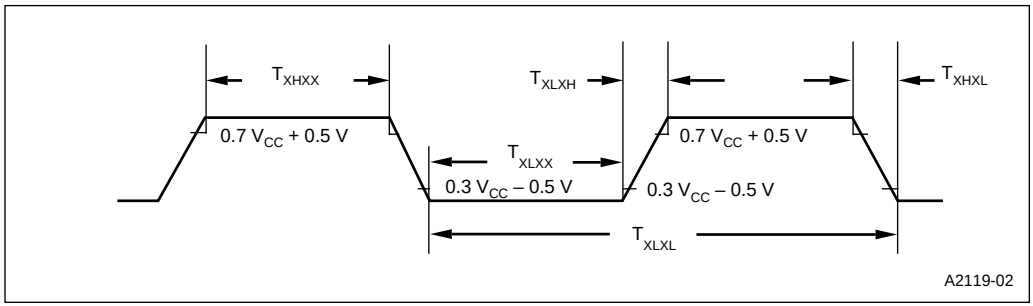


Figure 12. External Clock Drive Waveforms

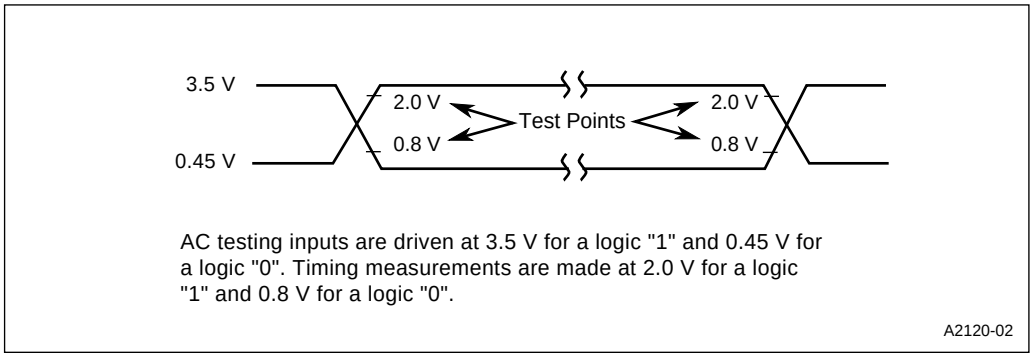
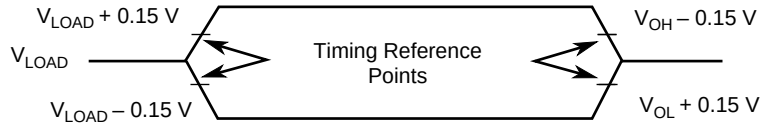


Figure 13. AC Testing Output Waveforms During 5.0 Volt Testing



For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2121-01

Figure 14. Float Waveforms During 5.0 Volt Testing

EXPLANATION OF AC SYMBOLS

Each AC timing symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H — High

L — Low

V — Valid

X — No Longer Valid

Z — Floating

Signals:

A — Address

AD — Address/Data Bus for Multiplexed Bus Mode

B — BHE#

C — CLKOUT

D — DATA

G — Buswidth

H — HOLD#

HA — HLDA#

L — ALE/ADV#

BR — BREQ#

R — RD#

W — WR#/WRH#/WRL#

X — XTAL1

Y — READY

Q — Data Out

S — Chip Select

8XC196NP ERRATA

Change identifiers have been used on embedded products since 1990. The change identifier is the last character in the FPO number. The FPO number is typically a nine character number located on the second line of the topside package mark. The following errata listing is applicable to the B–step (denoted by a “B” or “C” at the end of the topside tracking number):

1. Any jump, conditional jump, or call instruction located within six bytes of the top of a page, i.e., 0FFFA–0FFFFH, may cause a jump to the wrong page. To ensure this problem does not occur, place at least six NOPs at the top of each page.

The following errata listing is applicable to the A–step (denoted by an “A” at the end of the topside tracking number):

1. Any jump, conditional jump, or call instruction located within six bytes of the top of a page, i.e., 0FFFA–0FFFFH, may cause a jump to the wrong page. To ensure this problem does not occur, place at least six NOPs at the top of each page.

2. The illegal opcode interrupt vector is not taken when an illegal opcode is encountered. A branch to an unknown location occurs.

3. (1-Mbyte mode only.) If an interrupt is aborted, intentionally or unintentionally, an undesired branch to the lowest priority interrupt vector (FF2000H) may occur even if the lowest priority interrupt is not enabled. This may occur if any bit in the INT_MASK, INT_MASK1, INT_PEND, or INT_PEND1 register is cleared after the corresponding INT_PEND or INT_PEND1 bit is set.

4. (1-Mbyte mode only.) If a standard interrupt occurs at approximately the same time (this time is code dependent and therefore cannot be stated as an exact number of state times) as a PTS serviced interrupt, the PTS interrupt may be processed as a standard interrupt. The standard interrupt service routine for a PTS serviced interrupt (End-of-PTS) is typically used to modify the PTS control block and re-enable the PTS by setting the corresponding bit in the PTSSEL register. When this anomaly occurs, the End-of-PTS service routine will execute regardless of the value in PTSCOUNT. As a result, an undetermined number of PTS cycles will not occur. This applies to all PTS interrupts.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a “B” at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are important changes to the 272459-005 datasheet:

1. Revised Tables 8 through 15 and Figures 5, 6, 7, and 13 to reflect new or changed information.
2. Added Table 3 and Figure 9.
3. The input frequency on XTAL1, formerly called F_{OSC}, is now denoted by F_{XTAL1}.
4. The AC characteristics tables have been divided into the following: the timing specifications met by the device, and the timing specifications that must be met by the external memory system.
5. Maximum IOL and IOH specifications added to the DC characteristics tables.
6. AC timings T_{AVWL} and T_{AVRL} added to the AC characteristics–multiplexed bus mode tables.