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# Am27X010

1 Megabit (128 K x 8-Bit) CMOS ExpressROM Device

# DISTINCTIVE CHARACTERISTICS

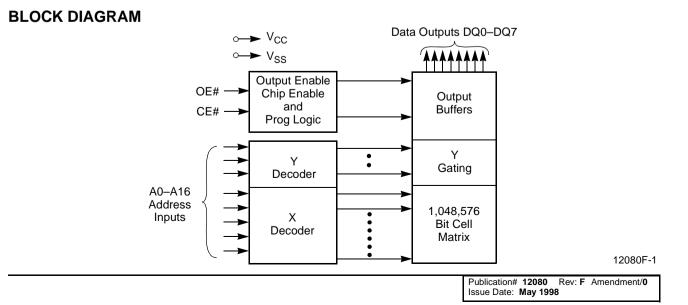
- As an OTP EPROM alternative:
  - Factory optimized programming
  - Fully tested and guaranteed
- As a Mask ROM alternative:
  - Shorter leadtime
  - Lower volume per code
- Fast access time
  - 55 ns
- Single +5 V power supply
- Compatible with JEDEC-approved EPROM pinout

- ±10% power supply tolerance
- High noise immunity
- Low power dissipation
  - 100 µA maximum CMOS standby current
- Available in Plastic Dual-In-line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)
- Latch-up protected to 100 mA from –1 V to V<sub>CC</sub> + 1 V
- Versatile features for simple interfacing
  - Both CMOS and TTL input/output compatibility
  - Two line control functions

# **GENERAL DESCRIPTION**

The Am27X010 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 128 Kwords by 8 bits per word and is available in plastic dual in-line packages (PDIP), as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs. Data can be accessed as fast as 55 ns, allowing high-performance microprocessors to operate with reduced WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100  $\mu$ W in standby mode.

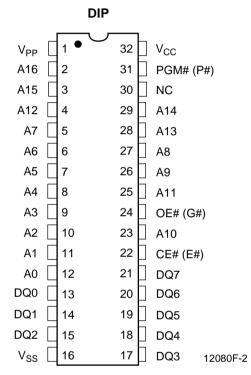


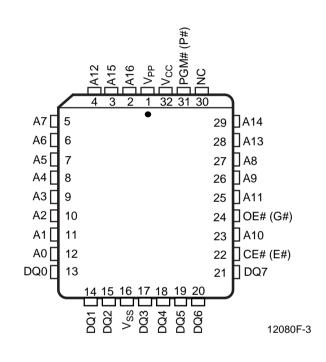
# **PRODUCT SELECTOR GUIDE**

Family Part Numb	Am27X010							
Speed Options	$V_{CC} = 5.0 \text{ V} \pm 5\%$							-255
	$V_{CC} = 5.0 \text{ V} \pm 10\%$	-55	-70	-90	-120	-150	-200	
Max Access Time	55	70	90	120	150	200	250	
CE# (E#) Access (ns)		55	70	90	120	150	200	250
OE# (G#) Access (ns)		35	70	40	50	65	75	100

# **CONNECTION DIAGRAMS**

# **Top View**





PLCC

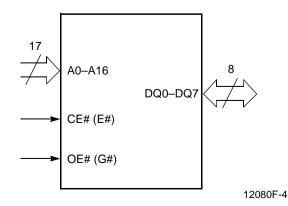
#### Notes:.

- 1. JEDEC nomenclature is in parenthesis.
- 2. Don't use (DU) for PLCC.

#### **PIN DESIGNATIONS**

A0–A16	= Address Inputs
CE# (E#)	<ul> <li>Chip Enable Input</li> </ul>
DQ0-DQ7	<ul> <li>Data Input/Outputs</li> </ul>
OE# (G#)	= Output Enable Input
PGM# (P#)	= Program Enable Input
V <sub>CC</sub>	= V <sub>CC</sub> Supply Voltage
V <sub>PP</sub>	= Program Voltage Input
V <sub>SS</sub>	= Ground
NC	= No Internal Connection

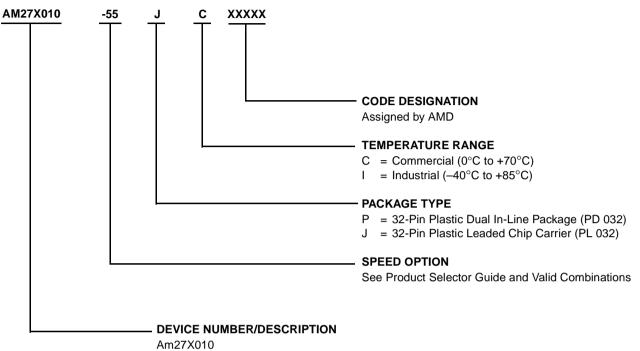
# LOGIC SYMBOL



### **ORDERING INFORMATION**

#### **Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



1 Megabit (128 K x 8-Bit) CMOS ExpressROM Device

Valid Combinations						
AM27X010-55						
AM27X010-70						
AM27X010-90						
AM27X010-120	PC, JC, PI, JI					
AM27X010-150						
AM27X010-200						
AM27X010-255 V <sub>CC</sub> = 5.0 V ± 5%						

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# FUNCTIONAL DESCRIPTION

### **Read Mode**

To obtain data at the device outputs, Chip Enable (CE#) and Output Enable (OE#) must be driven low. CE# controls the power to the device and is typically used to select the device. OE# enables the device to output data, independent of device selection. Addresses must be stable for at least  $t_{ACC}-t_{OE}$ . Refer to the Switching Waveforms section for the timing diagram.

# **Standby Mode**

The device enters the CMOS standby mode when CE# is at V<sub>CC</sub>  $\pm$  0.3 V. Maximum V<sub>CC</sub> current is reduced to 100 µA. The device enters the TTL-standby mode when CE# is at V<sub>IH</sub>. Maximum V<sub>CC</sub> current is reduced to 1.0 mA. When in either standby mode, the device places its outputs in a high-impedance state, independent of the OE# input.

# **Output OR-Tieing**

To accommodate multiple memory connections, a two-line control function provides:

- Low memory power dissipation, and
- Assurance that output bus contention will not occur.

CE# should be decoded and used as the primary device-selecting function, while OE# be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

# **System Applications**

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1  $\mu$ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V<sub>CC</sub> and V<sub>SS</sub> to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on Express-ROM device arrays, a 4.7  $\mu$ F bulk electrolytic capacitor should be used between V<sub>CC</sub> and V<sub>SS</sub> for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

#### MODE SELECT TABLE Mode CE# OE# PGM# VPP Outputs Read Х Х VIL VIL DOUT Output Disable Х Х Х High Z VIH Х Standby (TTL) V<sub>IH</sub> Х Х High Z $V_{CC}\pm0.3~V$ Standby (CMOS) Х Х Х High Z

Note:

 $X = Either V_{IH} or V_{IL}$ .

### **ABSOLUTE MAXIMUM RATINGS**

Storage Temperature
OTP Products
Ambient Temperature
with Power Applied
Voltage with Respect to V <sub>SS</sub>
All pins except V_CC $\ldots$ –0.6 V to V_CC + 0.6 V
$V_{CC}$ (Note 1)
Note:

1. Minimum DC voltage on input or I/O pins –0.5 V. During voltage transitions, the input may overshoot  $V_{SS}$  to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is  $V_{CC}$  + 5 V. During voltage transitions, input and I/O pins may overshoot to  $V_{CC}$  + 2.0 V for periods up

to 20 ns.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

# **OPERATING RANGES**

Ambient Temperature (T <sub>A</sub> )	0°C to +70°C
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#### Industrial (I) Devices

Ambient Temperature (T<sub>A</sub>) .....-40°C to +85°C

#### **Supply Read Voltages**

$V_{CC}$ for ± 5% devices	+4.75 V to +5.25 V
$V_{CC}$ for ± 10% devices $\ldots\ldots\ldots$	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

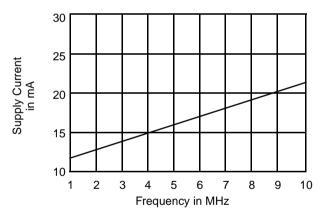
# DC CHARACTERISTICS over operating range (unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions	Min	Мах	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA		0.45	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	+0.8	V
I <sub>LI</sub>	Input Load Current	$V_{IN} = 0 V \text{ to } V_{CC}$		1.0	μA
I <sub>LO</sub>	Output Leakage Current	$V_{OUT} = 0 V \text{ to } V_{CC}$		10	μA
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Note 2)	$CE\# = V_{IL}, f = 10 \text{ MHz},$ $I_{OUT} = 0 \text{ mA}$		30	mA
I <sub>CC2</sub>	V <sub>CC</sub> TTL Standby Current	CE# = V <sub>IH</sub>		1.0	mA
I <sub>CC3</sub>	V <sub>CC</sub> CMOS Standby Current	$CE\#=V_{CC}\pm0.3\;V$		100	μA

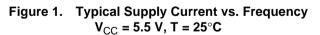
Caution: The device must not be removed from (or inserted into) a socket when V<sub>CC</sub> or V<sub>PP</sub> is applied.

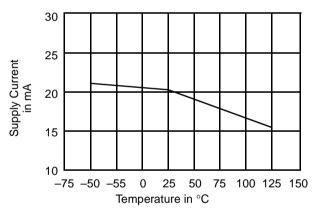
#### Notes:

- 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- 2.  $I_{CC1}$  is tested with  $OE\# = V_{IH}$  to simulate open outputs.
- Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V<sub>CC</sub> + 0.5 V, which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.

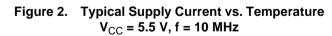


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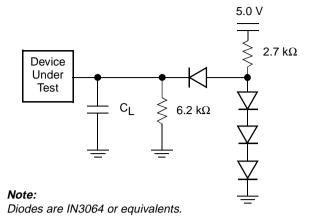




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# **TEST CONDITIONS**



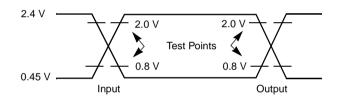
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Figure 3. Test Setup

#### Table 1. Test Specifications

Test Condition	All	Unit	
Output Load	1 TTL gate		
Output Load Capacitance, C <sub>L</sub> (including jig capacitance)	100	pF	
Input Rise and Fall Times	≤ 20	ns	
Input Pulse Levels	0.45–2.4	V	
Input timing measurement reference levels	0.8, 2.0	V	
Output timing measurement reference levels	0.8, 2.0	V	

#### SWITCHING TEST WAVEFORM



**Note:** For  $C_L = 100 \, pF$ .

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# **KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS					
	Steady						
	Cha	Changing from H to L					
	Cha	anging from L to H					
XXXXXX	Don't Care, Any Change Permitted Changing, State Unknown						
	Does Not Apply Center Line is High Impedance State (High Z						

KS000010-PAL

# **AC CHARACTERISTICS**

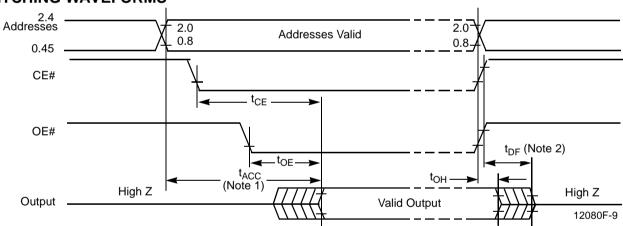
Paramete	er Symbols				Am27X010							
JEDEC	Standard	Description	Test Set	Test Setup		-70	-90	-120	-150	-200	-255	Unit
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	CE#, OE# = V <sub>IL</sub>	Max	55	70	90	120	150	200	250	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	OE# = V <sub>IL</sub>	Max	55	70	90	120	150	200	250	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$CE\# = V_{IL}$	Max	35	35	40	50	65	75	75	ns
t <sub>EHQZ</sub> t <sub>GHQZ</sub>	t <sub>DF</sub> (Note 2)	Chip Enable High or Output Enable High to Output High Z, Whichever Occurs First		Max	25	25	25	35	35	40	40	ns
t <sub>AXQX</sub>	t <sub>ОН</sub>	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First		Min	0	0	0	0	0	0	0	ns

**Caution:** Do not remove the device from (or insert it into) a socket or board that has  $V_{PP}$  or  $V_{CC}$  applied.

#### Notes:

- 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$
- 2. This parameter is sampled and not 100% tested.
- 3. Switching characteristics are over operating range, unless otherwise specified.
- 4. See Figure 3 and Table 1 for test specifications.

# SWITCHING WAVEFORMS



#### Notes:

- 1. OE# may be delayed up to  $t_{ACC} t_{OE}$  after the falling edge of the addresses without impact on  $t_{ACC}$ .
- 2. t<sub>DF</sub> is specified from OE# or CE#, whichever occurs first.

### PACKAGE CAPACITANCE

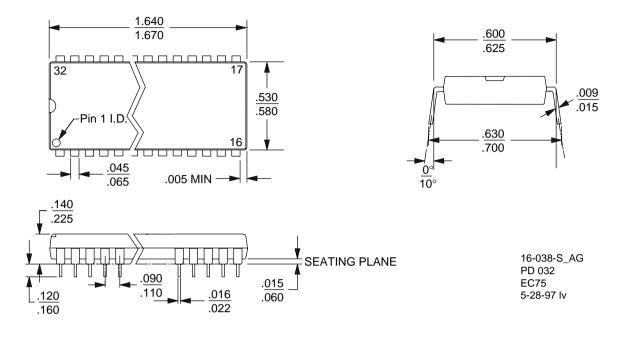
Parameter				032	PL		
Symbol	Parameter Description	Test Conditions	Тур	Max	Тур	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	8	12	8	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{OUT} = 0$	11	14	11	12	pF

#### Notes:

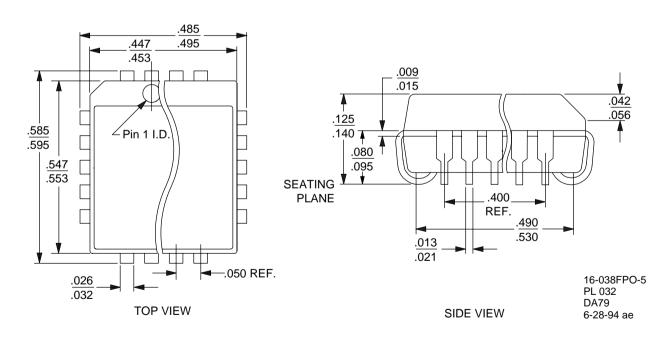
2.  $T_A = +25^{\circ}C, f = 1 MHz.$ 

<sup>1.</sup> This parameter is only sampled and not 100% tested.

# PHYSICAL DIMENSIONS PD 032—32-Pin Plastic Dual In-Line Package (measured in inches)



PL 032—32-Pin Plastic Leaded Chip Carrier (measured in inches)



# 

# **REVISION SUMMARY FOR AM27X010**

#### **Revision F**

#### Global

Changed formatting to match current data sheets.

#### **Distinctive Characteristics**

Fast access time: Changed 70 ns to 55 ns.

#### **General Description**

Changed "Data can be accessed as fast as 70 ns" to "Data can be accessed as fast as 55 ns".

#### **Product Selector Guide**

Added the -55 speed option.

#### **Ordering Information**

*Package Type:* Corrected "P = 28-Pin Plastic Dual In-Line Package (PD 028)" to "P = 32-Pin Plastic Dual In-Line Package (PD 032)".

Speed Option: Changed -70 to -55.

Valid Combinations: Added Am27X010-55.

#### **AC Characterisitics**

Added the -55 speed option.

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