SUPPLEMENT

Am29LV800B Known Good Die

8 Megabit (1 M x 8-Bit/512 K x 16-Bit)
CMOS 3.0 Volt-only, Boot Sector Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — 2.7 to 3.6 V for read, program, and erase operations
  - — Ideal for battery-powered applications
- **Manufactured on 0.35 μm process technology**
- **High performance**
  - — 90 or 120 ns access time
- **Low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 7 mA read current
  - — 15 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and fifteen 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

Publication# **21356** Rev: **B** Amendment/**+1**
Issue Date: **March 1998**

GENERAL DESCRIPTION

The Am29LV800B in Known Good Die (KGD) form is an 8 Mbit, 3.0 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29LV800B Features

The Am29LV800B is an 8 Mbit, 3.0 volt-only Flash memory organized as 1,048,576 bytes or 524,288 words. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. No V_{PP} is required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

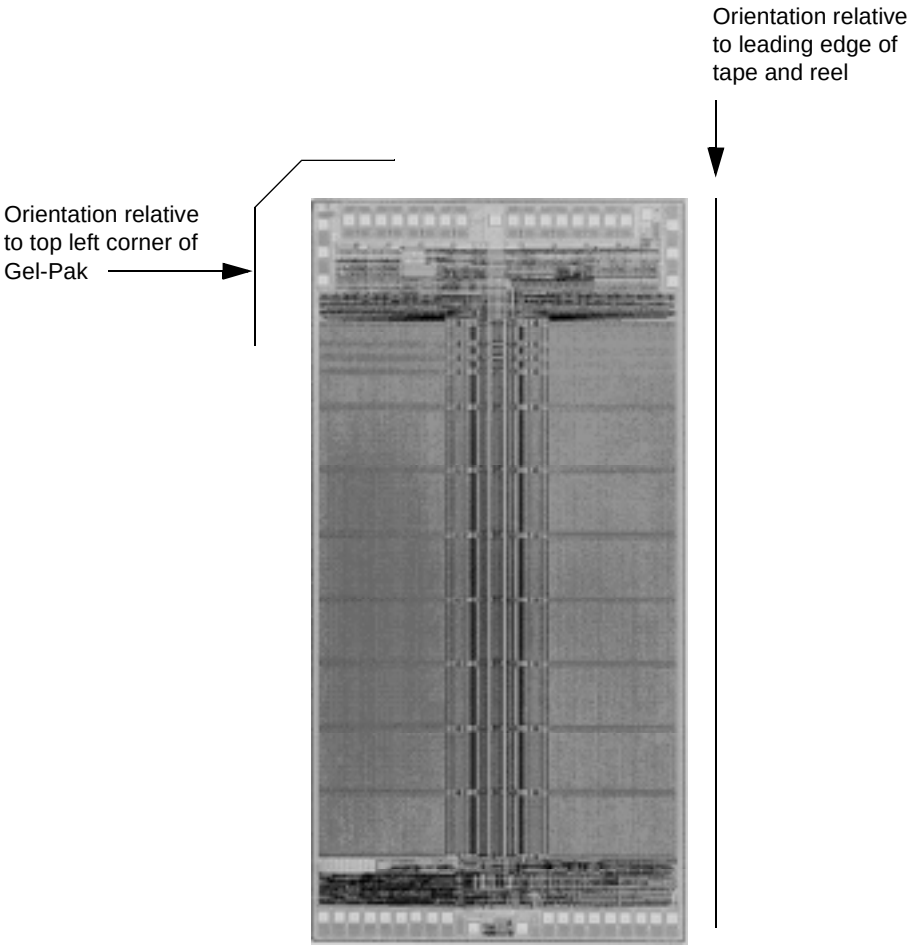
ELECTRICAL SPECIFICATIONS

Refer to the Am29LV800B data sheet, publication number 21490, for full electrical specifications on the Am29LV800B in KGD form.

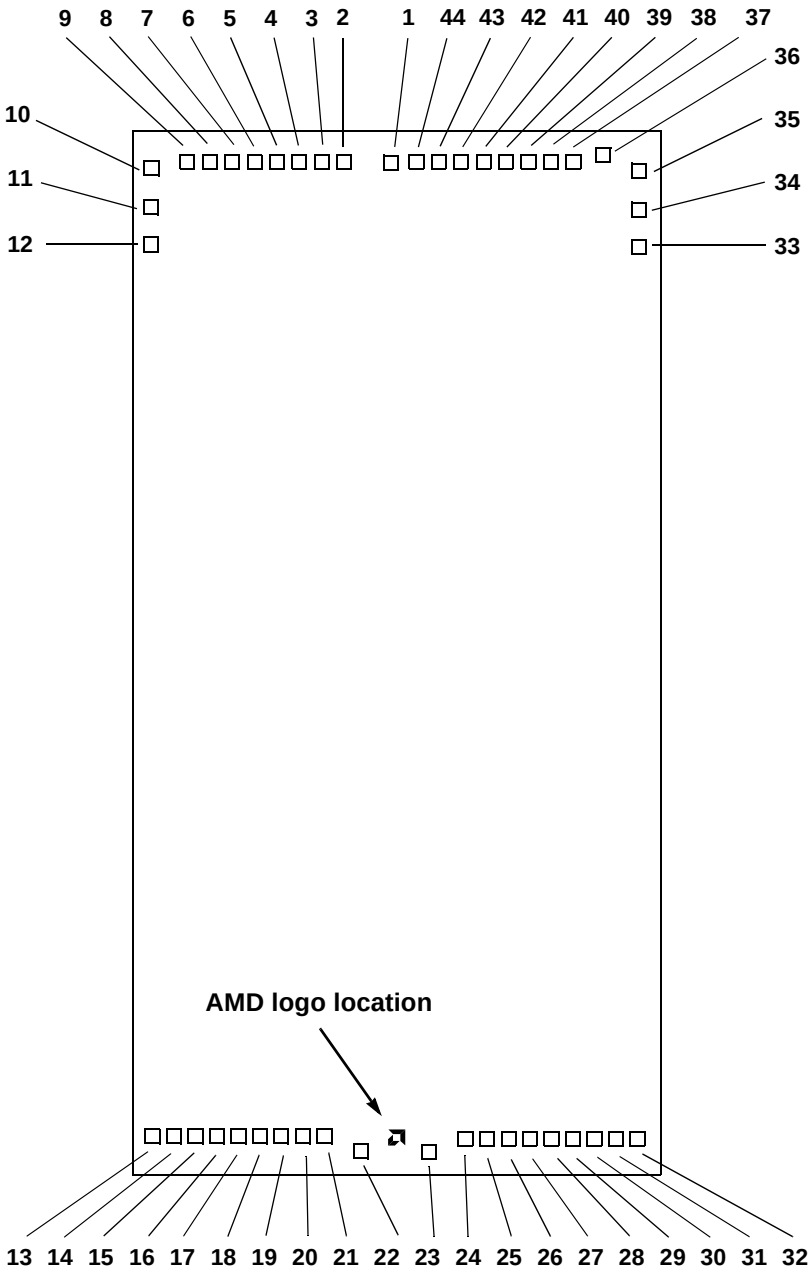
PRODUCT SELECTOR GUIDE

Family Part Number	Am29LV800B KGD	
Speed Option (V_{CC} = 2.7 – 3.6 V)	**-90**	**-120**
Max Access Time, t_{ACC} (ns)	90	120
Max CE# Access, t_{CE} (ns)	90	120
Max OE# Access, t_{OE} (ns)	35	50

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

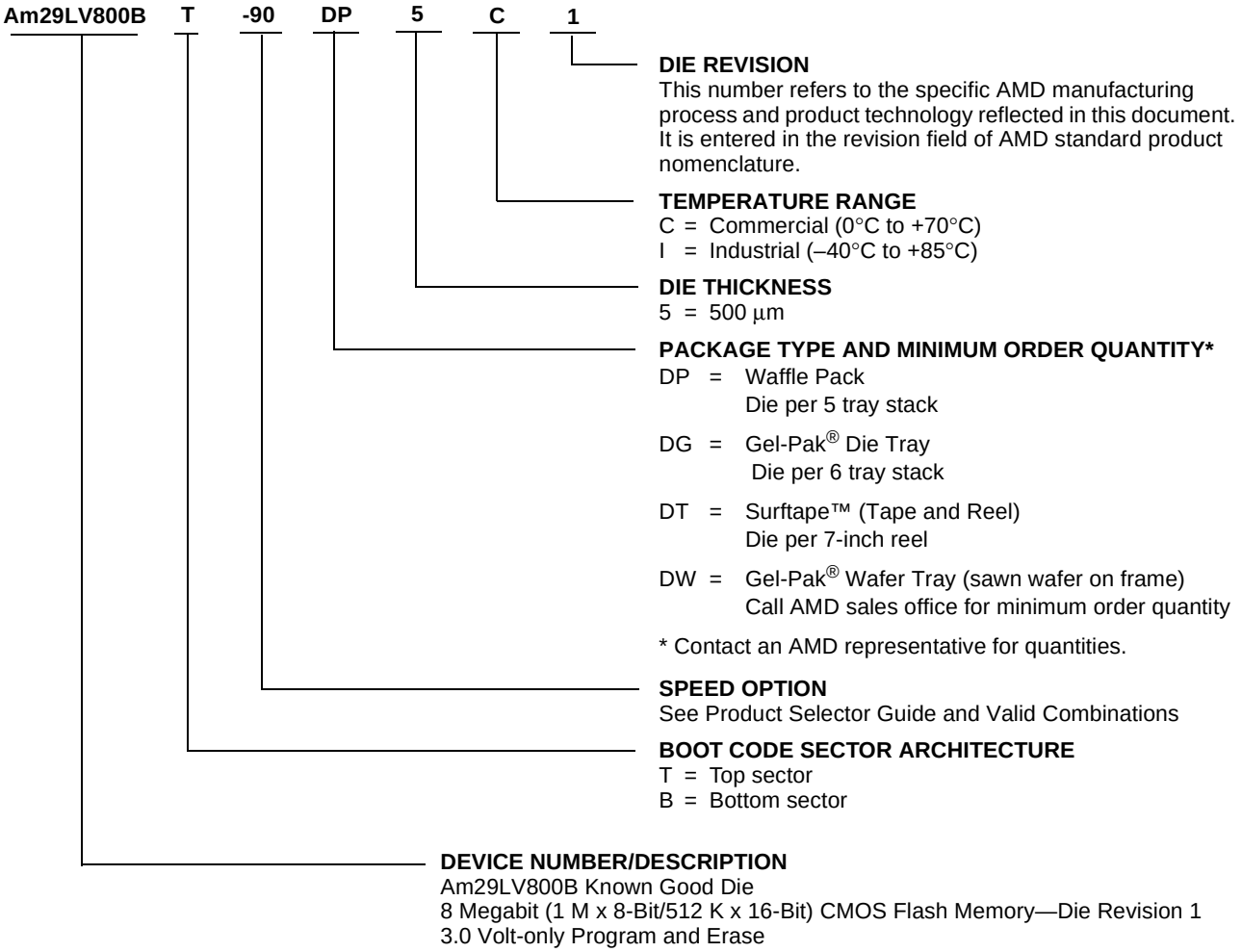
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.0000	0.0000
2	DQ4	–12.74	0.00	–0.3235	0.0000
3	DQ12	–18.96	0.00	–0.4817	0.0000
4	DQ5	–25.11	0.00	–0.6377	0.0000
5	DQ13	–31.33	0.00	–0.7959	0.0000
6	DQ6	–37.48	0.00	–0.9519	0.0000
7	DQ14	–43.71	0.00	–1.1101	0.0000
8	DQ7	–49.85	0.00	–1.2661	0.0000
9	DQ15/A–1	–56.08	0.00	–1.4243	0.0000
10	V_{SS}	–66.01	–1.69	–1.6767	–0.0430
11	BYTE#	–66.01	–12.30	–1.6767	–0.3123
12	A16	–66.01	–22.92	–1.6767	–0.5822
13	A15	–65.65	–266.81	–1.6674	–6.7770
14	A14	–59.50	–266.81	–1.5114	–6.7770
15	A13	–53.80	–266.81	–1.3664	–6.7770
16	A12	–47.65	–266.81	–1.2104	–6.7770
17	A11	–41.95	–266.81	–1.0654	–6.7770
18	A10	–35.80	–266.81	–0.9094	–6.7770
19	A9	–30.09	–266.55	–0.7644	–6.7704
20	A8	–23.85	–266.81	–0.6059	–6.7770
21	WE#	–18.15	–266.81	–0.4609	–6.7770
22	RESET#	–8.06	–270.78	–0.2047	–6.8778
23	RY/BY#	10.07	–270.78	0.2558	–6.8778
24	A18	20.14	–266.81	0.5116	–6.7770
25	A17	25.85	–266.81	0.6566	–6.7770
26	A7	31.99	–266.81	0.8126	–6.7770
27	A6	37.70	–266.81	0.9576	–6.7770
28	A5	43.84	–266.81	1.1136	–6.7770
29	A4	49.55	–266.81	1.2586	–6.7770
30	A3	55.69	–266.81	1.4146	–6.7770
31	A2	61.40	–266.81	1.5596	–6.7770
32	A1	67.54	–266.81	1.7156	–6.7770
33	A0	67.91	–23.08	1.7249	–0.5862
34	CE#	67.91	–12.45	1.7249	–0.3163
35	V_{SS}	67.91	–1.91	1.7249	–0.0484
36	OE#	58.00	2.27	1.4732	0.0576
37	DQ0	50.02	0.00	1.2705	0.0000
38	DQ8	43.79	0.00	1.1123	0.0000
39	DQ1	37.65	0.00	0.9563	0.0000
40	DQ9	31.42	0.00	0.7981	0.0000
41	DQ2	25.28	0.00	0.6421	0.0000
42	DQ10	19.05	0.00	0.4839	0.0000
43	DQ3	12.91	0.00	0.3279	0.0000
44	DQ11	6.68	0.00	0.1697	0.0000

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
Am29LV800BT-90 Am29LV800BB-90	DPC 1, DPI 1, DGC 1, DGI 1, DTC 1, DTI 1, DWC 1, DWI 1
Am29LV800BT-120 Am29LV800BB-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29LV800B product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

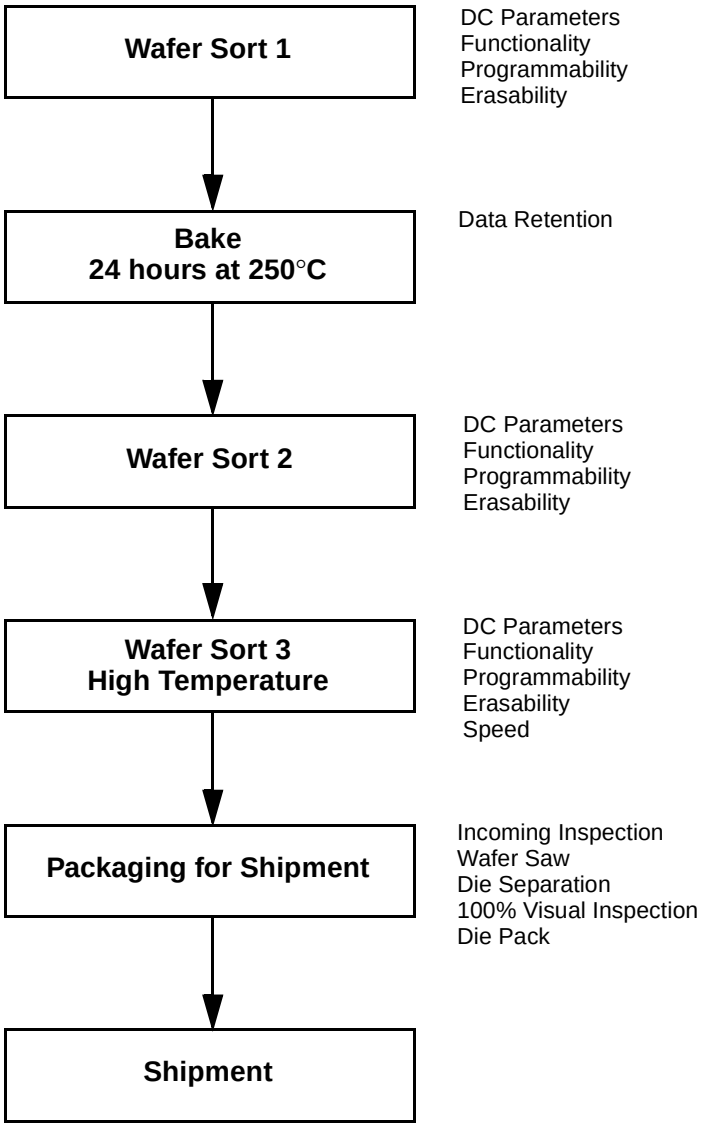


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 147 mils x 293 mils
. . . . . 3.74 mm x 7.45 mm

Die Thickness . . . . . ~20 mils

Bond Pad Size . . . . . 3.94 mils x 3.94 mils
. . . . . 100 µm x 100 µm

Pad Area Free of Passivation . . . . . 15.52 mils^2
. . . . . $10{,}000 \ \mu m^2$

Pads Per Die 44

Bond Pad Metalization . . . . . Al/Cu/Si

Die Backside . . . . . No metal, may be grounded (optional)

Passivation . . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . 2.7 V to 3.6 V

Operating Temperature

Commercial . . . . . 0°C to +70°C

Industrial . . . . . –40°C to +85°C

MANUFACTURING INFORMATION

Manufacturing . . . . . FASL

Test . . . . . SDC

Manufacturing ID (Top Boot) 98925AK

(Bottom Boot) 98925ABK

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process CS39

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to AMD Products under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

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REVISION SUMMARY FOR AM29LV800B KNOWN GOOD DIE

Revision B

Formatted to match current template. Updated Distinctive Characteristics and General Description sections using the current main data sheet. Updated for CS39 process technology.

Revision B+1

Distinctive Characteristics

Changed read and program/erase current to match data sheet.

Pad Description

Corrected signal names for pads 13–44. Replaced values for all pad coordinates.