

# 2SA1341, 2SC3395



2018A

T-37-13  
T-35-11

PNP/NPN Epitaxial Planar  
Silicon Transistors

## Switching Applications (with Bias Resistances R1=47kΩ, R2=47kΩ)

©1283C

### Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit.

### Features

- Built-in bias resistor (R1=47kΩ, R2=47kΩ).
- Small-sized package (CP).

( ) : 2SA1341

### Absolute Maximum Ratings/Ta=25°C

			unit
Collector to Base Voltage	VCBO	(-)50	V
Collector to Emitter Voltage	VCEO	(-)50	V
Emitter to Base Voltage	VEBO	(-)10	V
Collector Current	IC	(-)100	mA
Peak Collector Current	icp	(-)200	mA
Collector Dissipation	PC	200	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55 to +150	°C

### Electrical Characteristics/Ta=25°C

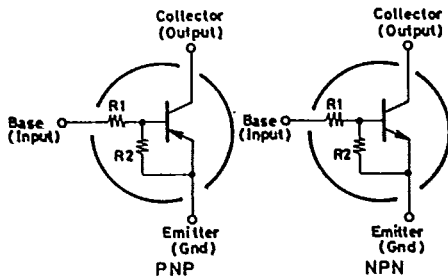
			min	typ	max	unit
Collector Cutoff Current	ICBO	VCB=(-)40V, IE=0			(-)0.1	μA
Collector Cutoff Current	ICEO	VCE=(-)40V, IB=0			(-)0.5	μA
Emitter Cutoff Current	IEBO	VEB=(-)5V, IC=0	(-)30	(-)53	(-)80	μA
DC Current Gain	hFE	VCE=(-)5V, IC=(-)5mA	50			
Gain Band-width product	fT	VCE(-)10V, IC(-)5mA		250 (200)		MHz
Output Capacitance	cob	VCB=(-)10V, f=1MHz		3.5 (5.3)		pF
Collector to Emitter Saturation Voltage	VCE(sat)	IC=(-)5mA, IB=(-)0.25mA	(-)0.1	(-)0.3		V

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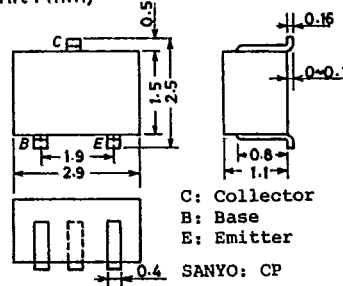
### Marking

2SA1341:BL, 2SC3395:BY

### Electrical Connection



### Case Outline 2018A (unit : mm)



2SA1341/2SC3395

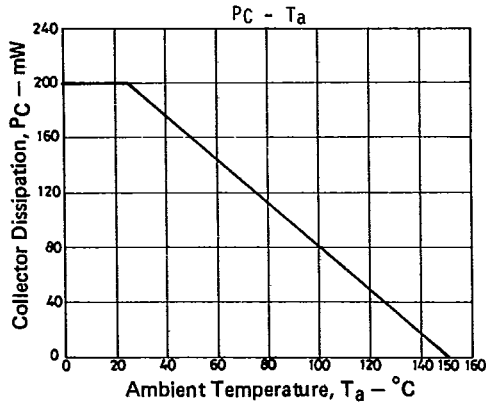
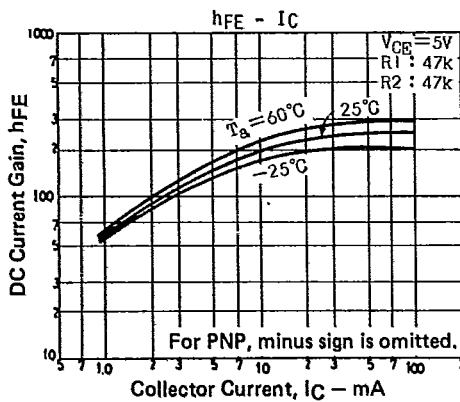
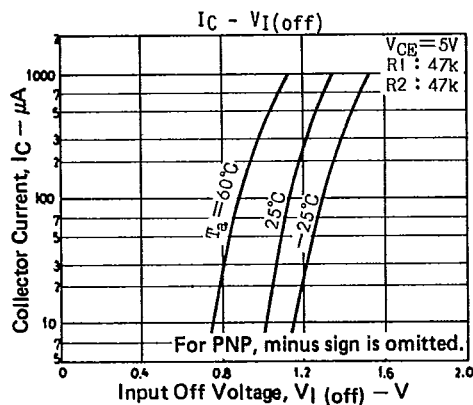
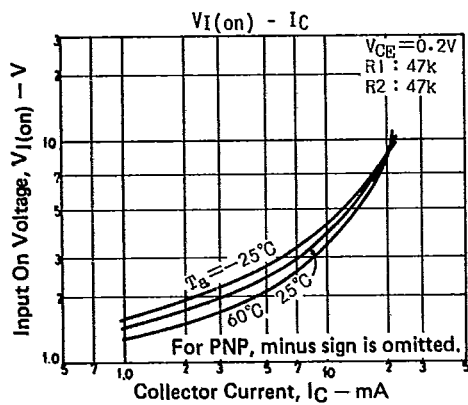
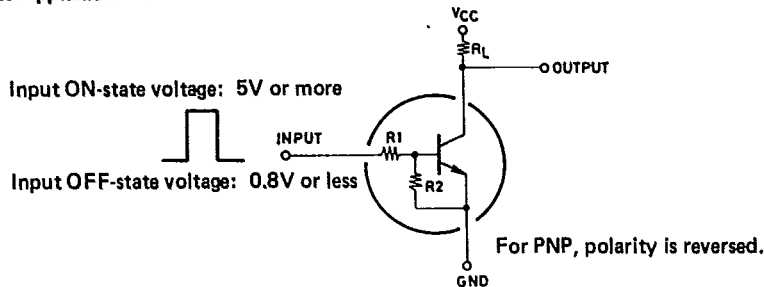
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			min	typ	max	unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = (-)10\mu A, I_E = 0$	(-)50			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = (-)100\mu A, R_{BE} = \infty$	(-)50			V
Input Off Voltage	$V_{I(off)}$	$V_{CE} = (-)5V, I_C = (-)100\mu A$	(-)0.8	(-)1.1	(-)1.5	V
Input On Voltage	$V_{I(on)}$	$V_{CE} = (-)0.2V, I_C = (-)5mA$	(-)1.0	(-)2.5	(-)5.0	V
Input Resistance	$R_1$		32	47	62	k $\Omega$
Input Resistance Ratio	$R_1/R_2$		0.9	1.0	1.1	-

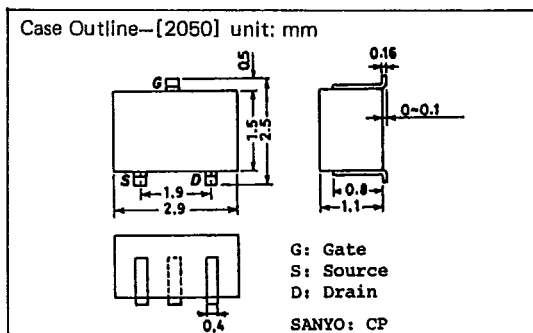
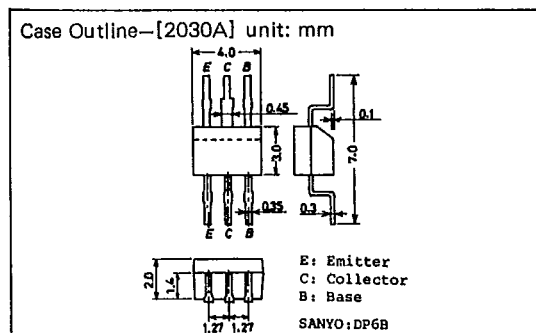
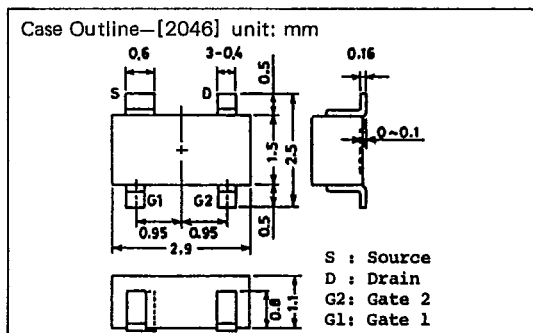
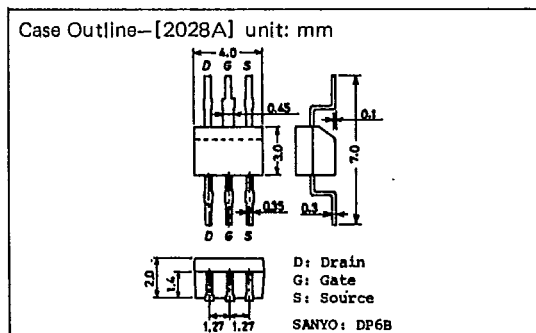
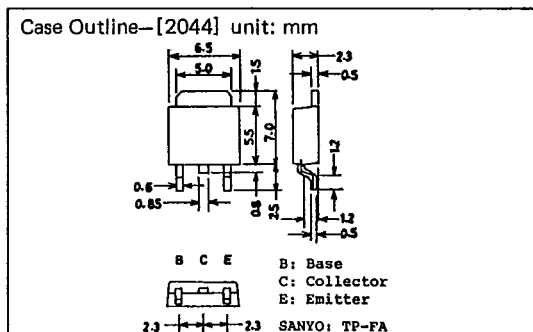
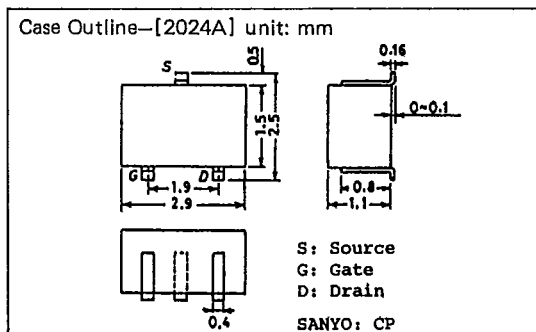
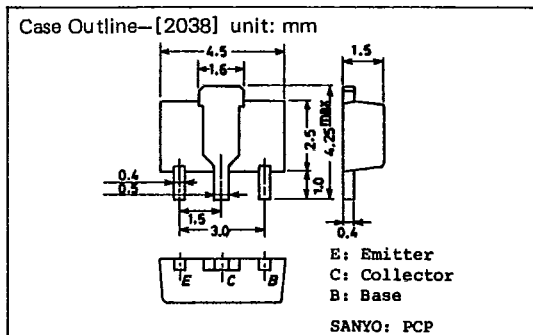
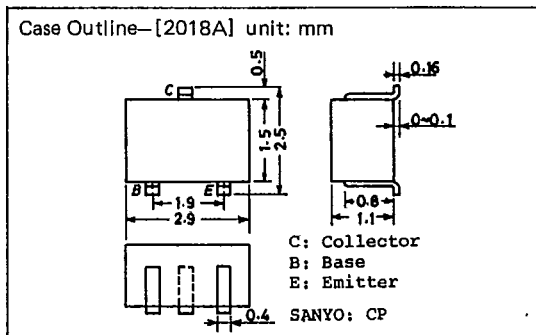
■ Sample Application Circuit



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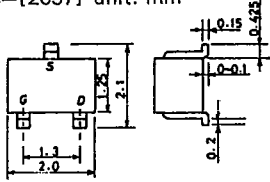
# CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



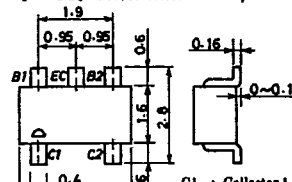
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Case Outline—[2057] unit: mm



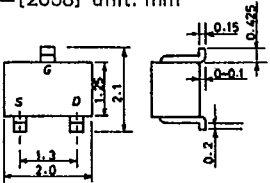
S: Source  
G: Gate  
D: Drain  
SANYO: MCP

Case Outline—[2066] unit: mm



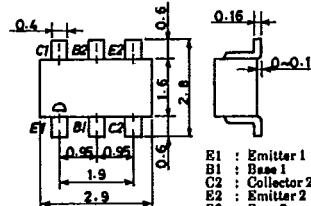
C1 : Collector 1  
C2 : Collector 2  
B2 : Base 2  
EC : Emitter Common  
B1 : Base 1  
SANYO : CP6

Case Outline—[2058] unit: mm



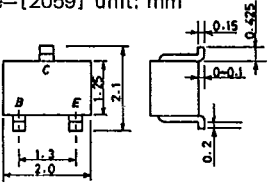
G: Gate  
S: Source  
D: Drain  
SANYO: MCP

Case Outline—[2067] unit: mm



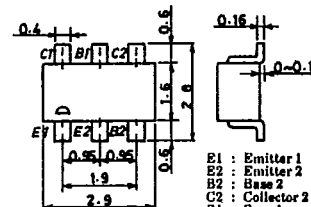
E1 : Emitter 1  
B1 : Base 1  
C2 : Collector 2  
E2 : Emitter 2  
B2 : Base 2  
C1 : Collector 1  
SANYO : CP6

Case Outline—[2059] unit: mm



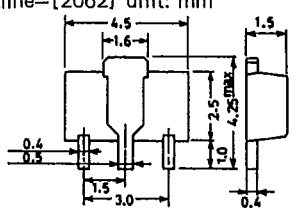
B: Base  
C: Collector  
E: Emitter  
SANYO: MCP

Case Outline—[2068] unit: mm



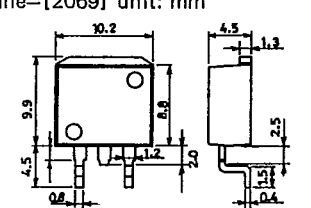
E1 : Emitter 1  
E2 : Emitter 2  
B2 : Base 2  
C2 : Collector 2  
B1 : Base 1  
C1 : Collector 1  
SANYO : CP6

Case Outline—[2062] unit: mm



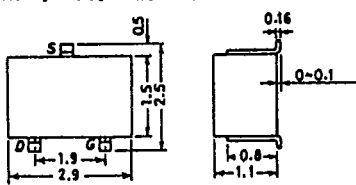
S: Source  
D: Drain  
G: Gate  
SANYO: PCP

Case Outline—[2069] unit: mm



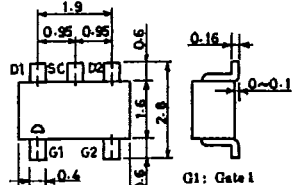
B: Base  
C: Collector  
E: Emitter  
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source  
D: Drain  
G: Gate  
SANYO: CP

Case Outline—[2070] unit: mm



G1 : Gate 1  
G2 : Gate 2  
D2 : Drain 2  
SC : Source Common  
D1 : Drain 1  
SANYO : CP6

T-9120

