

# 2SA1343, 2SC3397



2018A

PNP/NPN Epitaxial Planar  
Silicon Transistors

T-37-13  
T-35-11

## Switching Applications (with Bias Resistances $R_1=46k\Omega$ , $R_2=23k\Omega$ )

©1285C

### Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit.

### Features

- Built-in bias resistor ( $R_1=46k\Omega$ ,  $R_2=23k\Omega$ ).
- Small-sized package (CP).

( ) : 2SA1343

### Absolute Maximum Ratings/ $T_a=25^\circ\text{C}$

			unit
Collector to Base Voltage	$V_{CB0}$	(-)50	V
Collector to Emitter Voltage	$V_{CEO}$	(-)50	V
Emitter to Base Voltage	$V_{EBO}$	(-)10	V
Collector Current	$I_C$	(-)100	mA
Peak Collector Current	$i_{cp}$	(-)200	mA
Collector Dissipation	$P_C$	200	mW
Junction Temperature	$T_j$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### Electrical Characteristics/ $T_a=25^\circ\text{C}$

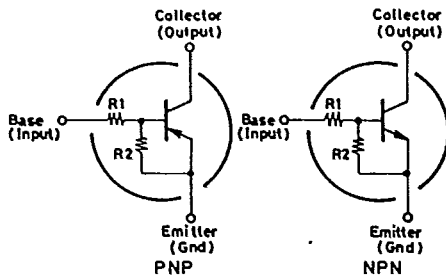
			min	typ	max	unit
Collector Cutoff Current	$I_{CBO}$	$V_{CB}=(-)40\text{V}, I_E=0$			(-)0.1	$\mu\text{A}$
Collector Cutoff Current	$I_{CEO}$	$V_{CE}=(-)40\text{V}, I_B=0$			(-)0.5	$\mu\text{A}$
Emitter Cutoff Current	$I_{EBO}$	$V_{EB}=(-)5\text{V}, I_C=0$	(-)40	(-)72	(-)100	$\mu\text{A}$
DC Current Gain	$h_{FE}$	$V_{CE}=(-)5\text{V}, I_C=(-)5\text{mA}$	50			
Gain Band-width product	$f_T$	$V_{CE}=(-)10\text{V}, I_C=(-)5\text{mA}$		250 (200)		MHz
Output Capacitance	$c_{ob}$	$V_{CB}=(-)10\text{V}, f=1\text{MHz}$		3.5 (5.3)		pF
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)5\text{mA}, I_B=(-)0.25\text{mA}$	(-)0.1	(-)0.3		V

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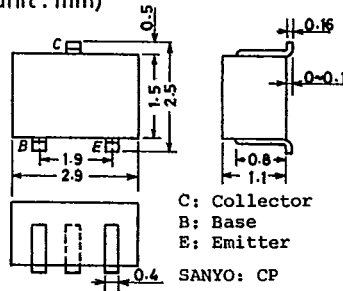
### Marking

2SA1343: DL, 2SC3397: DY

### Electrical Connection



### Case Outline 2018A (unit: mm)



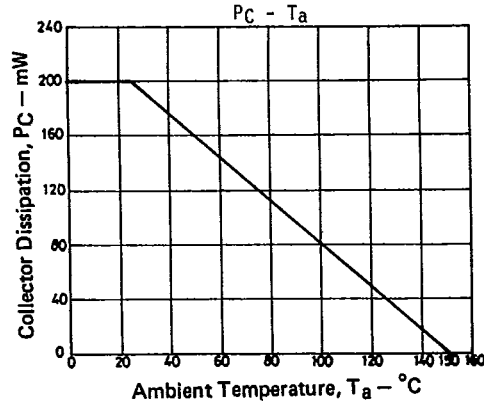
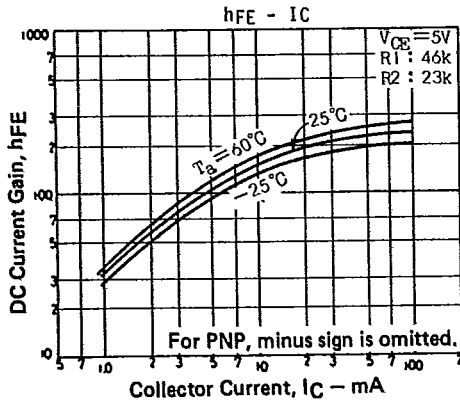
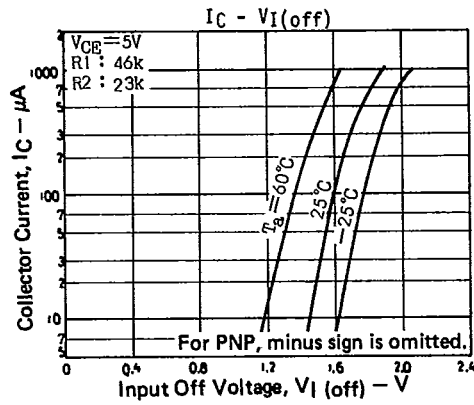
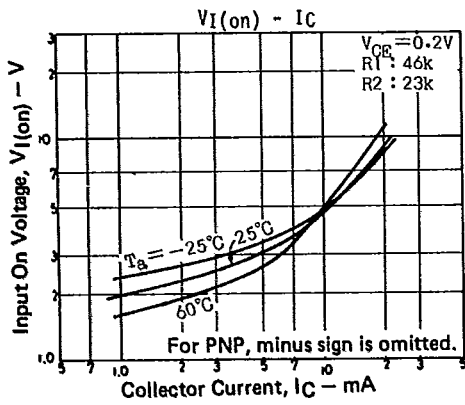
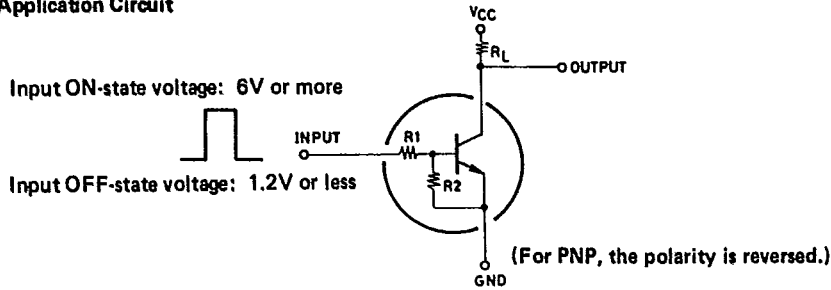
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			min	typ	max	unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu A, I_E=0$	(-)50			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)100\mu A, R_{BE}=\infty$	(-)50			V
Input Off Voltage	$V_{I(off)}$	$V_{CE}=(-)5V, I_C=(-)100\mu A$	(-)1.2	(-)1.6	(-)2.3	V
Input On Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2V, I_C=(-)5mA$	(-)1.5	(-)3.1	(-)6.0	V
Input Resistance	R1		32	46	60	k $\Omega$
Input Resistance Ratio	R1/R2		1.8	2.0	2.2	-

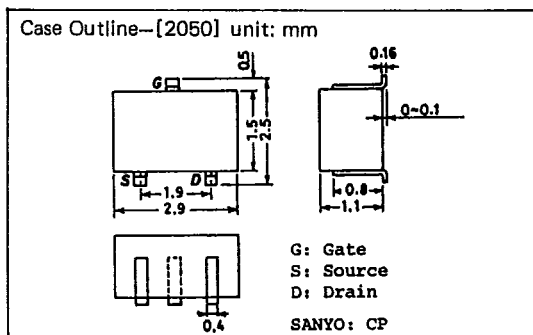
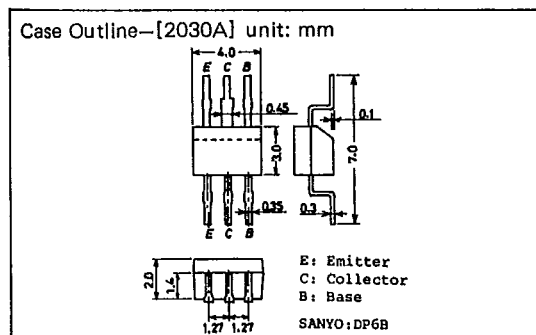
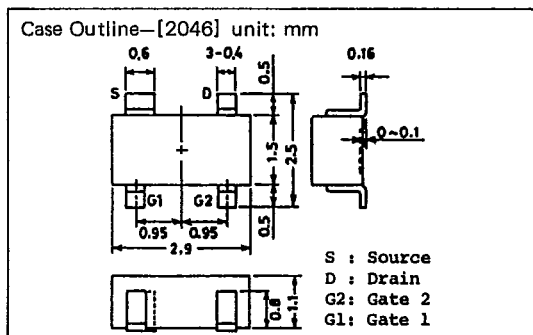
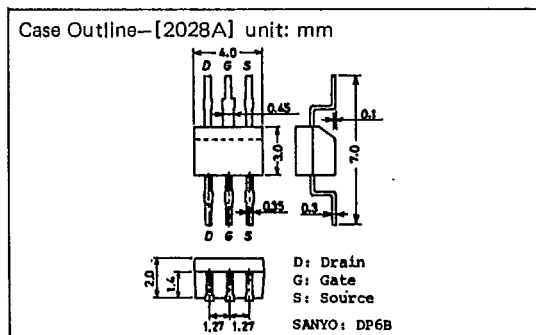
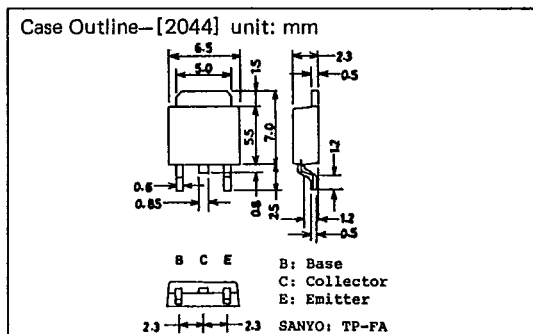
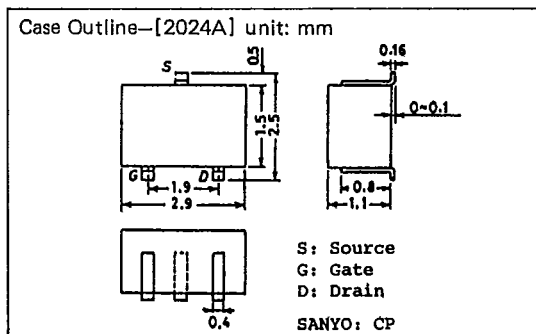
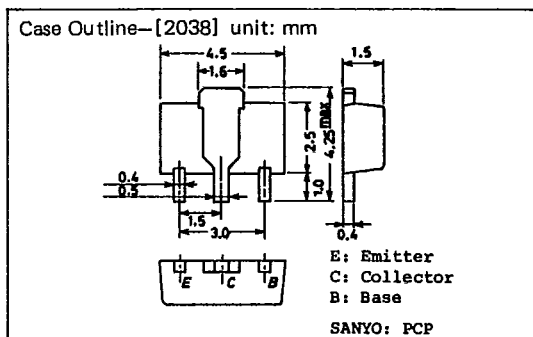
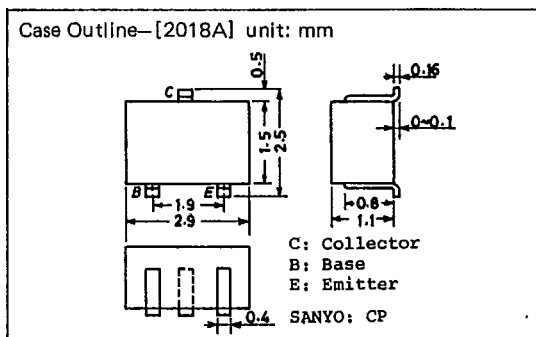
■ Sample Application Circuit



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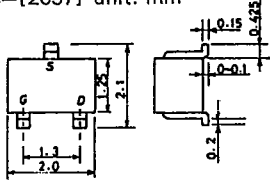
# CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



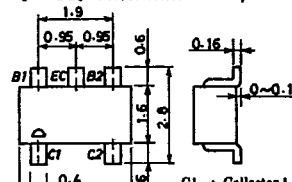
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Case Outline—[2057] unit: mm



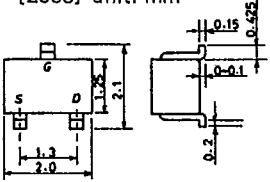
S: Source  
G: Gate  
D: Drain  
SANYO: MCP

Case Outline—[2066] unit: mm



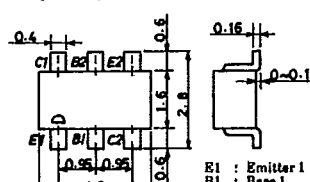
C1 : Collector 1  
C2 : Collector 2  
B2 : Base 2  
EC : Emitter Common  
B1 : Base 1  
SANYO : CP6

Case Outline—[2058] unit: mm



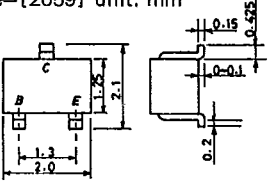
G: Gate  
S: Source  
D: Drain  
SANYO: MCP

Case Outline—[2067] unit: mm



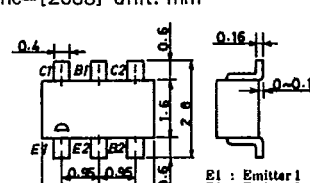
E1 : Emitter 1  
B1 : Base 1  
C2 : Collector 2  
E2 : Emitter 2  
B2 : Base 2  
C1 : Collector 1  
SANYO : CP6

Case Outline—[2059] unit: mm



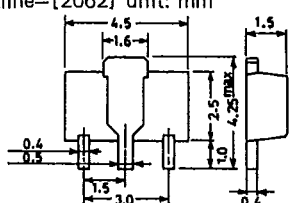
B: Base  
C: Collector  
E: Emitter  
SANYO: MCP

Case Outline—[2068] unit: mm



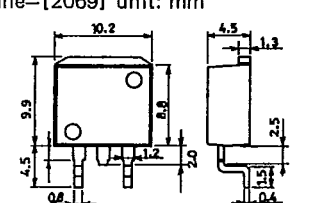
B1 : Emitter 1  
E2 : Emitter 2  
B2 : Base 2  
C2 : Collector 2  
B1 : Base 1  
C1 : Collector 1  
SANYO : CP6

Case Outline—[2062] unit: mm



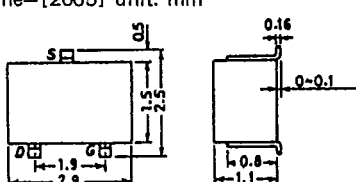
S: Source  
D: Drain  
G: Gate  
SANYO: PCP

Case Outline—[2069] unit: mm



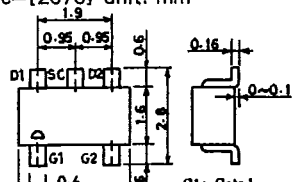
B: Base  
C: Collector  
E: Emitter  
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source  
D: Drain  
G: Gate  
SANYO: CP

Case Outline—[2070] unit: mm



G1 : Gate 1  
G2 : Gate 2  
D2 : Drain 2  
SC : Source Common  
D1 : Drain 1  
SANYO : CP6

T-9120

