

SANYO**LA2000M****Audio Level Sensor**

Overview

LA2000M is an IC for detecting interprogram spaces to pick out the starting point of a program immediately preceding or following a musical program recorded on tape, and to detect end of tape.

Used in

- Radio-cassette recorders
- Cassette decks
- Car stereos

Applications

- Detection of spaces between programs recorded on tape
- Detection of end of tape
- Other

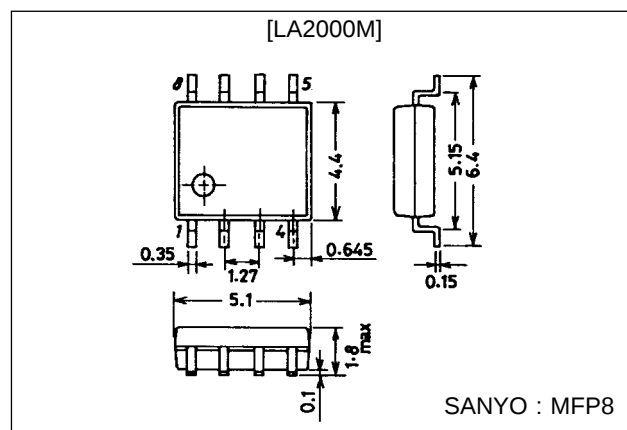
Features

- Has transistors capable of driving plungers with maximum 50 mA, and a protective diode to prevent induced reverse voltages.
- Can provide designated time delays by externally connected capacitors and resistors.
- Has a comparator with stable hysteresis to handle variations in power supply voltage.
- Detects unrecorded portions of tape.

Package Dimensions

unit : mm

3032B-MFP8



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		15	V
Allowable power dissipation	P _d max		300	mW
Flow-in current	I ₆ max		50	mA
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-40 to +125	°C

Note: 1. The voltage at pin 7 must not exceed the supply voltage at pin 8.
 2. The maximum current flowing into pin 7 should be no greater than 0.5 mA.

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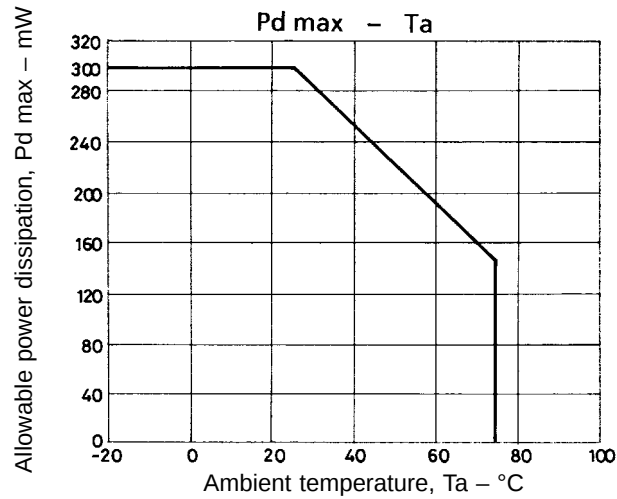
42896HA(II) No. 4158-1/8

Operating Conditions at $T_a = 25^\circ\text{C}$

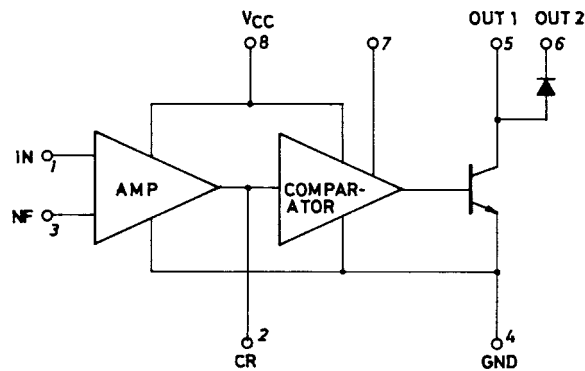
Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage	$V_{CC\text{ op}}$		3.5 to 14	V

Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 9.0\text{ V}$, $f = 1\text{ kHz}$

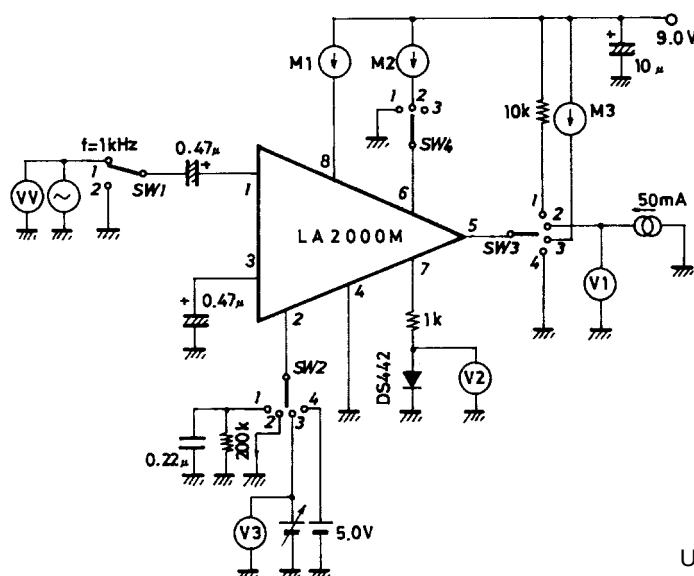
Parameter	Symbol	Conditions	min	typ	max	Unit
Circuit current	I_{CC}	$f = 1\text{ kHz}$, $V_{IN} = -45\text{ dBm}$		6	12	mA
Output transistor saturating voltage	$V_{CE\text{ (sat)}}$	$I_6 = 50\text{ mA}$		0.5	1.8	V
Output diode forward voltage	V_F	$I_F = 50\text{ mA}$		0.7	1.5	V
Output-off level in input equivalent	V_{IN}	$f = 1\text{ kHz}$	-43	-50	-54	dBm
Comparator-on level	V_{TH-H}		3.0	3.5	4.0	V
Comparator-off level	V_{TH-L}		1.8	2.2	2.6	V
Pin 7 high level	$V_7\text{ pin}$		0.45	0.55		V
Output transistor leakage current	I_{L-TR}				100	μA
Output diode leakage current	I_{L-Di}				100	μA



Equivalent Circuit Block Diagram



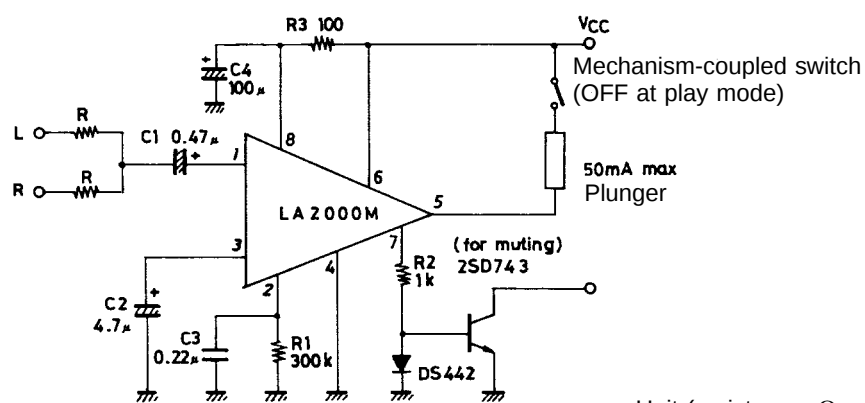
Test Circuit

Unit (resistance: Ω , capacitance: F)

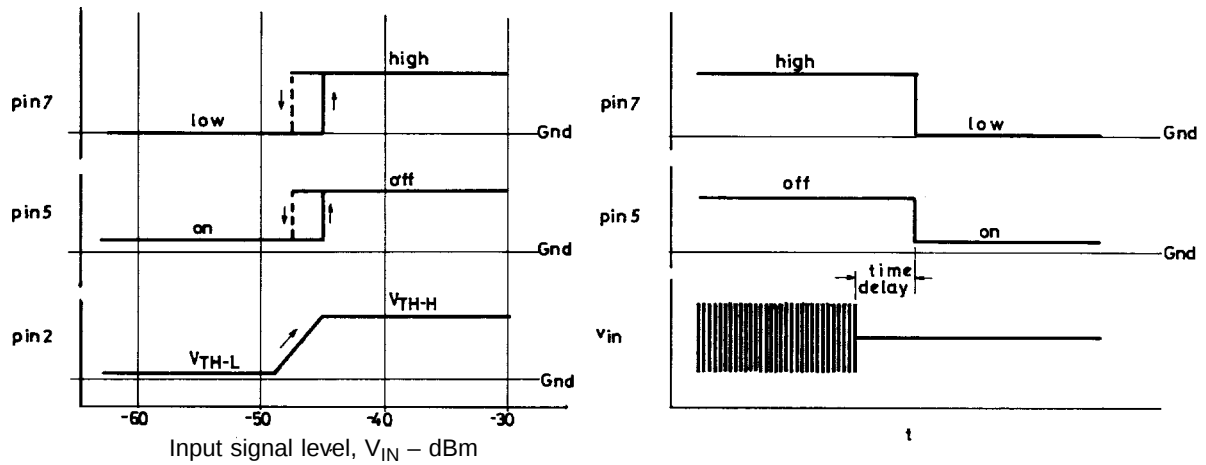
Test Conditions

Test items	Symbol	SW-1	SW-2	SW-3	SW-4	Conditions
Circuit current	I_{CC}	1	1	1	3	Measure current flowing into pin 8 at $V_{IN} = -45$ dB
Output transistor saturation voltage	$V_{CE(sat)}$	2	2	2	3	Measure V_{IN} at pin 5
Output diode forward voltage	V_F	2	4	2	1	Measure V_{IN} at pin 5
Output-off level in input equivalent	V_{IN}	1	1	1	3	Input level (v.v) when pin 5 turns over
Comparator-on level	V_H	2	3	1	3	Measure V_3 when pin 5 turns over
Comparator-off level	V_L	2	3	1	3	Measure V_3 when pin 5 turns over
Pin 7 high level	V_{p-7}	2	4	1	3	Measure V_2 at pin 7
Output transistor leakage current	I_{TL}	2	4	3	3	Measure M3
Output diode leakage current	I_{DL}	2	4	4	2	Measure M2

Sample Application Circuit 1

Unit (resistance: Ω , capacitance: F)

2. Individual pins and their operations



As shown above, when input level is raised and the pin 2 voltage reaches the V_{TH-H} level of the comparator, pins 5 and 7 turn over. ($V_{IN} = -45$ dBm).

- pin 5 is for driving plungers. When it is on the “L” side, pin 5 turns on and can draw current up to 50 mA maximum.
- Pin 6 is a diode that prevents reverse voltages induced when the plunger is turned off from on.
- Pin 7 functions in phase with pin 5 and can drive external transistors (such as for MUTE).

3. Time delays and obtaining CRs

When input signals that have been applied at a level not less than -45 dBm are removed, discharging occurs through the CR connected at pin 2, lowering pin 2 potential. A time delay is provided before the hysteresis comparator turns over.

$$\frac{E1}{E0} = - \frac{t}{e^{\tau}}$$

E0 : Initial voltage
E1 : Threshold voltage
 τ : Time constant

Accordingly,

$$t = -\tau \ln \frac{E1}{E0}$$

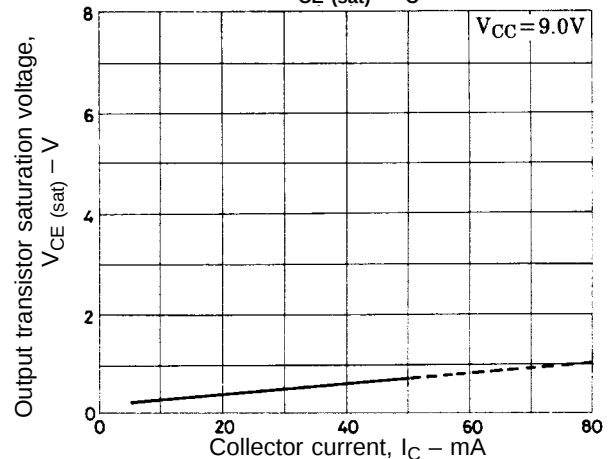
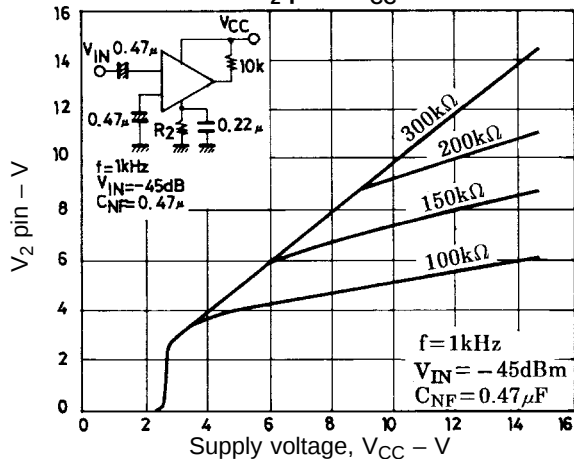
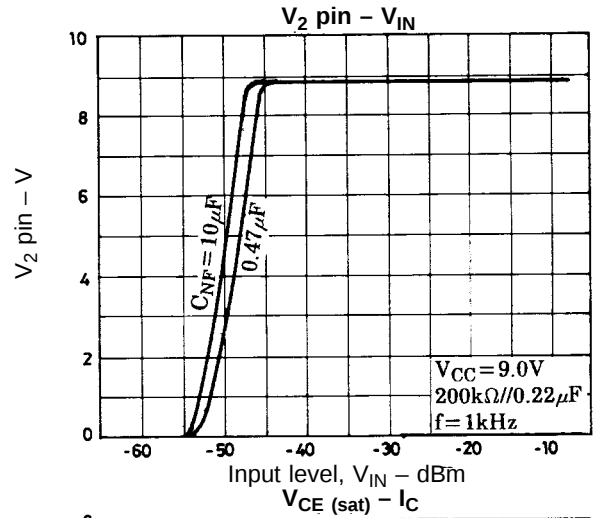
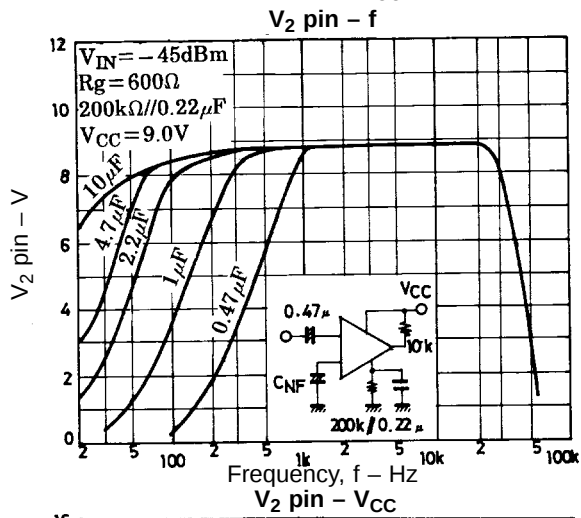
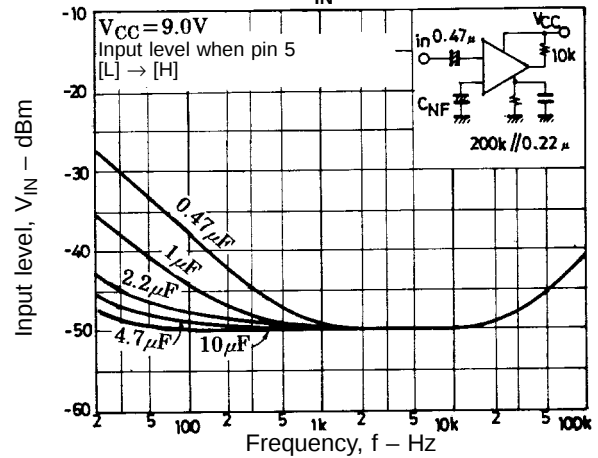
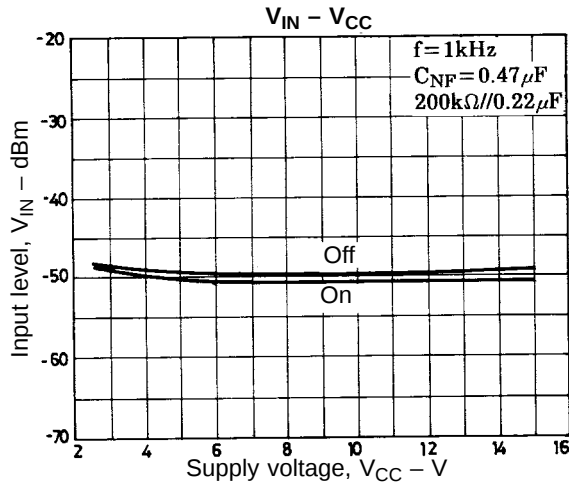
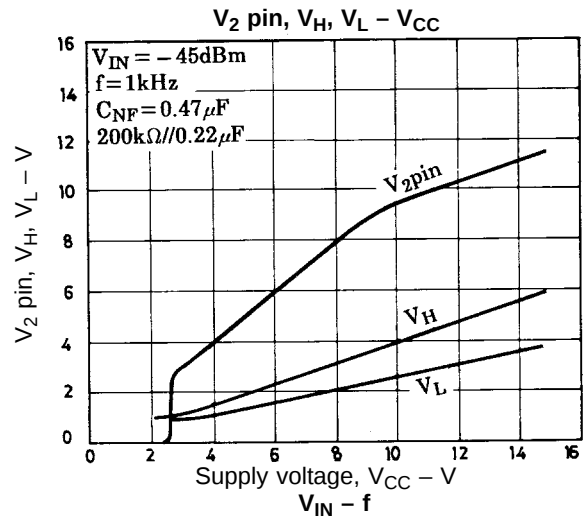
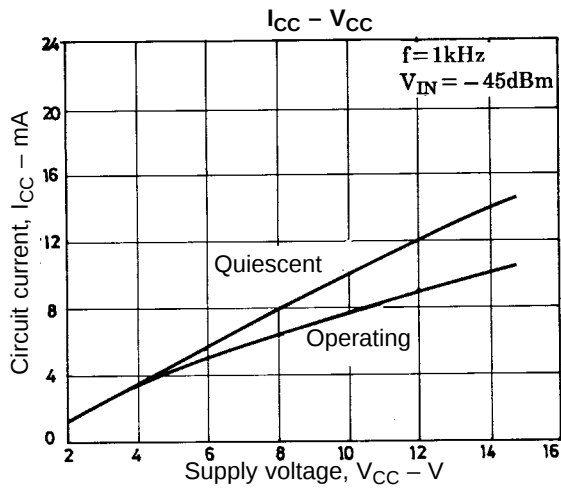
$E1/E0$, within the IC, is 0.26. A desired time delay is obtained by an appropriate choice of τ ($\tau = C_3R_1$). Therefore, the time delay is obtained by the following formula:

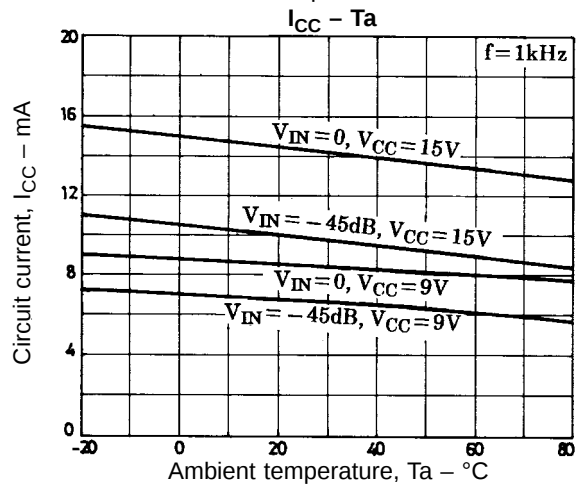
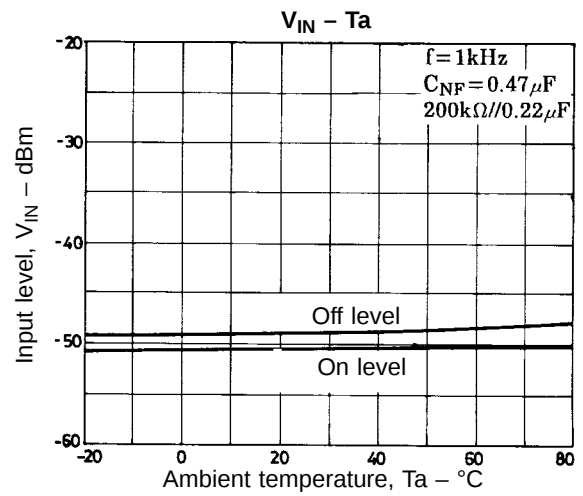
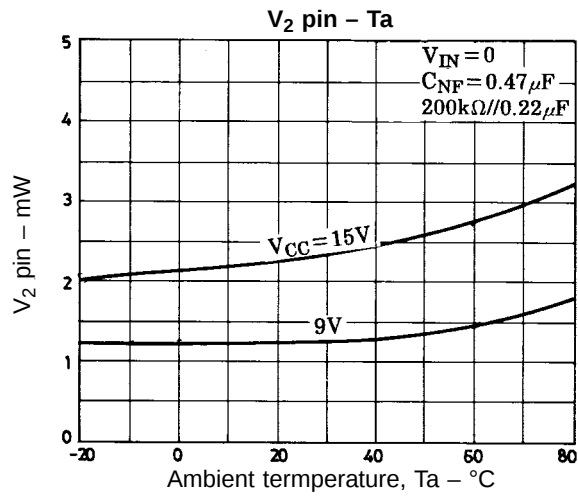
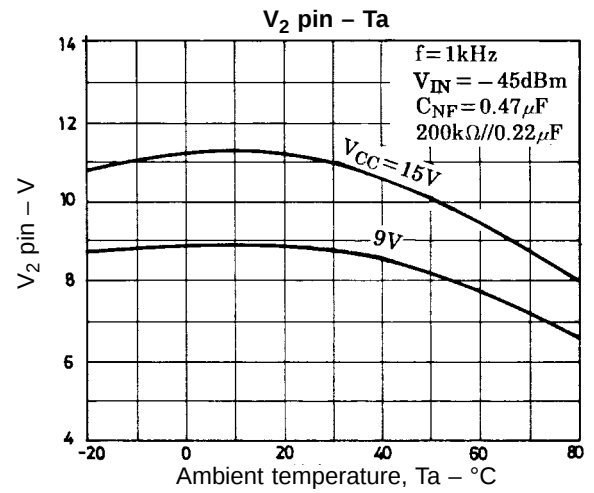
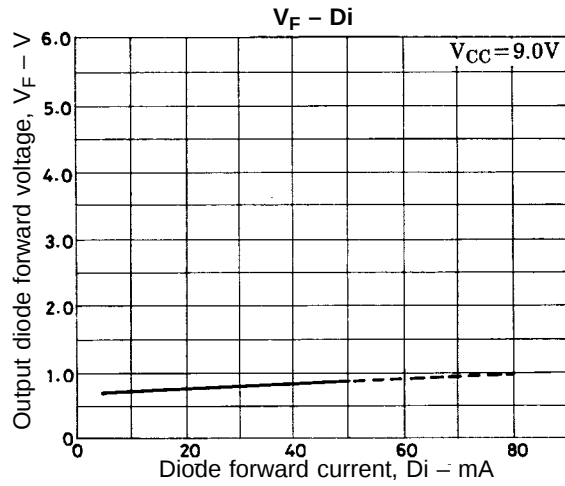
$$t = 1.34 \times C_3R_1 \text{ (sec)}$$

We recommend $150 \text{ k}\Omega$ to $500 \text{ k}\Omega$ for R when determining CR.

4. IC usage notes

- Maximum ratings
When maximum ratings are surpassed, destruction or deterioration may result.
- Interpin short circuits and reverse insertions
These cause destruction or deterioration of the IC: be careful when mounting on circuit board.
- Voltage applied to pin 7 should never exceed pin 8 voltage.
- The current flowing into pin 7 is to be 0.5 mA maximum.





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