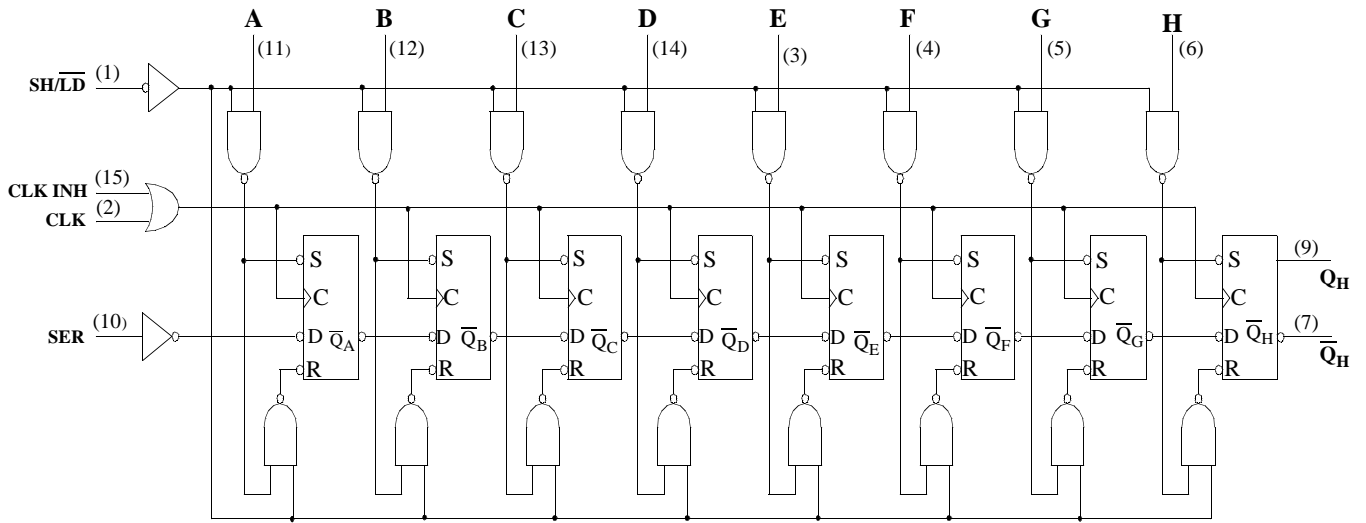


LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to $V_{DD} + .3$	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS ⁷(V_{DD} = 5.0V ±10%; V_{SS} = 0V ⁶, -55 °C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3V _{DD}	V
V _{IH}	High-level input voltage ¹ ACTS ACS		.5V _{DD} .7V _{DD}		V
I _{IN}	Input leakage current ACTS/ACS	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
V _{OL}	Low-level output voltage ³ ACTS ACS	I _{OL} = 8.0mA I _{OL} = 100μA		0.40 0.25	V
V _{OH}	High-level output voltage ³ ACTS ACS	I _{OH} = -8.0mA I _{OH} = -100μA	.7V _{DD} V _{DD} - 0.25		V
I _{OS}	Short-circuit output current ^{2,4} ACTS/ACS	V _O = V _{DD} and V _{SS}	-200	200	mA
I _{OL}	Output current ¹⁰ (Sink)	V _{IN} = V _{DD} or V _{SS} V _{OL} = 0.4V	8		mA
I _{OH}	Output current ¹⁰ (Source)	V _{IN} = V _{DD} or V _{SS} V _{OH} = V _{DD} - 0.4V	-8		mA
P _{total}	Power dissipation ^{2,8,9}	C _L = 50pF		2.9	mW/MHz
I _{DDQ}	Quiescent Supply Current	V _{DD} = 5.5V		10	μA
ΔI _{DDQ}	Quiescent Supply Current Delta ACTS	For input under test V _{IN} = V _{DD} - 2.1V For all other inputs V _{IN} = V _{DD} or V _{SS} V _{DD} = 5.5V		1.6	mA
C _{IN}	Input capacitance ⁵	f = 1MHz @ 0V		15	pF
C _{OUT}	Output capacitance ⁵	f = 1MHz @ 0V		15	pF

UT54ACS165/UT54ACTS165

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, $- 0\%$; $V_{IL} = V_{IL(max)} + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS ²(V_{DD} = 5.0V ±10%; V_{SS} = 0V ¹, -55 °C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PHL}	CLK or CLK INH to Q _H or \overline{Q}_H	2	21	ns
t _{PLH}	CLK or CLK INH to Q _H or \overline{Q}_H	2	18	ns
t _{PHL}	SH/ \overline{LD} to Q _H or \overline{Q}_H	2	21	ns
t _{PLH}	SH/ \overline{LD} to Q _H or \overline{Q}_H	2	18	ns
t _{PHL}	H to Q _H	2	21	ns
t _{PLH}	H to Q _H	2	17	ns
t _{PHL}	H to \overline{Q}_H	2	20	ns
t _{PLH}	H to \overline{Q}_H	2	18	ns
f _{MAX}	Maximum clock frequency		71	MHz
t _{SU1}	SER, SH/ \overline{LD} , CLKINH or CLK Setup time before CLK ↑ or CLK INH ↑	7		ns
t _{SU2}	Data setup time before SH/ \overline{LD}	7		ns
t _{H1}	SER hold time after CLK or CLK INH ↑	2		ns
t _{H2}	CLK INH hold time after CLK ↑	2		ns
t _{H3} ³	Hold time for any input after SH/ \overline{LD}	2		ns
t _w	Minimum pulse width CLK or CLK INH high CLK or CLK INH low SH/ \overline{LD}	7		ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Based on characterization, hold time (t_{H3}) of 0ns for data pins A-H, can be assumed if data setup time (t_{SU2}) is ≥ 10ns. This is guaranteed, but not tested.