UT54ACS169/UT54ACTS169

Radiation-Hardened
4-Bit Up-Down Binary Counters

FEATURES

- Fully synchronous operation for counting and programming
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Fully independent clock circuit
- 1.2µ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack

DESCRIPTION

The UT54ACS169 and the UT54ACTS169 are synchronous 4-bit binary counters that feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. Synchronous operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. The clock input triggers the four flip-flops on the rising (positive-going) edge of the clock.

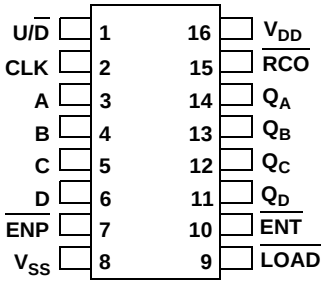
The counters are fully programmable (i.e., the outputs may each be preset high or low). The load input circuitry allows loading with the carry-enable output of cascaded counters. Loading is synchronous; applying a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascaded counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Assert both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output

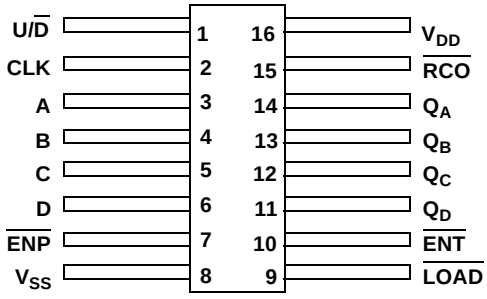
$\overline{RCO}$ enables a low-level pulse while the count is zero (all inputs low) counting down or maximum (15) counting up. The low-level overflow carry pulse can be used to enable successive cascaded stages.

PINOUTS

16-Pin DIP
Top View



16-Lead Flatpack
Top View

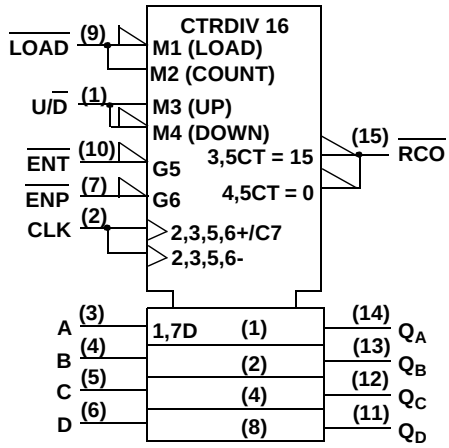


Transitions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input.

The counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The devices are characterized over full military temperature range of -55°C to +125°C.

LOGIC SYMBOL

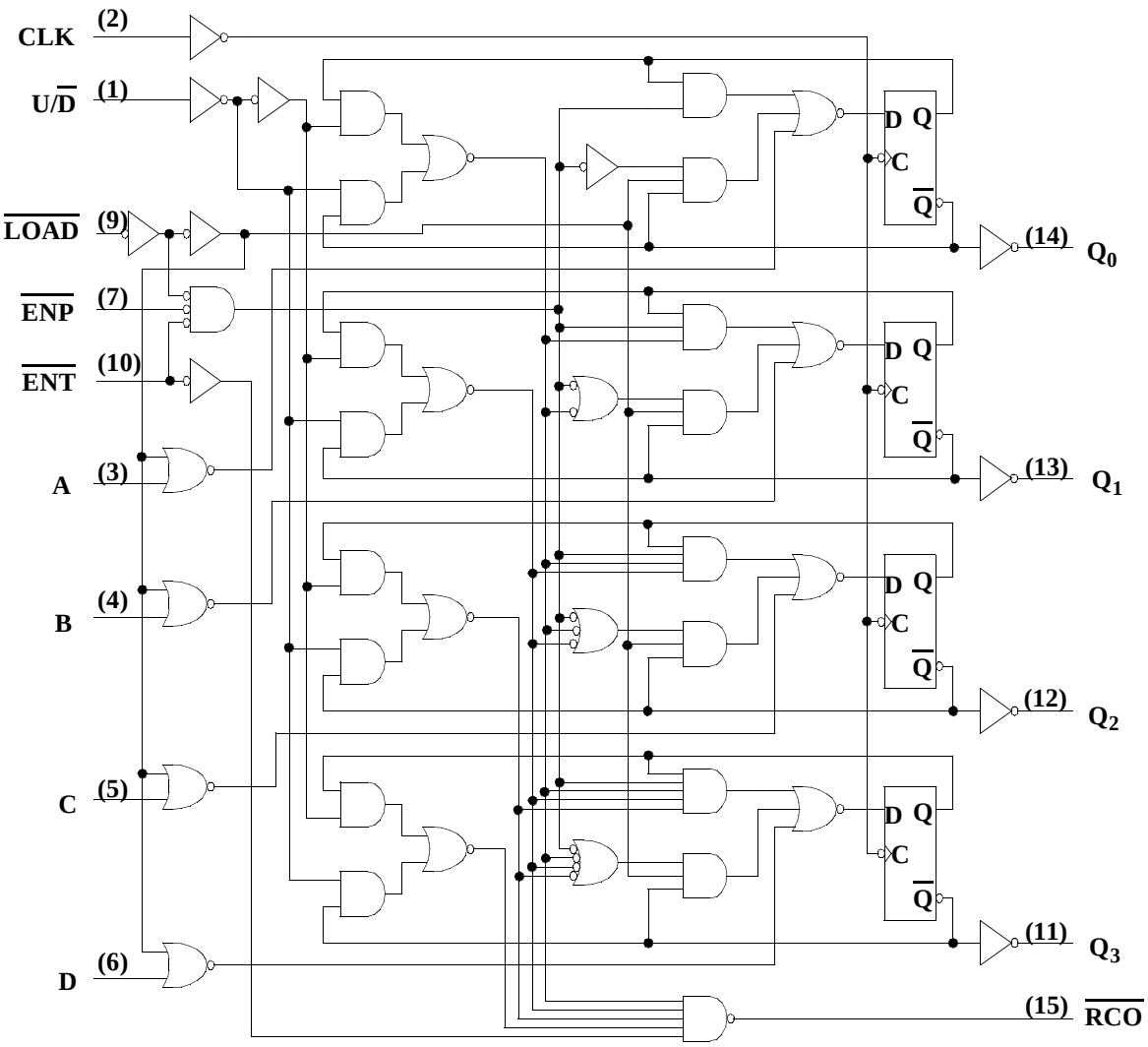


Note:
1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

OUTPUT	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	$U/\overline{D}$	CLK
Count Up	H	L	L	H	↑
Count Down	H	L	L	L	↑
Load Preset	L	X	X	X	↑
Inhibit	H H	H X	X H	X X	X X

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

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(V = 5.0V ±10%; V_{SS} = 0V 6, -55°C < T_C °C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage 1 ACTS ACS			0.8 .3V_{DD}	V
V_{IH}	High-level input voltage 1 ACTS ACS		.5V_{DD} .7V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	V_{IN} = V_{DD} or V_{SS}	-1	1	µ
V_{OL}	3 ACTS	I_{OL} I_{OL} µA		0.40 0.25	V
V_{OH}	High-level output voltage 3 ACTS ACS	I_{OH} = -8.0mA I_{OH} = -100µ	.7V_{DD} $_{DD}$-0.25		
I_{OS}	2,4	V_O $_{DD}$ and V	-200	200	
I_{OL}	10 (Sink)	$_{IN}$ = V or V_{SS} $_{OL}$ = 0.4V			mA
I	Output current10	V_{IN} $_{DD}$ or V V_{OH} $_{DD}$ - 0.4V			mA
P	Power dissipation 2, 8, 9	$_L$ = 50pF			mW/MHz
I	Quiescent Supply Current	V = 5.5V		10	µA
ΔI_{DDQ}	ACTS	For input under test $_{IN}$ = V - 2.1V For all other inputs $_{IN}$ = V or V_{SS} $_{DD}$ = 5.5V			mA
C	Input capacitance 5	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance 5	f = 1MHz @ 0V		15	

Notes:
1.Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose ≤ 1E6 rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	CLK to $\overline{RCO}$	2	23	ns
t_{PHL}	CLK to $\overline{RCO}$	4	28	ns
t_{PLH}	CLK to any Q	4	24	ns
t_{PHL}	CLK to any Q	4	24	ns
t_{PLH}	$\overline{ENT}$ to $\overline{RCO}$	1	15	ns
t_{PHL}	$\overline{ENT}$ to $\overline{RCO}$	2	16	ns
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$	2	16	ns
t_{PHL}	U/$\overline{D}$ to $\overline{RCO}$	2	16	ns
f_{MAX}	Maximum clock frequency		71	MHz
t_{SU1}	A, B, C, D setup time before CLK ↑	9		ns
t_{SU2}	$\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$, U/$\overline{D}$ Setup time before CLK ↑	9		ns
t_{H1}	Data hold time after CLK ↑	2		ns
t_{H2}	All synchronous inputs hold time after CLK ↑	2		ns
t_W	Minimum pulse width CLK high CLK low	7		ns

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Based on characterization, hold time (t_{H1}) of 0ns can be assumed if data setup time (t_{SU1}) is ≥10ns. This is guaranteed, but not tested.