

# UT54ACS245S

## Radiation-Hardened Schmitt Octal Bus Transceiver with Three-State Outputs

### FEATURES

- Three-state outputs drive bus line directly
- 1.2 $\mu$  radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 20-pin DIP
  - 20-lead flatpack

### DESCRIPTION

The UT54ACS245S is a non-inverting octal bus transceiver with Schmitt Trigger input levels. The circuit is designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ( $\overline{G}$ ) disables the device so that the buses are effectively isolated.

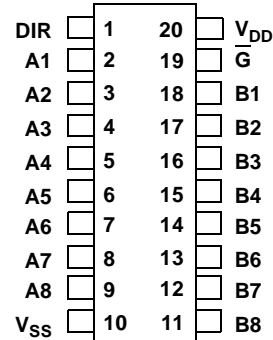
The device is characterized over full military temperature range of -55 $^{\circ}$ C to +125 $^{\circ}$ C.

### FUNCTION TABLE

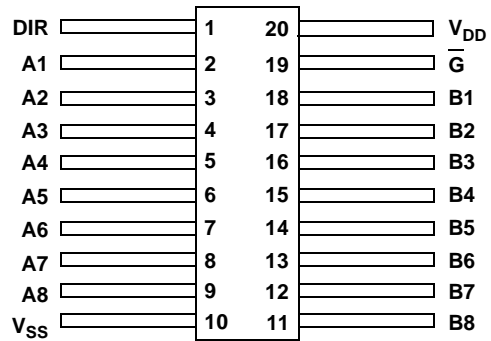
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

### PINOUTS

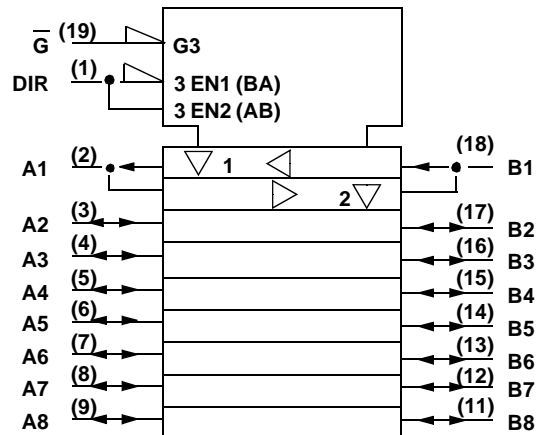
20-Pin DIP  
Top View



20-Lead Flatpack  
Top View



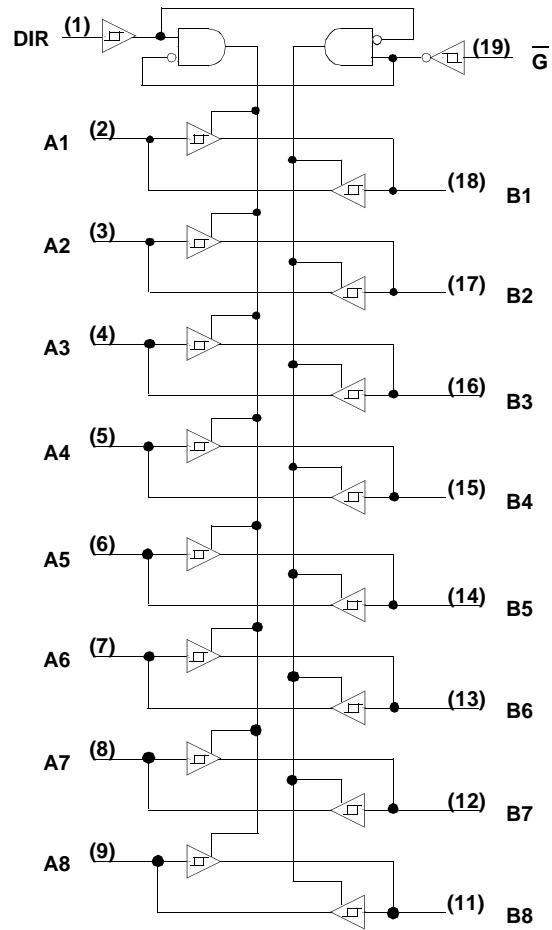
### LOGIC SYMBOL



**Note:**

1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



**RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>**

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
SEL Threshold <sup>3</sup>	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	4.5 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to + 125	°C

**DC ELECTRICAL CHARACTERISTICS**<sup>7</sup>(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V<sup>6</sup>, -55°C < T<sub>C</sub> < +125 °C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V <sub>T+</sub>	Schmitt Trigger, positive going threshold <sup>1</sup> ACS			.7V <sub>DD</sub>	V
V <sub>T-</sub>	Schmitt Trigger, negative going threshold <sup>1</sup> ACS		.3V <sub>DD</sub>		V
V <sub>H</sub>	Schmitt Trigger, typical range of hysteresis <sup>2</sup> ACS		0.6	1.5	V
I <sub>IN</sub>	Input leakage current ACS	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	1	μA
V <sub>OL</sub>	Low-level output voltage <sup>3</sup> ACS	I <sub>OL</sub> = 100μA		0.25	V
V <sub>OH</sub>	High-level output voltage <sup>3</sup> ACS	I <sub>OH</sub> = -100μA	V <sub>DD</sub> - 0.25		V
I <sub>OL</sub>	Output current (Sink) <sup>10</sup>	V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub> V <sub>OL</sub> =0.4V	12		mA
I <sub>OH</sub>	Output current (Source) <sup>10</sup>	V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub> V <sub>OH</sub> =V <sub>DD</sub> - 0.4	-12		mA
I <sub>OZ</sub>	Three-state output leakage current	V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>	-30	30	μA
I <sub>OS</sub>	Short-circuit output current <sup>2,4</sup> ACS	V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>	-300	300	mA
P <sub>total</sub>	Power dissipation <sup>2,8,9</sup>	C <sub>L</sub> = 50pF		2.0	mW/MHz
I <sub>DDQ</sub>	Quiescent Supply Current	V <sub>DD</sub> = 5.5V		10	μA
C <sub>IN</sub>	Input capacitance <sup>5</sup>	f = 1MHz @ 0V		15	pF
C <sub>OUT</sub>	Output capacitance <sup>5</sup>	f = 1MHz @ 0V		15	pF

## UT54ACS245S

### Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
2. Supplied as a design limit, but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. Guaranteed based on characterization data, but not tested.

**AC ELECTRICAL CHARACTERISTICS <sup>2</sup>**(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V <sup>1</sup>, -55 °C < T<sub>C</sub> < +125°C)

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MINIMUM</b>	<b>MAXIMUM</b>	<b>UNIT</b>
t <sub>PLH</sub>	Data to bus	2	15	ns
t <sub>PHL</sub>	Data to bus	2	15	ns
t <sub>PZL</sub>	$\overline{G}$ low to bus active	2	12	ns
t <sub>PZH</sub>	$\overline{G}$ low to bus active	2	12	ns
t <sub>PLZ</sub>	$\overline{G}$ high to bus three-state	2	15	ns
t <sub>PHZ</sub>	$\overline{G}$ high to bus three-state	2	15	ns

**Notes:**

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si)