



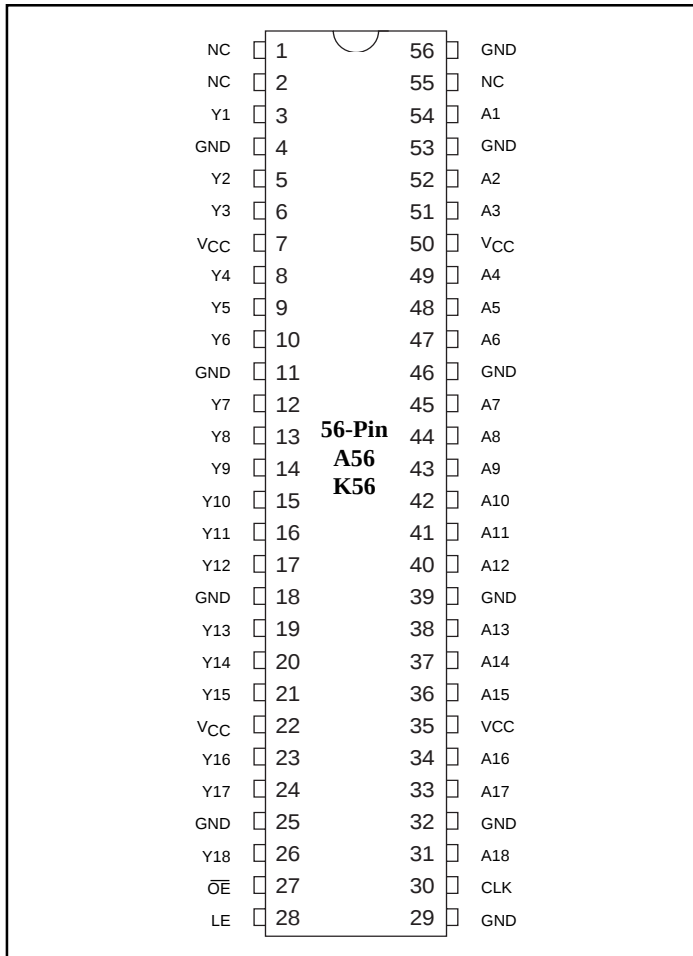
PI74AVC16835

18-Bit Universal Bus Driver with 3-State Outputs

Product Features

- Very high-speed, low-noise universal bus driver with embedded resistor outputs
- Meets PC133 SDRAM Registered DIMM specification
- Implements output impedance control for low-noise and heavy-load applications
- Fast Propagation Delay:
2.5ns max. for 50pF test load
- $V_{CC} = 3.3V$ or $2.5V$ or $1.8V$
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (K)

Product Pin Configuration



Product Description

Pericom Semiconductor's PI74AVC series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

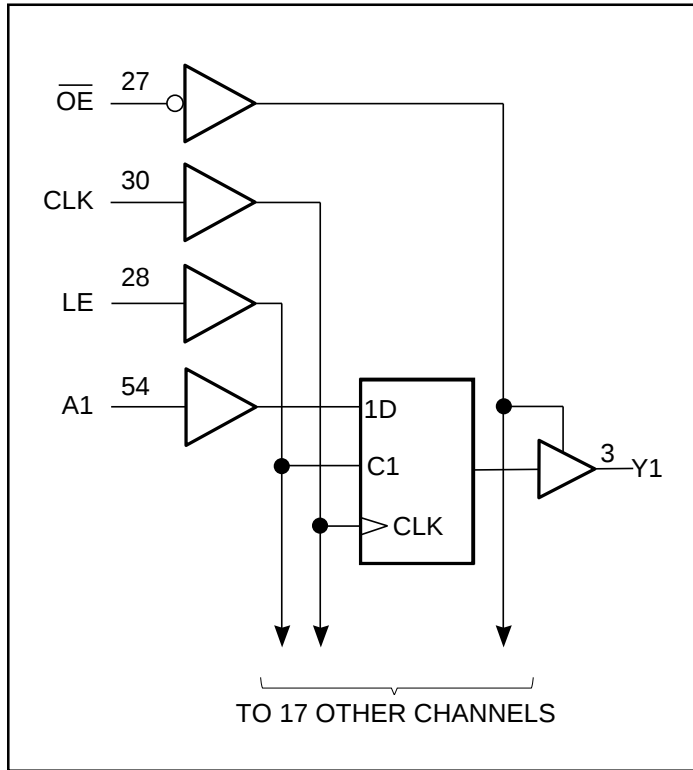
The 18-bit PI74AVC16835 universal bus driver is designed for 1.8V to 3.6V V_{CC} operation.

Data flow from A to Y is controlled by Output Enable ($\overline{OE}$). The device operates in the transparent mode when LE is HIGH. The A data is latched if CLK is held at a high or low logic level. If LE is LOW, the A-bus is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.

The PI74AVC16835 bus driver is designed to drive an array of 133 MHz synchronous memory chips, with minimal undershoot/overshoot noise, and to meet the input signal rise/fall time requirement of memory chips.

The output drivers of this part have an embedded series-resistor. For DIMM module design, no external series termination resistors near the buffer drivers or any other termination resistors are required. This feature simplifies DIMM module layout design, and results in cost savings.

Logic Block Diagram



Truth Table⁽¹⁾

Inputs				Outputs Y
OE	LE	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y ₀ ⁽²⁾
L	L	L	X	Y ₀ ⁽³⁾

Note:

- 1 H = High Signal Level
L = Low Signal Level
Z = High Impedance
↑ = Transition LOW-to-HIGH
X = Irrelevant
2. Output level before the indicated steady-state input conditions were established, provided that CLK is HIGH before LE goes LOW.
3. Output level before the indicated steady-state input conditions were established.

Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
LE	Latch Enable
CLK	Clock Input
A	Data Input
Y	Data Output
GND	Ground
VCC	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage Range, V_{CC}	-0.5V to +4.6V
Input Voltage Range, $V_I^{(1)}$	-0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, $V_O^{(1)}$	-0.5V to +4.6V
Voltage range applied to any output in the high or low state, $V_O^{(1,2)}$	-0.5V to $V_{CC} + 0.5V$
Input clamp current, I_{IK} ($V_I < 0$)	-50mA
Output clamp current, I_{OK} ($V_O < 0$)	-50mA
Continuous output current, I_O	±50mA
Continuous current through each V_{CC} or GND	±100mA
Package thermal impedance, $\theta_{JA}^{(3)}$: A (TSSOP) package	81°C/W
K (TVSOP) package	86°C/W

Note:

1. Input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.
2. Output positive voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. Package thermal impedance is calculated in accordance with JESD 51.

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions⁽¹⁾

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage	Operating	1.65	3.6	V
		Data Retention Only	1.2		
V_{IH}	High-level Input Voltage	$V_{CC} = 1.2V$	V_{CC}		
		$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3V$ to $2.7V$	1.7		
		$V_{CC} = 3V$ to $3.6V$	2		
V_{IL}	Low-level Input Voltage	$V_{CC} = 1.2V$		GND	
		$V_{CC} = 1.65V$ to $1.95V$		$0.35 \times V_{CC}$	
		$V_{CC} = 2.3V$ to $2.7V$		0.7	
		$V_{CC} = 3V$ to $3.6V$		0.8	
V_{IN}	Input Voltage		0	3.6	
V_{OUT}	Output Voltage	Active State	0	V_{CC}	
		3-State	0	3.6	
I_{OHS}	High-level Output Current ⁽²⁾	$V_{CC} = 1.65V$ to $1.95V$		-4	mA
		$V_{CC} = 2.3V$ to $2.7V$		-8	
		$V_{CC} = 3V$ to $3.6V$		-12	
I_{OLS}	Low-level Output Current ⁽²⁾	$V_{CC} = 1.65V$ to $1.95V$		4	
		$V_{CC} = 2.3V$ to $2.7V$		8	
		$V_{CC} = 3V$ to $3.6V$		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65V$ to $3.6V$		5	ns/V
T_A	Operating Free-Air Temperature		-40	85	°C

Note:

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. Dynamic drive is greater than standard output drive of $I_{OH} = -24mA$ and $I_{OL} = 24mA$

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$)

Parameters		Test Conditions		$V_{CC}^{(1)}$	Min.	Typ. ⁽²⁾	Max.	Units
V_{OH}		$I_{OHS} = -100\mu\text{A}$	V_{IH} or V_{IL}	1.65 to 3.6	$V_{CC} - 0.2$			V
		$I_{OHS} = -4\text{mA}$	$V_{IH} = 1.07\text{V}$	1.65	1.2			
		$I_{OHS} = -8\text{mA}$	$V_{IH} = 1.7\text{V}$	2.3	1.75			
		$I_{OHS} = -12\text{mA}$	$V_{IH} = 2\text{V}$	3.0	2.3			
V_{OL}		$I_{OLS} = 100\mu\text{A}$	V_{IH} or V_{IL}	1.65 to 3.6			0.2	V
		$I_{OLS} = 4\text{mA}$	$V_{IL} = 0.57\text{V}$	1.65			0.45	
		$I_{OLS} = 8\text{mA}$	$V_{IL} = 0.7\text{V}$	2.3			0.55	
		$I_{OLS} = 12\text{mA}$	$V_{IL} = 0.8\text{V}$	3.0			0.7	
I_I	Control Inputs	$V_I = V_{CC}$ or GND		3.6			2.5	μA
I_{OFF}		$V_I = 0$ or 3.6V		0			± 10	
$I_{OZ}^{(3)}$		$V_O = V_{CC}$ or GND	$\overline{OE} = V_{CC}$	3.6			± 10	
I_{CC}		$V_I = V_{CC}$ or GND	$I_O = 0$	3.6			40	
C_I	Control Inputs	$V_I = V_{CC}$ or GND		2.5		4.5		pF
				3.3		4.5		
	Data Input			2.5		4.0		
				3.3		4.0		
C_O	Outputs	$V_O = V_{CC}$ or GND		2.5		6.5		
				3.3		6.5		

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are measured at $+25^{\circ}\text{C}$.
3. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock Frequency		150		150		150	MHz
t_W Pulse Duration	LE High	2.0		1.2		1.0		ns
	CLK High or Low	2.0		1.2		1.0		
t_{SU} Setup time	Data before $\text{CLK} \uparrow$	1.4		1.2		1.0		
	Data before $\text{LE} \downarrow$, CLK High or Low	1.4		1.2		1.0		
t_H Hold time	Data after $\text{CLK} \uparrow$	1.0		0.8		0.6		
	Data after $\text{LE} \downarrow$, CLK High or Low	1.0		0.8		0.6		

Switching Characteristics Over Recommended Operating Free-Air Temperature Range

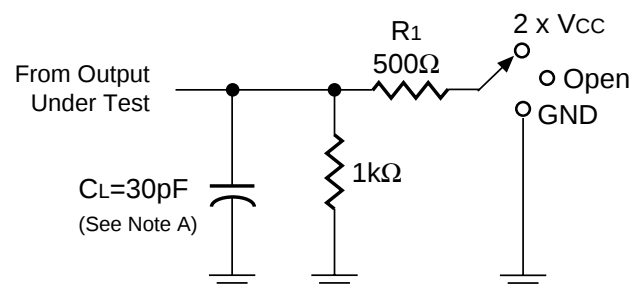
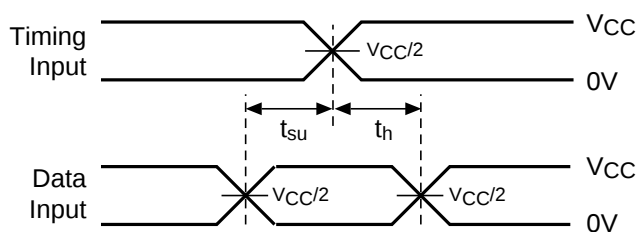
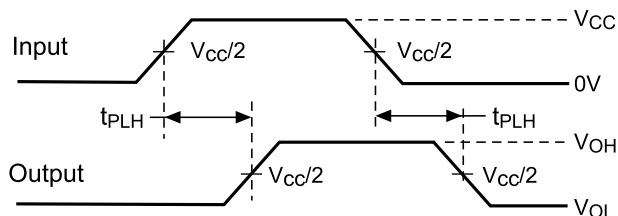
Unless otherwise noted, see Figures 3 through 5.

Parameter	From (Input)	To (Output)	V _{CC} = 1.8V ±0.15V		V _{CC} = 2.5V ±0.2V		V _{CC} = 3.3V ⁽¹⁾ ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f _{max}			150		150		150		MHz
t _{pd}	A	Y	1.0	4.5	0.8	3.0	0.7	2.4	ns
	LE		1.0	5.0	0.8	3.3	0.7	2.5	
	CLK		1.0	4.5	0.8	3.0	0.7	2.5	
t _{en}	$\overline{\text{OE}}$		1.5	5.5	1.0	4.5	1.0	4.0	
t _{DIS}	$\overline{\text{OE}}$		1.5	5.0	1.0	4.5	1.0	4.0	

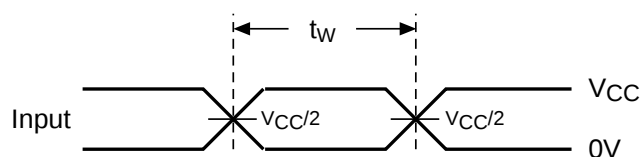
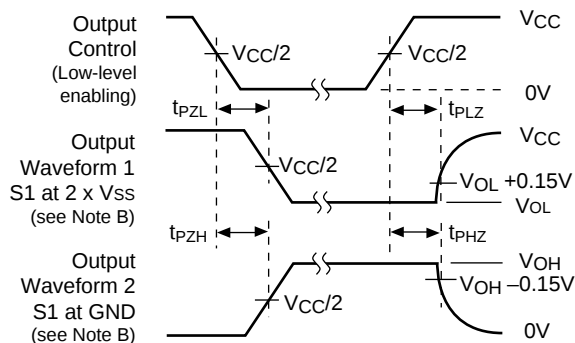
Note 1. Load at 50pF and 500Ω.

Operating Characteristics, T_A = 25°C

Parameters		Test Conditions	V _{CC} = 1.8V	V _{CC} = 2.5V	V _{CC} = 3.3V	Units
			Typ.	Typ.	Typ.	
C _{pd} Power dissipation capacitance	Outputs Enabled	C _L = 0, f = 10 MHz	45	48	52	pF
	Outputs Disabled		23	25	28	

Parameter Measurement Information ($V_{CC} = 1.8V \pm 0.15V$)

Load Circuit

**Voltage Waveforms
Setup and Hold Times**

**Voltage Waveforms
Propagation Delay Times**

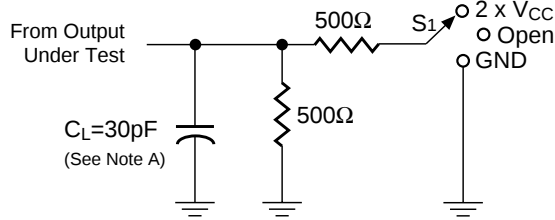
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND


**Voltage Waveforms
Pulse Duration**

**Voltage Waveforms
Enable and Disable Times**
Notes:

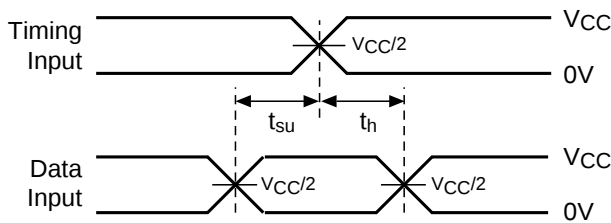
- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_r \leq 2ns$, $t_f \leq 2ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{dis} .
- t_{PLH} and t_{PHL} are the same as t_{dis} .

Figure 3. Load Circuit and Voltage Waveforms

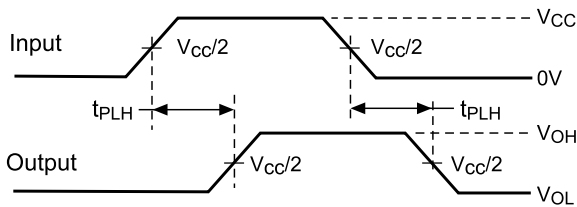
Parameter Measurement Information ($V_{CC} = 2.5V \pm 0.2V$)



Load Circuit

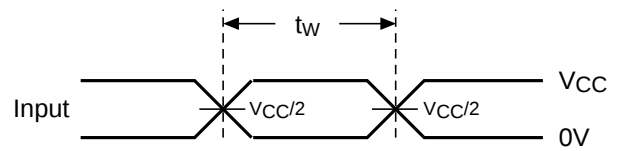


**Voltage Waveforms
Setup and Hold Times**

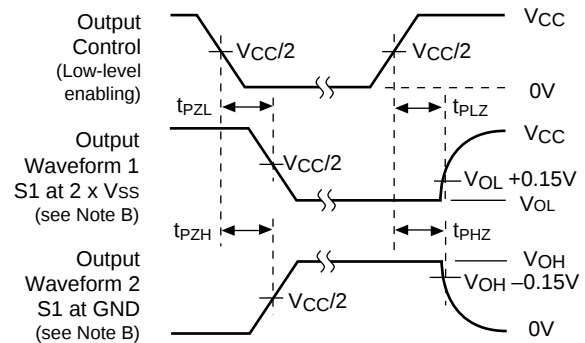


**Voltage Waveforms
Propagation Delay Times**

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND



**Voltage Waveforms
Pulse Duration**



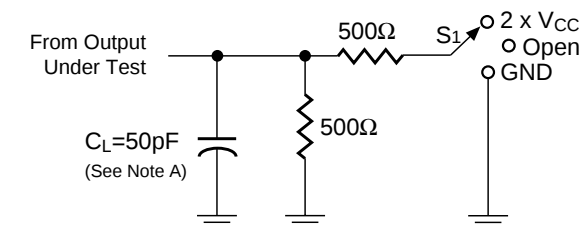
**Voltage Waveforms
Enable and Disable Times**

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_r \leq 2\text{ns}$, $t_f \leq 2\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{dis} .
- G. t_{PLH} and t_{PHL} are the same as t_{dis} .

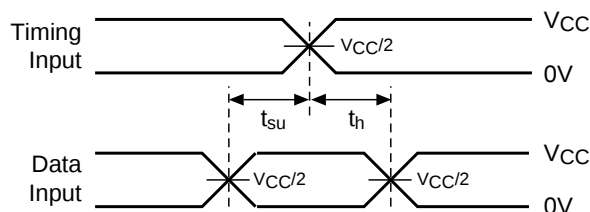
Figure 4. Load Circuit and Voltage Waveforms

Parameter Measurement Information ($V_{CC} = 3.3V \pm 0.3V$)

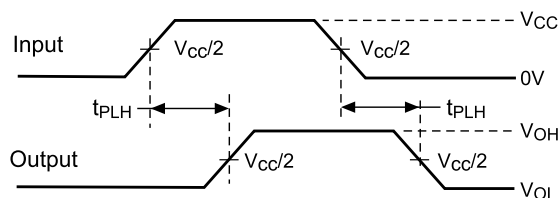


Load Circuit

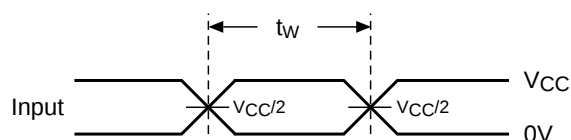
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND



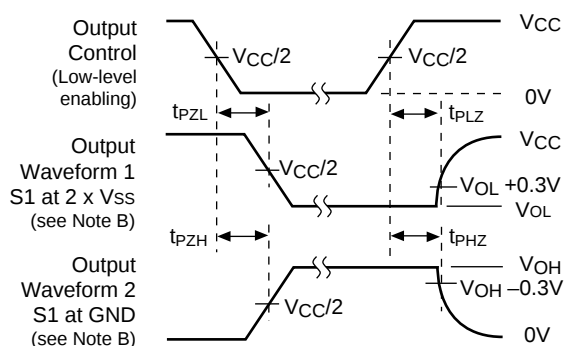
**Voltage Waveforms
Setup and Hold Times**



**Voltage Waveforms
Propagation Delay Times**



**Voltage Waveforms
Pulse Duration**



**Voltage Waveforms
Enable and Disable Times**

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50\Omega$, $t_r \leq 2ns$, $t_f \leq 2ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{dis} .
- t_{PLH} and t_{PHL} are the same as t_{dis} .

Figure 5. Load Circuit and Voltage Waveforms