Precision, Quad, SPST, Analog Switches

Features

- Low On-Resistance, (16–ohms typ)
  Minimizes Distortion and Error Voltages
- On-Resistance Match Between Channels, <2 ohms
- Guaranteed On-Resistance Flatness, <4 ohms
- Low Charge Injection, 3pC typ.
- Improved Leakage Over Temperature, <2.5nA at +85°C
- ESD Rating >2000V per Method 3015.7
- Single-Supply Operation (+3V to +15V)
- Bipolar-Supply Operation (±3V to ±8V)
- Low Power Consumption, <1µA
- TTL/CMOS Compatible

Applications

- Instrumentation
- Battery Powered Systems
- Audio Switching
- ±5V Data Acquisition Systems
- Sample-and-Hold Circuits
- Telecommunications Systems

Description

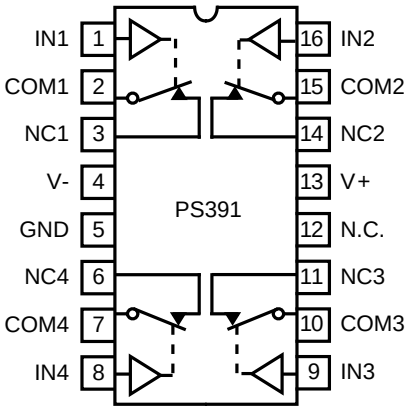
The PS391/ PS392/ PS393 are improved, quad, single-pole single-throw (SPST) analog switches designed to operate with ±3V to ±8V power supplies or a single 3V to 15V supply. The PS391 has four normally closed (NC) switches, the PS392 has four normally open (NO) switches. The PS393 has two NO and two NC switches. All three devices offer low leakage (<2pA typ) and fast switching speeds (t_{ON} <130ns). Power consumption is less than 1µA, ideal for battery-powered equipment.

With ±5V supplies, the PS391/PS392/PS393 guarantee <2ohm channel-to-channel matching, <30ohm on-resistance (R_{ON}), and <4ohm R_{ON} flatness over the specified range.

These switches are fully specified for single +5V operation, with <2ohm R_{ON} match, <45ohm R_{ON}, and <4ohm flatness.

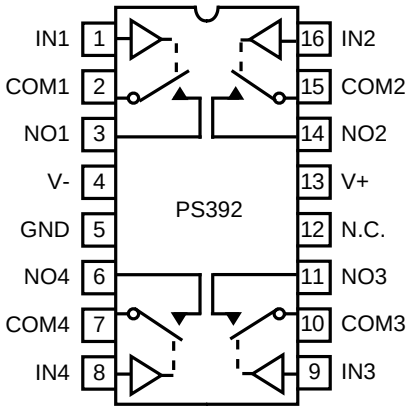
For operation below 5V, the PI5A391A/PI5A392A/PI5A393A are also recommended.

Functional Diagrams, Pin Configurations, and Truth Tables



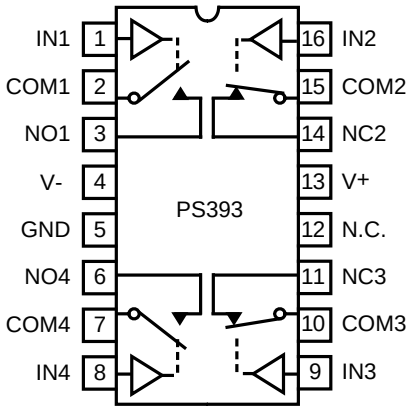
Top View

N.C. = No Connect.



Top View

Switches shown for logic "0" input



Top View

PS391	
Logic	**Switch**
0	ON
1	OFF

PS392	
Logic	**Switch**
0	OFF
1	ON

PS393		
Logic	**Switches 1,4**	**Switches 2,3**
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Voltages Referenced to V–
V+ ..... –0.3V to +17V
V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... (V–)–2V to (V+)+2V
or 30mA, whichever occurs first
Current (any terminal) 30mA
Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA
ESD per Method 3015.7 ..... >2000V

Thermal Information

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.5mW/°C above +70°C) 800mW
SO and QSOP (derate 8.7mW/°C above +70°C) 650mW
Storage Temperature ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note
Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +12V Supply

(V+ = 12V ±10%, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V+	V
On Resistance	R_{ON}	V+ = 12V, I_{COM} = 2mA, V_{NO} = 10V	25		16	45	ohm
			Full			55	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 12V, I_{COM} = 2mA V_{NO} = 10V	25		0.5	4	
			Full			6	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 12V, I_{COM} = 2mA, V_{NO} = 10V, 5V, 1V	25		2	4	
			Full			6	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 12V, V_{COM} = 0V, V_{NO} = 10V	25	–1		1	nA
			Full	–6		6	
COM Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 12V, V_{COM} = 0V, V_{NO} = 10V	25	–1		1	
			Full	–6		6	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 12V, V_{COM} = 10V, V_{NO} = 10V	25	–2		2	
			Full	–12		12	

Electrical Specifications - Single +12V Supply (continued)

(V+ = 12V ±10%, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Logic Input							
Input Current with Input Voltage High	I_{INH}	I_N = 5V, all others = 0.8V	Full	–0.5	0.005	0.5	µA
Input Current with Input Voltage Low	I_{INL}	I_N = 0.8V, all others =5V		–0.5	0.005	0.5	
Dynamic							
Turn-On Time	t_{ON}	V_{COM} = 10V, Figure 2	25		51	130	ns
			Full			175	
Turn-Off Time	t_{OFF}		25		17	75	
			Full			100	
On-Channel Bandwidth	BW	Signal = 0dbm Figure 4, 50ohm in and out	25		100		MHz
Charge Injection(3)	Q	C_L=1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3			3	10	pC
Off Isolation	O_{IRR}	R_L = 50ohm, C_L= 5pF, f = 1 MHz, Figure 4			–58		dB
Crosstalk(8)	X_{TALK}	R_L = 50ohm, C_L= 5pF, f = 1 MHz, Figure 5			–86		
NO Capacitance	$C_{(OFF)}$	f = 1 MHz, Figure 6			12		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1 MHz, Figure 6			12		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 7			25		
Positive Supply Current	I+	V_{IN} = 0V or V+, all channels on or off	Full	–1	0.001	1	µA
Total Harmonic Distortion	THD				0.03		%

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NO})], V_{COM} = 0utput, V_{NC} / V_{NO} = input to off switch
8. Between any two switches.

Electrical Specifications - Dual Supplies

(V+ = +5V ±10%, V– = –5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp°C	Min(2)	Typ(2)	Max(2)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	V–		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, V– = –4.5V, I_{COM} = –10mA, V_{NO} or V_{NC} = +3.5V	25		16	30	ohm
			Full			40	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 5.5V, V– = –5.5V, V_{COM} = –10mA, V_{NO} or V_{NC} = ±3.5V	25		0.2	2	
			Full			4	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$		25		1	4	
			Full			6	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NO(OFF)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	25	–0.1	–0.001	0.1	nA
			Full	–2.5		2.5	
COM Off Leakage Current(6)	$I_{COM(OFF)}$		25	–0.1	–0.001	0.1	
			Full	–2.5		2.5	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	25	–0.2	0.002	0.2	
			Full	–5		5	

Electrical Specifications - Dual Supplies (continued)

(V+ = +5V ±10%, V– = –5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp°C	Min(1)	Typ(2)	Max(1)	Units
Logic Input							
Input Current with Input Voltage High	I_{INH}	I_N = 2.4V, all others = 0.8V	Full	–0.5	0.005	0.5	µA
Input Current with Input Voltage Low	I_{INL}	I_N = 0.8V, all others = 2.4V					
Dynamic							
Turn-On-Time	t_{ON}	V_{COM} = ± 3V, Figure 1	25		51	130	ns
			Full			175	
Turn-Off-Time	$t_{(OFF)}$		25		29	75	
			Full			100	
Break-Before-Make Time Delay	t_D	PS393 only, R_L = 300ohm, C_L = 35pF, Figure 2	Full	10	20		
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0ohm, Figure 3	25		3	5	pC
Off Isolation	O_{IRR}	R_L = 50ohm, CL = 5pF, f = 1MHz, Figure 4			–65		dB
Crosstalk	X_{TALK}	R_L = 50ohm, CL = 5pF, f = 1MHz, Figure 5			–90		
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 6			12		pF
COM Off Capacitance	$C_{COM(OFF)}$				12		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 7			25		
Supply							
Positive Supply Range	V+, V–		Full	±3		±8	V
Positive Supply Current	I+	V+ = 5.5V, V– = –5.5V, V_{IN} = 0V or V+ All channels on or off		–1		1	µA
Negative Supply Current	I–						

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = Output, V_{NC} , V_{NO} = input to off switch
8. Between any two switches.

Electrical Specifications - Single 5V Supply

(V+ = +5V ±10%, V– = –5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Description	Parameter	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Switch Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, I_{COM} = –10mA, V_{NO} or V_{NC} = 3.5V	25		23	45	W
			Full			60	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 5V, I_{COM} = –1mA, V_{NO} or V_{NC} = 3V	25		0.3	2	
			Full			4	
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$	V+ = 5V, I_{COM} = –1mA, V_{NO} or V_{NC} = 1V, 4V	25		1	4	
			Full			6	
NO or NC Off Leakage Current(9)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25	–0.1	0.0004	0.1	nA
			Full	–2.5		2.5	
COM Off Leakage Current(9)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25	–0.1	0.001	0.1	
			Full	–2.5		2.5	
COM On Leakage Current(9)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 4.5V	25	–0.2	0.002	0.2	
			Full	–5		5	
Dynamic							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3V	25		63	170	ns
			Full			240	
Turn-Off Time	t_{OFF}		25		34	50	
			Full			100	
Break-Before-Make Time Delay(3)	t_D	PS393 only, R_L = 300ohm, C_L = 35pF	Full	10	20		
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 4	25		0	5	pC
Supply							
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V+, All channels on or off	Full	–1		1	mA
Negative Supply Current	I–						

Electrical Specifications - Single 3.3V Supply

(V+ = +3V to 3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

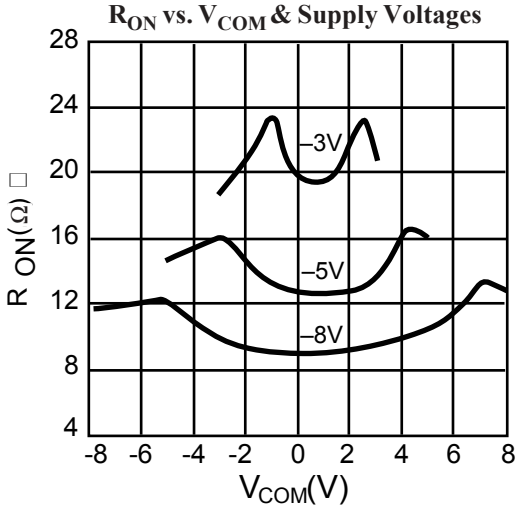
Description	Parameter	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Switch Range(3)	V_{ANALOG}		Full	0		V+	V
Channel On-Resistance	R_{ON}	V+ =3V, I_{COM} = –10mA, V_{NO} or V_{NC} = 1.5V	25		62	175	ohm
			Full			275	
Dynamic							
Turn-On-Time(3)	t_{ON}	V_{NO} or V_{NC} = 1.5V	25		97	400	ns
			Full			500	
Turn-Off-Time(3)	$t_{(OFF)}$		25		53	125	
			Full			175	
Break-Before-Make Time Delay(3)	t_D	PS393 only, R_L = 300ohm; C_L = 35pF	25	20			
Charge Injection(3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V	Full		1	5	pC
Supply							
Positive Supply Current	I+	V+ = 3.6V, V_{IN} = 0V or V+, All channels on or off	Full	–1		1	µA
Negative Supply Current	I–						

Notes:

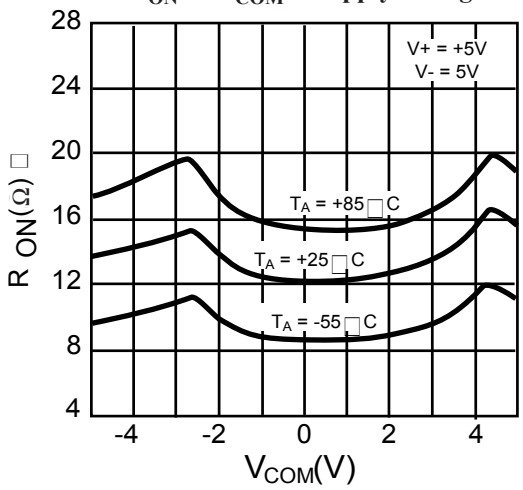
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}max - R_{ON}min$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}[V_{COM} / (V_{NC}$ or $V_{NO})]$, V_{COM} = Output, V_{NC}, V_{NO} = input to off switch
8. Between any two switches.
9. Leakage testing at single supply is guaranteed by testing with dual supplies.

Typical Operating Characteristics (T_A = +25ºC, unless otherwise noted)

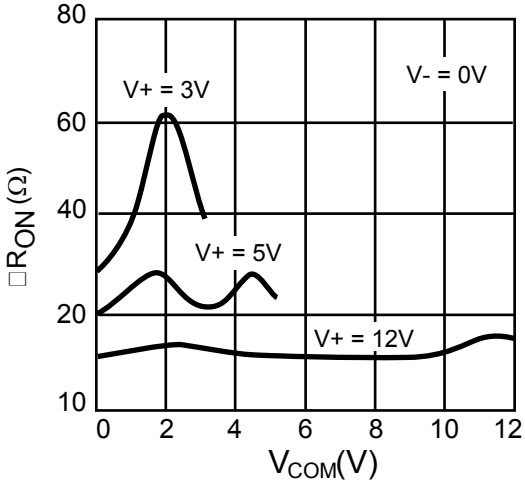
R_{ON} vs. V_{COM} & Supply Voltages



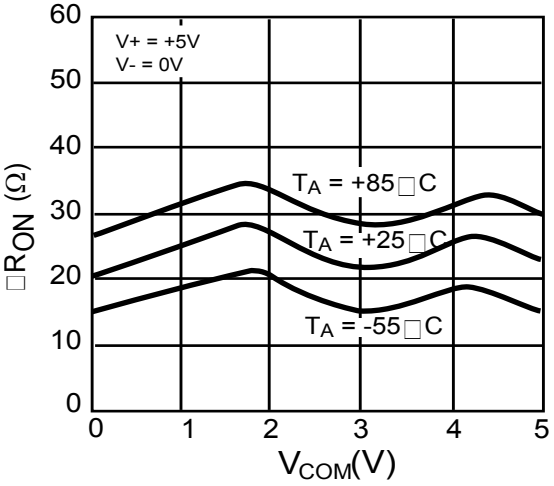
R_{ON} vs. V_{COM} & Supply Voltages



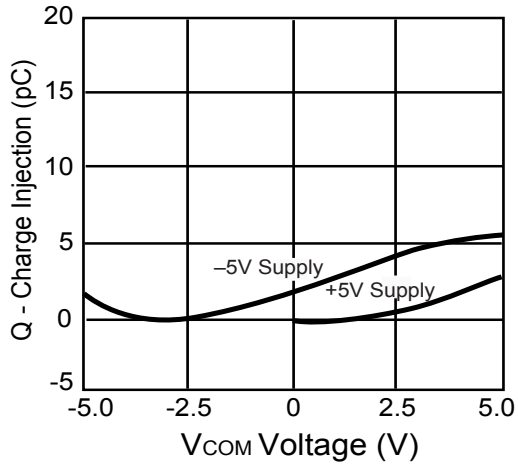
R_{ON} vs. V_{COM} (Single Supply)



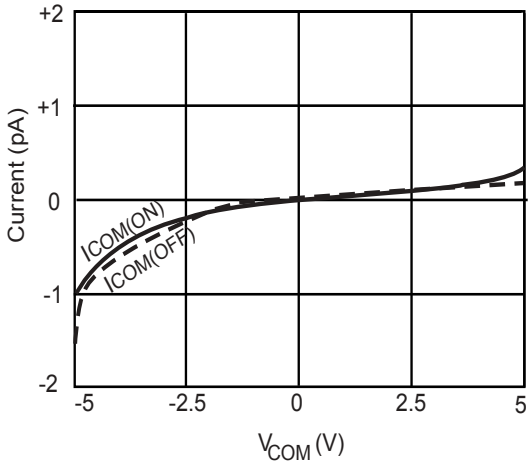
R_{ON} vs. V_{COM} and Temperature (Single Supply)



Charge Injection vs. Analog Voltage

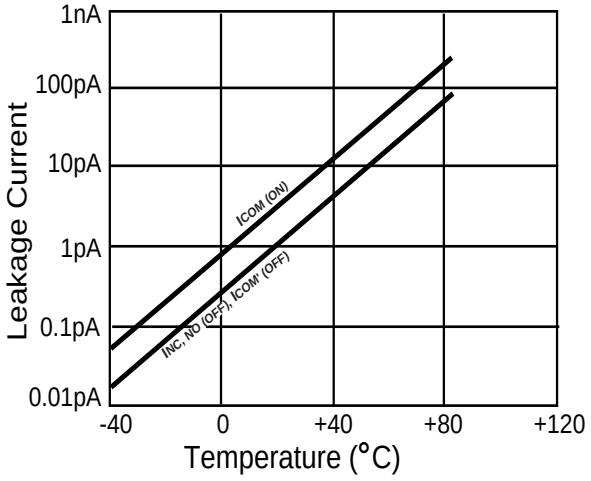


Leakage Current vs. V_{COM}

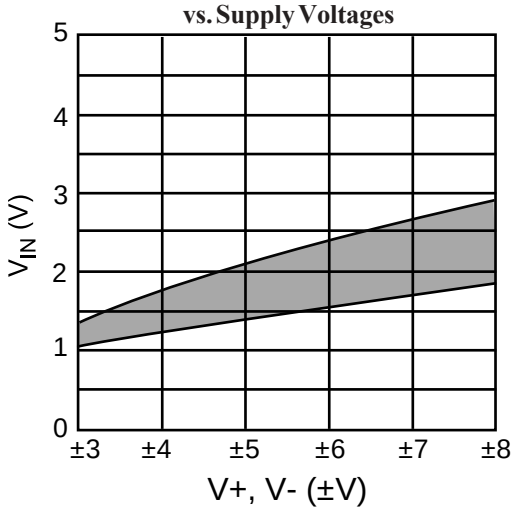


Typical Operating Characteristics (continued)

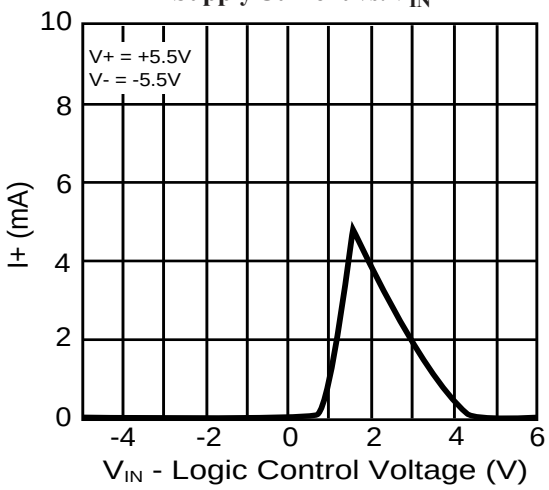
Leakage Current vs. Temperature



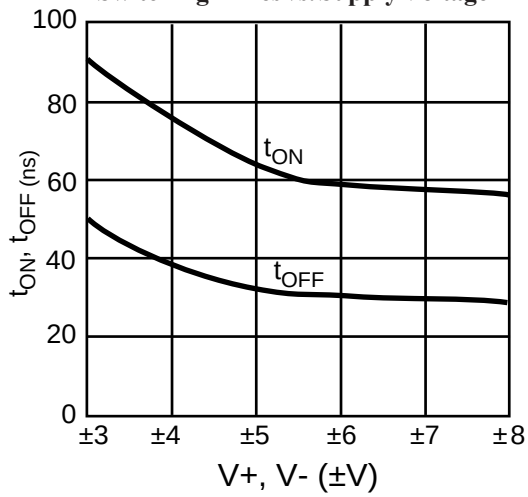
Input Switching Threshold vs. Supply Voltages



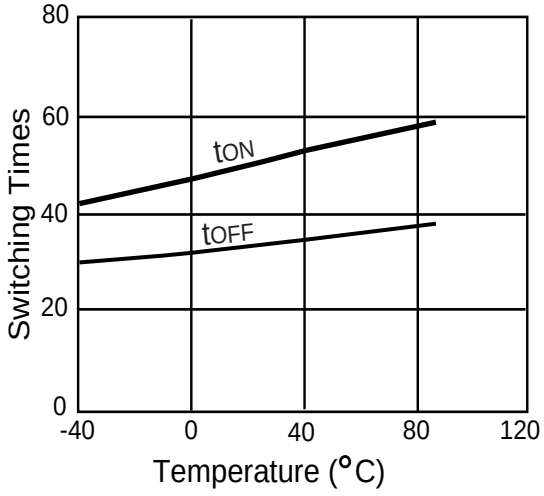
Supply Current vs. V_{IN}



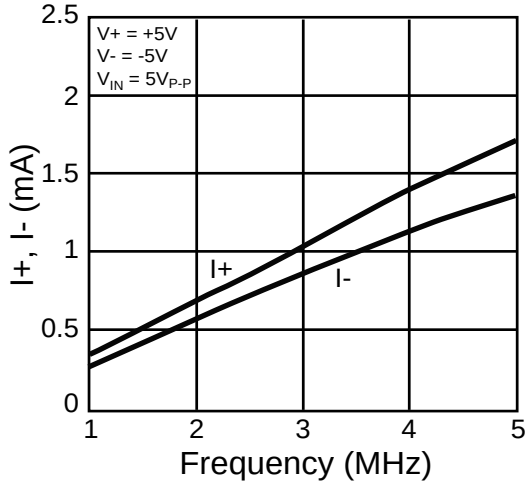
Switching Times vs. Supply Voltage



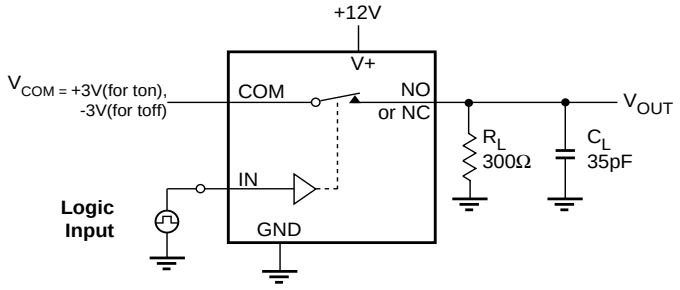
Switching Times vs. Temperature

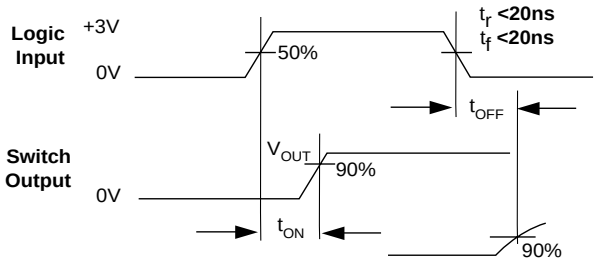


Supply Currents vs. Switching Frequency



Test Circuits/Timing Diagrams



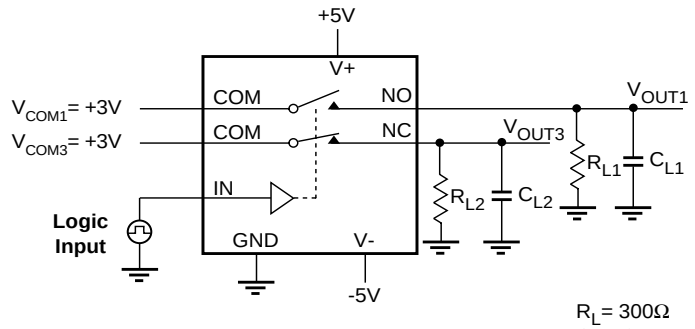


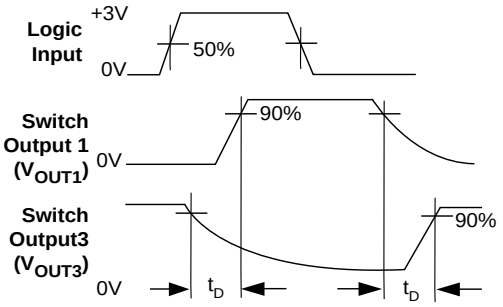
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC

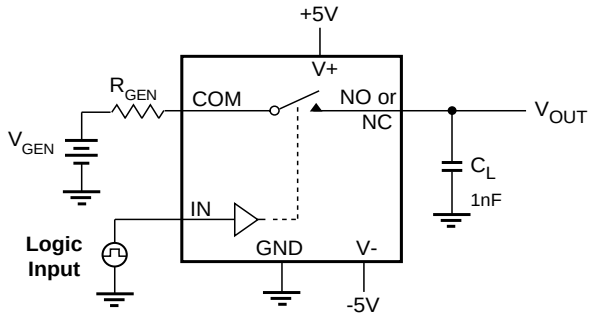
Figure 1. Switching Time

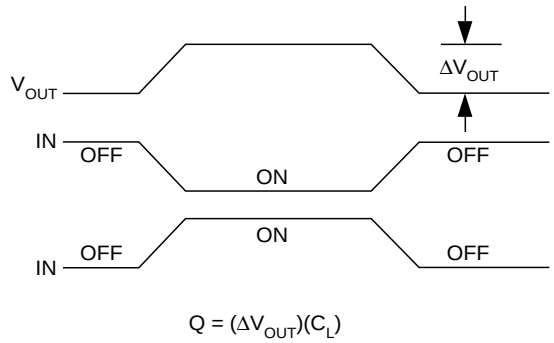




C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

Figure 2. Break-Before-Make Interval (PS393 only)





$$Q = (\Delta V_{OUT})(C_L)$$

Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

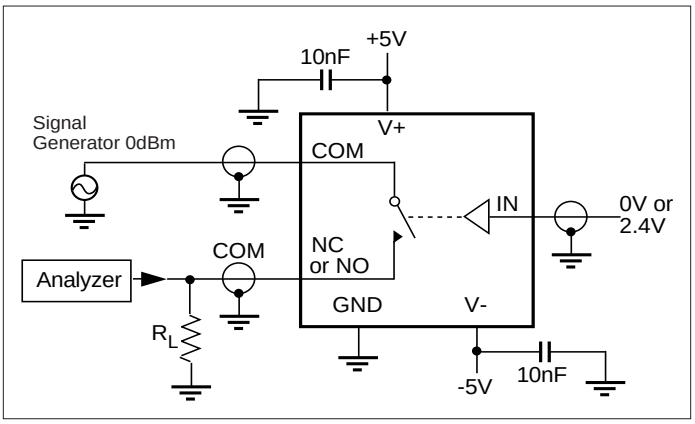


Figure 4. Off Isolation

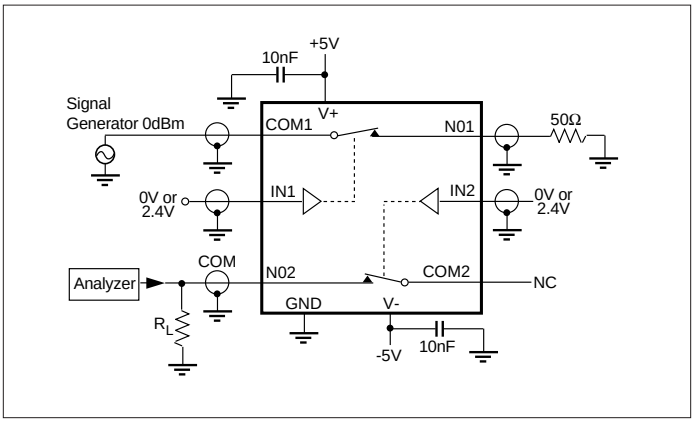


Figure 5. Crosstalk

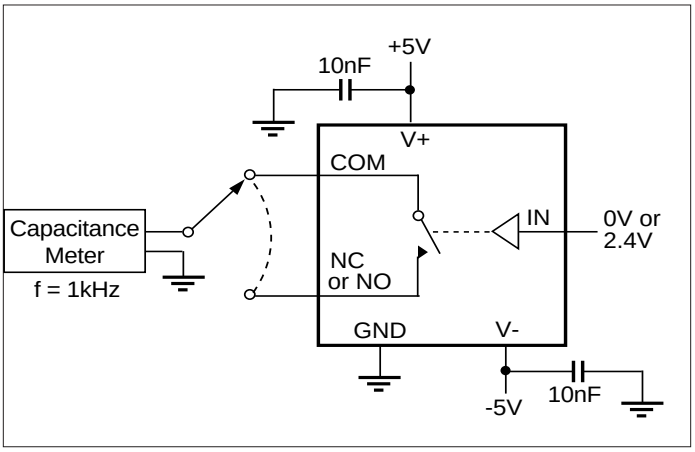


Figure 6. Channel-Off Capacitance

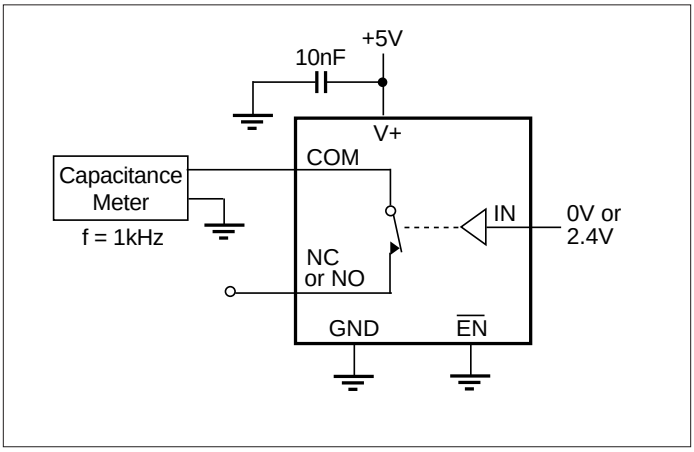


Figure 7. Channel-On Capacitance

Applications

As illustrated in Figure 8, PS391 can be used to insert various capacitors (C1, C2) and set proper RC times for integration. The resistors R1 and R2 set initial gain. The R_{IN} resistor x C1 or C2 sets the RC time. The reset switch discharges the hold capacitor through R_{IN}.

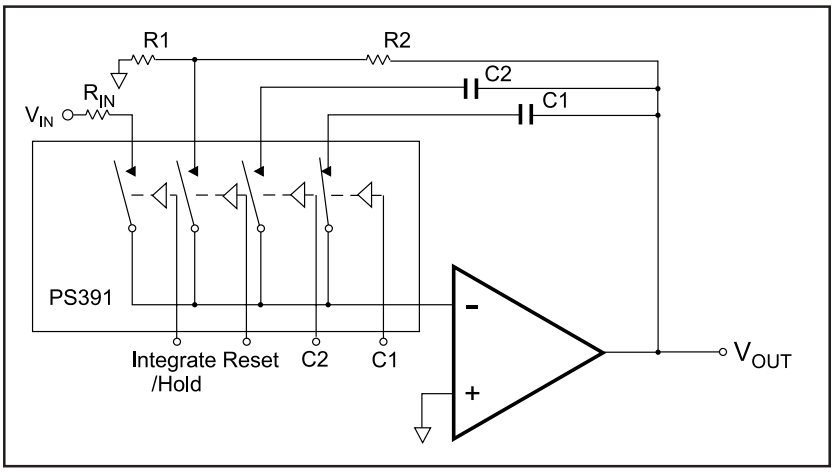


Figure 8. Programmable Integrator and Sample/Hold

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then the logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 9). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

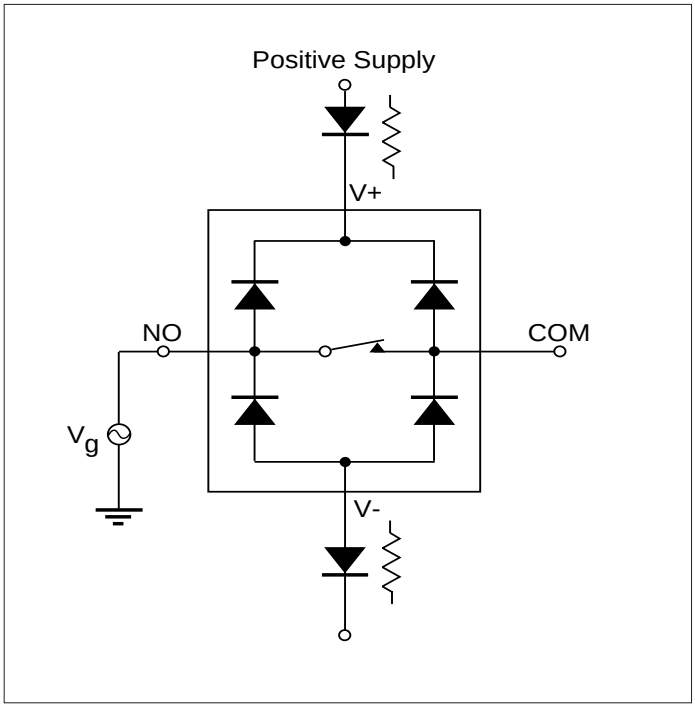


Figure 9. Overvoltage protection is accomplished using two external blocking diodes or two current limiting resistors.

Ordering Information

Part Number	Temperature Range	Package
PS391CPE	0ºC to + 70ºC	16 Ld PDIP
PS391CSE	0ºC to + 70ºC	16 Narrow SOIC
PS391EPE	–40ºC to + 85ºC	16 Ld PDIP
PS391ESE	–40ºC to + 85ºC	16 Narrow SOIC
PS391EEE	–40ºC to + 85ºC	16 QSOP
PS392CPE	0ºC to + 70ºC	16 Ld PDIP
PS392CSE	0ºC to + 70ºC	16 Narrow SOIC
PS392EPE	–40ºC to + 85ºC	16 Ld PDIP
PS392ESE	–40ºC to + 85ºC	16 Narrow SOIC
PS392EEE	–40ºC to + 85ºC	16 QSOP
PS393CPE	0ºC to + 70ºC	16 Ld PDIP
PS393CSE	0ºC to + 70ºC	16 Narrow SOIC
PS393EPE	–40ºC to + 85ºC	16 Ld PDIP
PS393ESE	–40ºC to + 85ºC	16 Narrow SOIC
PS393EEE	v40ºC to + 85ºC	16 QSOP