Precision 8-Ch, Diff. 4-Ch, 17V Analog Multiplexers

Features

- Low On-Resistance (60Ω typ.) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors and Improves Settling Times. Charge Injection: <5pC
- Split-Supply Operation (+3V to +8V)
- Improved Second Sources for MAX398/MAX399
- On-Resistance Matching Between Channels: <6Ω
- On-Resistance Flatness: <11Ω
- Low Off-Channel Leakage, $I_{NO(OFF)}$ < 1nA @ +85°C, $I_{COM(ON)}$, <2.5nA @ +85°C
- TTL/CMOS Logic Compatible
- Fast Switching Speed, t_{TRANS} <250ns
- Break-Before-Make action eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Range
- Low Power Consumption, <300µW
- Narrow SOIC and QSOP Packages Minimize Board Area

Applications

- Data Acquisition Systems
- Audio Switching and Routing
- Test Equipment
- PBX, PABX
- Telecommunication Systems
- Battery-Powered Systems

Description

The PS398/PS399 are improved high precision analog multiplexers. The PS398, an 8-channel single-ended mux, selects one of eight inputs to a common output as determined by a 3-bit address A0-A2. An EN (enable) pin when low disables all switches, useful when stacking several devices. The PS399 is a 4-channel differential multiplexer. It selects one of four differential inputs to a common differential output as determined by a 2-bit address A0, A1. An EN pin may be driven low to disable all switches.

These multiplexers operate with dual supplies from +3V to +8V. Single-supply operation is possible from +3V to +15V.

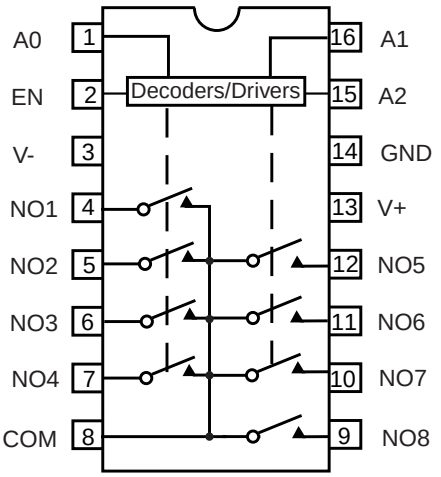
With +5V power supplies, the PS398/PS399 guarantee <100Ω on-resistance. On-resistance matching between channels is within 6Ω. On-resistance flatness is less than 11Ω over the specified signal range.

Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

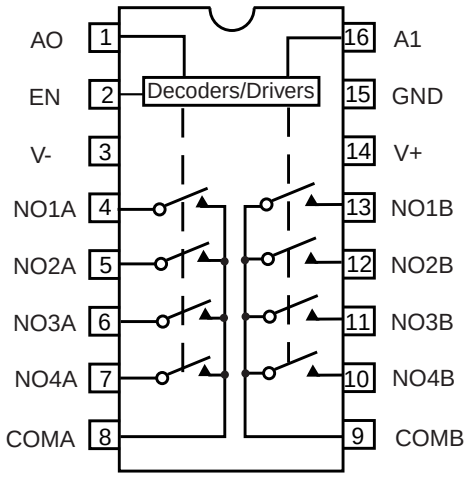
Both devices guarantee low leakage currents (<2.5nA at +85°C) and fast switching speeds (t_{TRANS} <250ns). Break-before-make switching action protects against momentary crosstalk between channels.

Functional Block Diagrams and Pin Configurations

Top View
PS398



Top View
PS399



Truth Tables

PS398				
A2	**A1**	**A0**	**EN**	**On Switch**
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

PS399			
A1	**A0**	**EN**	**ON Switch**
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0", $V_{AL} \leq 0.8V$
Logic "1", $V_{AH} \geq 2.4V$

Ordering Information

Part Number	Temperature Range	Package
PS398CPE	0°C to +70°C	16 Plastic DIP
PS398CSE	0°C to +70°C	16 Narrow SO
PS398EPE	-40°C to +85°C	16 Plastic DIP
PS398ESE	-40°C to +85°C	16 Narrow SO
PS398EEE	-40°C to +85°C	16 QSOP

Part Number	Temperature Range	Package
PS399CPE	0°C to +70°C	16 Plastic DIP
PS399CSE	0°C to +70°C	16 Narrow SO
PS399EPE	-40°C to +85°C	16 Plastic DIP
PS399ESE	-40°C to +85°C	16 Narrow SO
PS399EEE	-40°C to +85°C	16 QSOP

Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... -0.3V to + 17V

GND ..... -0.3V to + 17V

GND ..... -0.3V to (V+) + 0.3V

V_{IN}, V_{COM}, V_{NO} (Note 1) ..... (V-) -2V to (V+) + 2V or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC

(pulsed at 1ms, 10% duty cycle) 100mA

ESD per method 3015.7 ..... > 2000V

Thermal Information

Continuous Power Dissipation

Plastic DIP (derate 10.5mW/ °C above +70°C) 800mW

Narrow SO and QSOP(derate 8.7mW/ °C above +70°C)650mW

Storage Temperature ..... –65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1:

Signals on NO, COM, or logic inputs exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Dual Supplies ($V\pm = \pm5V \pm 10\%$, GND = 0V, $V_{AH} = V_{ENH} = 2.4V$, $V_{AL} = V_{ENL} = 0.8V$)

Parameter	Symbol	Conditions		Temp. (°C)	Min.(2)	Typ.(1)	Max.(2)	Units
Analog Switch								
Analog Signal Range (3)	V_{ANALOG}			Full	V-		V+	V
On Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, V_{COM} = ±3.5V I_{NO} = 1mA,		25		60	100	Ω
				Full			125	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{COM} or V_{NC} = ±3.5V, I_{NO} = 1mA, V+ = 5V, V- = -5V		25			6	
				Full			8	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V, 0V		25			11	
				Full			14	
NO Off Leakage Current(6)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} = ±4.5V		25	-0.1		0.1	nA
				Full	-1.0		1.0	
COM-Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V V_{COM} = ± 4.5V, V_{NO} = -/+4.5V	PS398	25	-0.2		50	
				Full	-2.5		100	
			PS399	25	-0.1		50	
				Full	-1.5		100	
COM On Leakage Current(7)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V V_{COM} = ±4.5V V_{NO} = 4.5V	PS398	25	-0.4		0.4	
				Full	-5		5	
			PS399	25	-0.2		0.2	
				Full	-2.5		2.5	
Logic Input								
Logic High Input Voltage	V_{AH}, V_{ENH}			Full	2.4			V
Logic Low Input Voltage	V_{AL}, V_{ENL}						0.8	
Input Current with Input Voltage High	I_{AH}, I_{ENH}	$V_A = V_{EN}$ = 2.4V			-0.1		0.1	µA
Input Current with Input Voltage Low	I_{AL}, I_{ENL}	$V_A = V_{EN}$ = 0.8V			-0.1		0.1	

Electrical Specifications - Dual Supplies ($V\pm = \pm5V \pm 10\%$, GND = 0V, $V_{AH} = V_{ENH} = 2.4V$, $V_{AL} = V_{ENL} = 0.8V$) **(continued)**

Parameter	Symbol	Conditions		Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Dynamic								
Transition Time	t_{TRANS}	Figure 1					150	ns
Break-Before-Make Time Delay	t_{OPEN}	Figure 3			0	40		
Enable Turn-OnTime	$t_{ON(EN)}$	Figure 2		25		72	150	
				Full			250	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 2		25		55	150	
				Full			200	
Charge Injection(3)	Q	C_L= 1nF, V_S = 0V, R_S = 0Ω,		25		2.8	5	pC
Off Isolation(7)	OIRR	V_{EN} = 0V, R_L= 1kΩ, f = 100kHz				-101		dB
Crosstalk	X_{TALK}	R_L = 1kΩ, f = 100kHz, Figure 6				-92		
Logic Input Capacitance	C_{IN}	f=1MHz				2.5		pF
NO Off Capacitance	$C_{NO(OFF)}$	f=1MHz, $V_{EN} = V_{NO}$ = 0V				3.6		
COM Off Capacitance	$C_{COM(OFF)}$	f=1MHz, $V_{EN} = V_{COM}$ =0V	PS398			31		
			PS399			14		
COM On Capacitance	$C_{COM(ON)}$	f=1MHz, V_{COM} = 0V	PS398			35		
			PS399			20		
Supply								
Power-Supply Range				Full	±3		±8	V
Positive Supply Current	I+	$V_{EN} = V_A$ = 0V or V+, V+ =5.5V, V- = -5.5V			-1		1	µA
NegativeSupply Current	I-				-1		1	
Ground Current	I_{GND}				-1		1	

Notes:
1. Algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum values of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ V_{COM} / V_{NO}. See Figure 5.

Electrical Characteristics - Single 5V Supply

(V+ = + 5V ± 10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4, V_{AL} = V_{ENL} = +0.8V)

Parameter	Symbol	Conditions		Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Switch								
Analog Signal Range(3)	V_{COM}, V_{NO}			Full	0		V+	V
On Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		25		100	225	Ω
				Full			280	
R_{ON} Matching Between Channels(4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		25			11	
				Full			13	
On -Resistance Flatness	R_{FLAT}	I_{NO} = 1mA, V_{COM} = 1.5V, 2.5V, 3.5V, V+ = 5V		25			18	
				Full			22	
NO-Off Leakage Current(8)	$I_{NO(OFF)}$	V_{NO} = 4.5V, V_{COM} = 0V, V+ = 5.5V		25	-0.1		0.1	nA
				Full	-1.0		1.0	
COM-Off Leakage Current(8)	$I_{COM(OFF)}$	V_{COM} = 4.5V, V_{NO} =0V, V+ = 5.5V	PS398	25	-0.2		50	
				Full	-2.5		100	
			PS399	25	-0.2		50	
				Full	-1.5		100	
COM-On Leakage Current(8)	$I_{COM(ON)}$	V_{COM} = 4.5V, V_{NO} =4.5V, V+ = 5.5V	PS398	25	-0.4		0.4	
				Full	-5		5	
			PS399	25	-0.2		0.2	
				Full	-2.5		2.5	
Digital Logic Input								
Logic High Input Voltage	V_{AH}, V_{ENH}			Full	2.4			V
Logic Low Input Voltage	V_{AH}, V_{ENL}						0.8	
Input Current with Input Voltage High	I_{AH}, I_{ENH}	V_A= V_{EN} = 2.4V			-0.1		0.1	µA
Input Current with Input Voltage Low	I_{AH}, I_{ENL}	V_A= V_{EN} = 0.8V			-0.1		0.1	
Supply								
Power-Supply Range	V+			Full	3		15	V
Positive-Supply Current	I+	V_{EN} = V+ or 0V, V_A = 0V, V+ = 5.5V, V- = 0V			-1.0		1.0	µA
Negative-Supply Current	I-				-1.0		1.0	
Ground Current	I_{GND}				-1.0		1.0	

Electrical Characteristics - Single 5V

($V+ = +5V \pm 10\%$, $V- = 0V$, $GND = 0V$, $V_{AH} = V_{ENH} = +2.4$, $V_{AL} = V_{ENL} = +0.8V$ **(continued)**

Parameter	Symbol	Conditions	Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Dynamic							
Transition Time	t_{TRANS}	$V_{NO} = 3V$	25		72	245	ns
Break-Before-Make Interval	t_{OPEN}			10	36		
Enable Turn-On Time	$t_{ON(EN)}$				110	200	
			Full			275	
Enable Turn-Off Time	$t_{OFF(EN)}$		25		65	125	
			Full			200	
Charge Injection(3)	Q	$C_L = 1nF$, $V_S = 0V$, $R_S = 0\Omega$	25		2.8	5	pC

Electrical Characteristics - Single 3V Supply

($V+ = +3V \pm 10\%$, $V- = 0V$, $GND = 0V$, $V_{AH} = V_{ENH} = +2.4$, $V_{AL} = V_{ENL} = +0.8V$)

Parameter	Symbol	Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V+	V
On-Resistance	R_{ON}	$I_{NO} = 1mA$, $V_{COM} = 1.5V$, $V+ = 3V$	25		160	375	Ω
			Full			425	
Dynamic							
Transition Time(3)	t_{TRANS}	Figure 1, $V_{IN} = 2.4V$, $V_{NO1} = 1.5V$, $V_{NO8} = 0V$	25		200	575	ns
Enable Turn-OnTime(3)	$t_{ON(EN)}$	Figure 2, $V_{INH} = 2.4V$, $V_{INL} = 0V$, $V_{NO1} = 1.5V$			200	500	
Enable Turn-Off Time(3)	$t_{OFF(EN)}$	Figure 2, $V_{INH} = 2.4V$, $V_{INL} = 0V$, $V_{NO1} = 1.5V$			92	400	
Charge Injection (3)	Q	$C_L = 10nF$, $V_S = 0V$, $R_S = 0\Omega$			2	5	pC

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin.
   Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, V_{NO} = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Test Circuits/Timing Diagrams

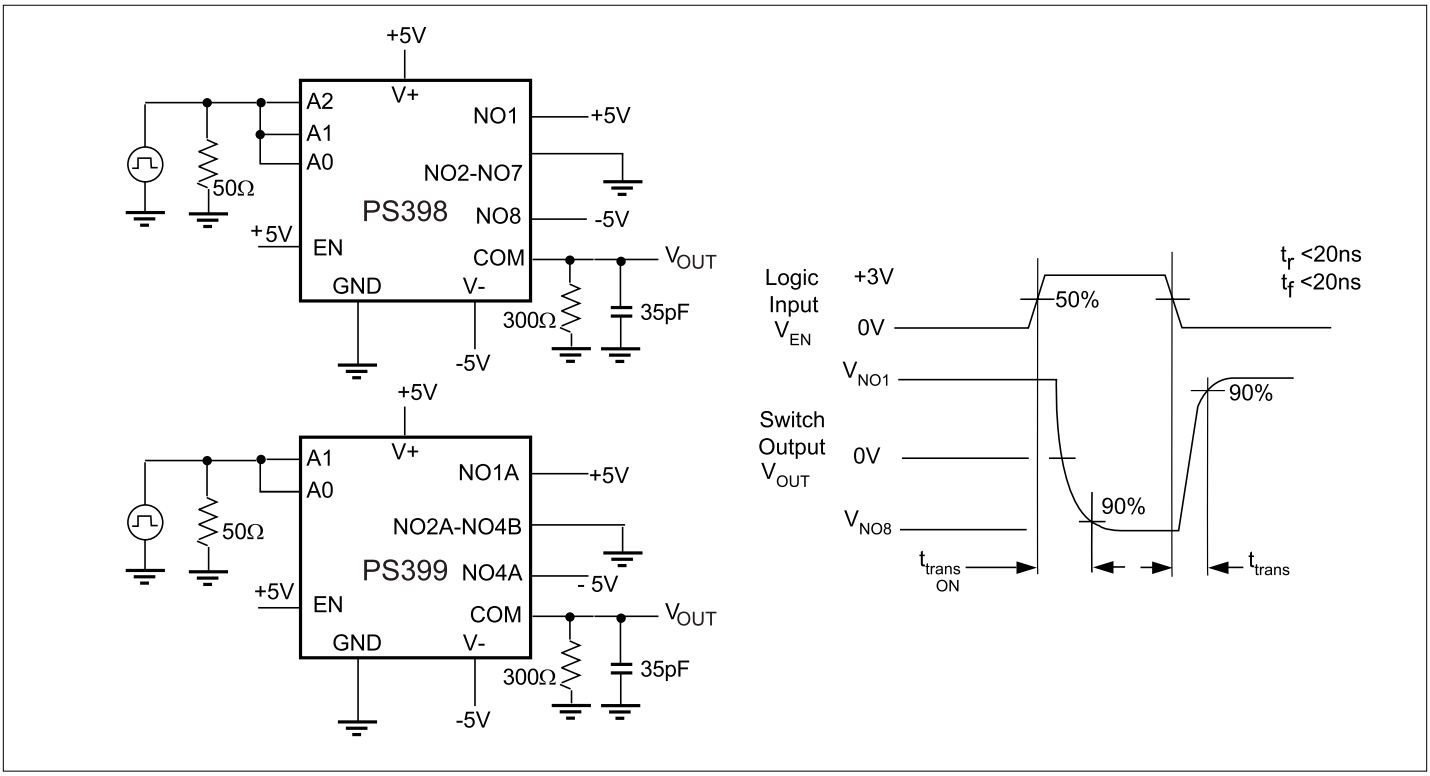


Figure 1. Transition Time

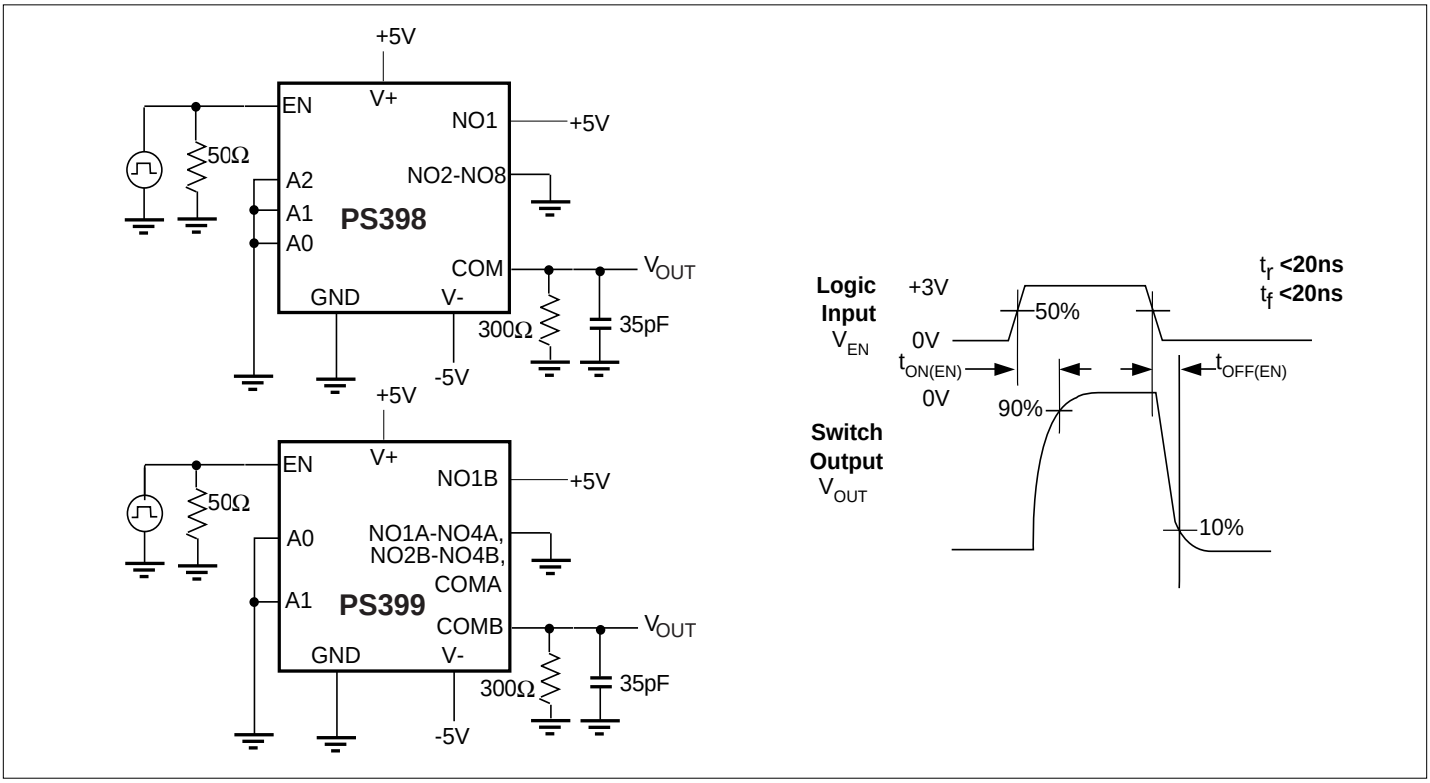


Figure 2. Enable Switching Time

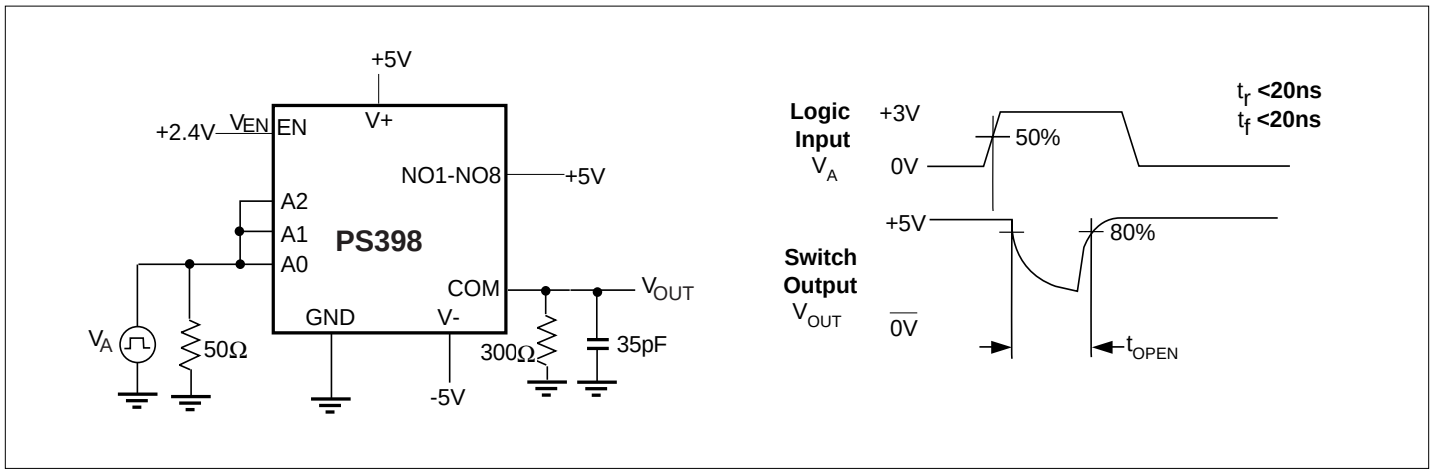


Figure 3. Break-Before-Make Interval

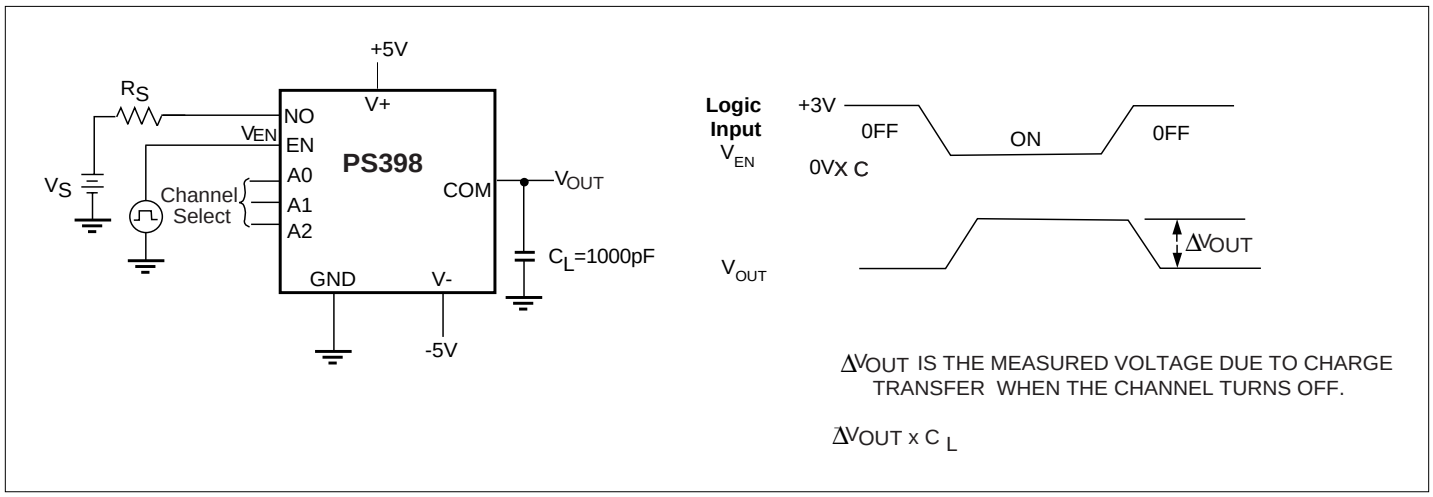


Figure 4. Charge Injection

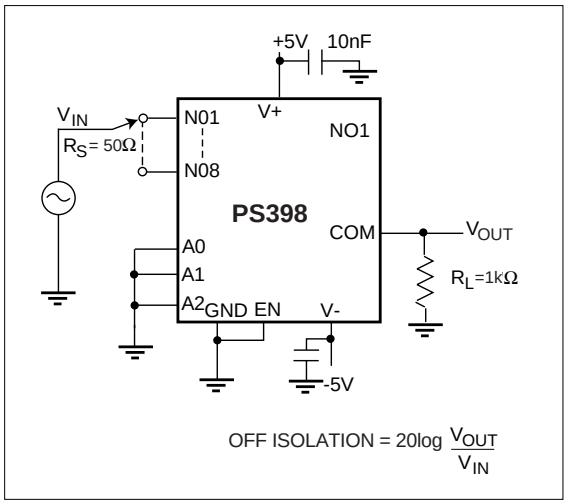


Figure 5. Off Isolation

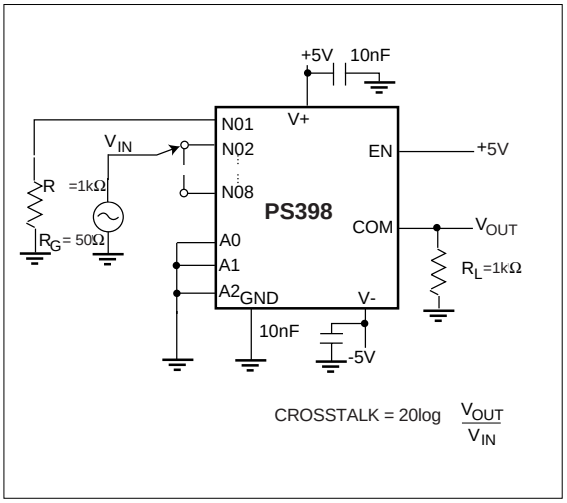


Figure 6. CrossTalk

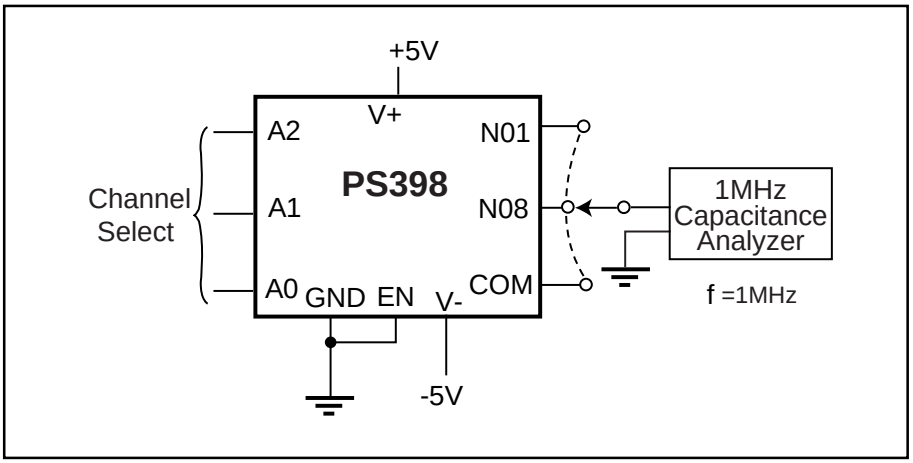


Figure 8. NO/COM Capacitance

Applications

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 9). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

Maximum Sampling Rate

From the sampling theorem, the sampling frequency needed to properly recover the original signal should be more than twice its maximum component frequency. In real applications, sampling at three or four times the maximum signal frequency is customary.

The maximum sampling rate of a multiplexer is determined by its transition time (t_{TRANS}), the number of channels being multiplexed, and the settling time ($t_{SETTLING}$) of the sampled signal at the output. The maximum sampling rate is:

$$f_S = \frac{1}{n\,(t_{TRANS} + t_{SETTLING})} \qquad (1)$$

Where n = number of channels scanned: 8 for PS398, 4 for PS399. t_{TRANS} is given on the specification table: 150 ns max.

Settling time is the time needed for the output to stabilize within the desired accuracy band of +1 LSB (least significant bit).

Other factors determining settling time are: signal source impedance, capacitive load at the output. Figure 10 illustrates the steady state model. To figure out what the settling time due to the multiplexer is, we can assume that $R_S = 0\Omega$, and $C_L = 0$. In real life, the effects of R_S and C_L should be taken into account when performing these calculations.

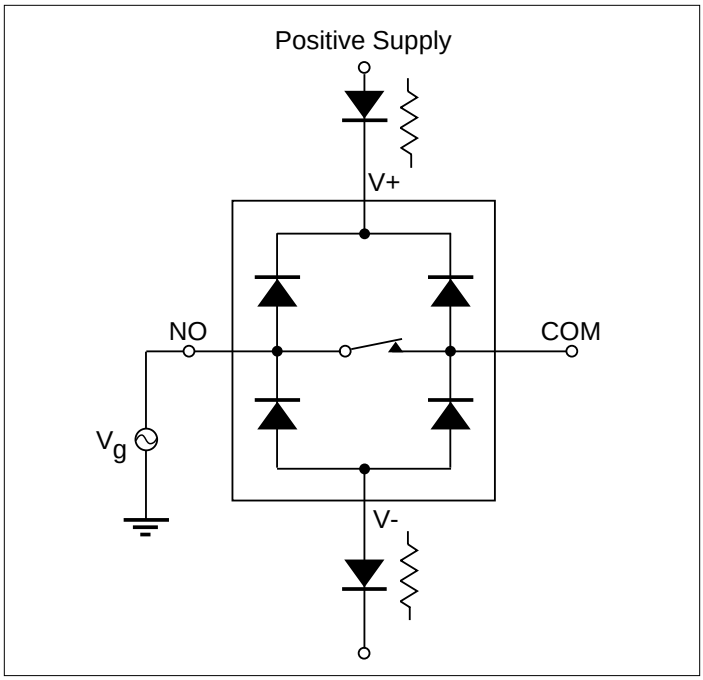


Figure 9. Overvoltage protection is accomplished using two external blocking diodes or two current limiting resistors.

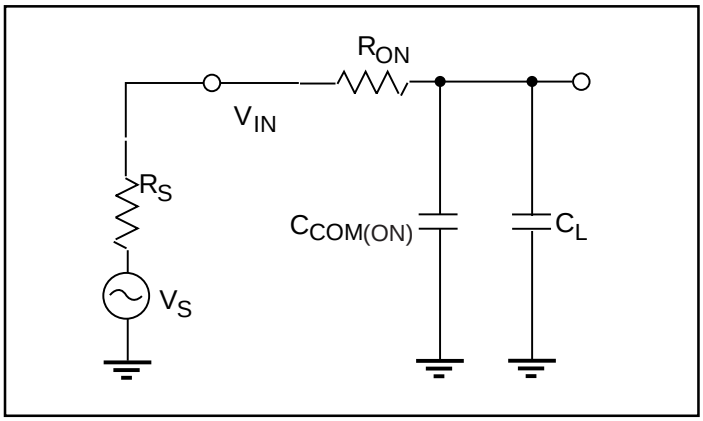


Figure 10. Equivalent model of one multiplexer channel

The table below shows how many time constants ($m\tau$) are needed to reach an accuracy of one LSB. $\tau = R_{ON} \times C_{COM(ON)}$

Bits	Accuracy (%)	m
8	0.25	6
12	0.012	9
15	0.0017	11

Now, let's calculate what the maximum sampling rate for the PS398. Assume a 12-bit accuracy and room temperature operation.

In equation (1) above, n = 8, t_{TRANS} = 150ns, $t_{SETTLING} = 9\tau$, $\tau = 100\Omega \times 54pF$

$$f_S = \frac{1}{8\,[150ns + 9(100\Omega \times 54pF)]},$$

or f_S = 630kHz.

Assuming a x4 oversampling rate, the maximum sampling speed for the PS398 would be 630÷4 = 157kHz.