

2SJ130(L), 2SJ130(S)

Silicon P-Channel MOS FET

HITACHI

Application

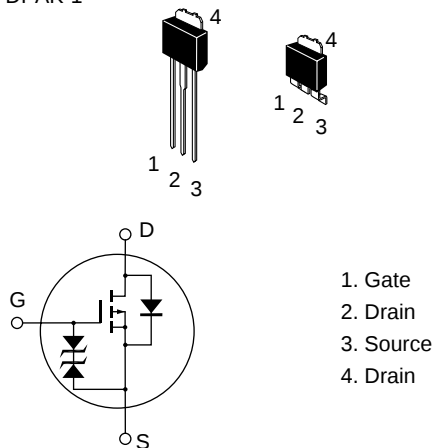
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and ultrasonic power oscillators

Outline

DPAK-1



2SJ130(L), 2SJ130(S)

Absolute Maximum Ratings (Ta = 25°C)

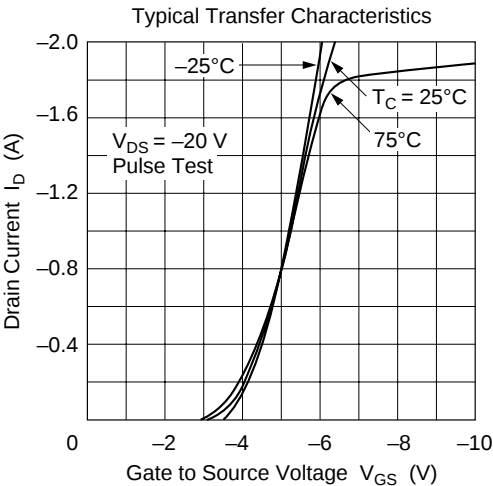
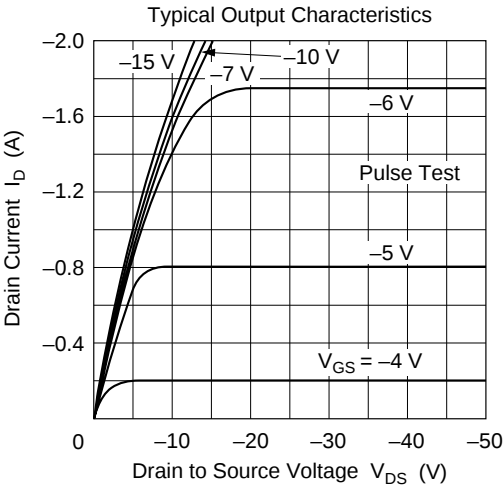
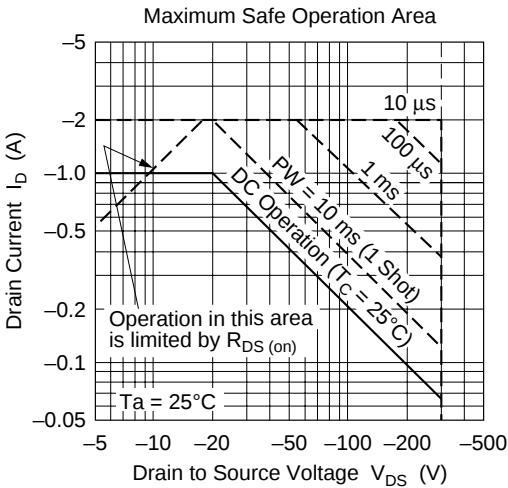
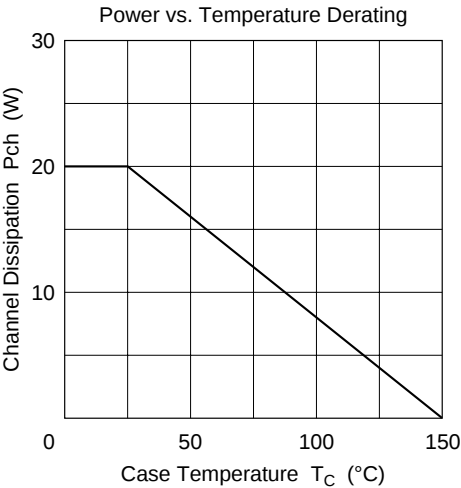
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	−300	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	−1	A
Drain peak current	$I_{D(pulse)}$	−2	A
Body to drain diode reverse drain current	I_{DR}	−1	A
Channel dissipation	P_{ch}^{*1}	20	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note: 1. Value at $T_C = 25^\circ\text{C}$

Electrical Characteristics (Ta = 25°C)

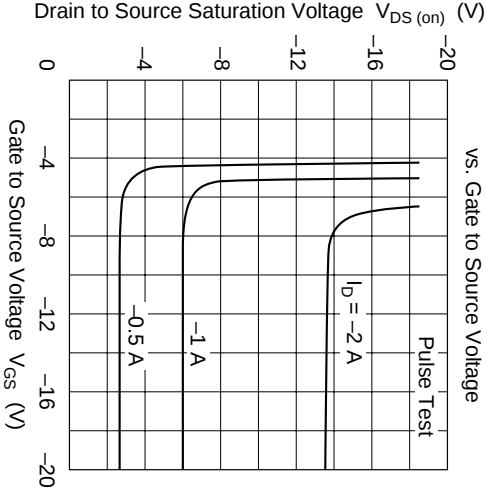
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	−300	—	—	V	$I_D = -10\text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	−100	μA	$V_{DS} = -240\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	−2.0	—	−4.0	V	$I_D = -1\text{ mA}$, $V_{DS} = -10\text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.0	8.5	Ω	$I_D = -0.5\text{ A}$, $V_{GS} = -10\text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	0.25	0.4	—	S	$I_D = -0.5\text{ A}$, $V_{DS} = -20\text{ V}^{*1}$
Input capacitance	C_{iss}	—	235	—	pF	$V_{DS} = -10\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$
Output capacitance	C_{oss}	—	65	—	pF	
Reverse transfer capacitance	C_{rss}	—	16	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = -0.5\text{ A}$, $V_{GS} = -10\text{ V}$, $R_L = 60\text{ }\Omega$
Rise time	t_r	—	25	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	45	—	ns	
Body to drain diode forward voltage	V_{DF}	—	−0.9	—	V	$I_F = -1\text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	200	—	ns	$I_F = -1\text{ A}$, $V_{GS} = 0$, $di_F/dt = 50\text{ A}/\mu\text{s}$

Note: 1. Pulse test

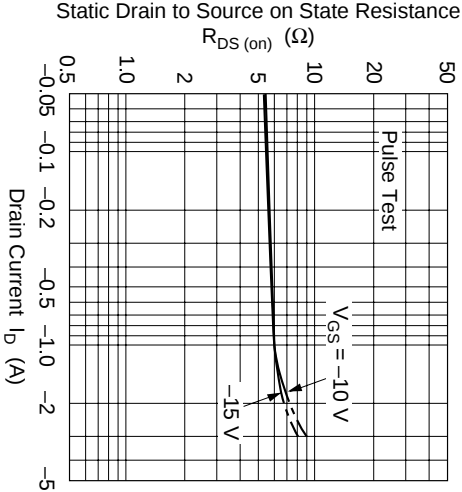


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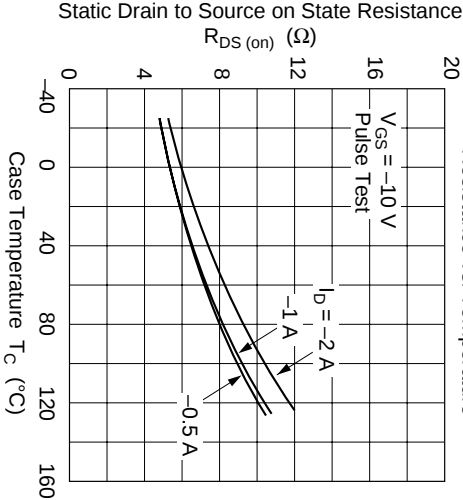
Drain to Source Saturation Voltage
vs. Gate to Source Voltage



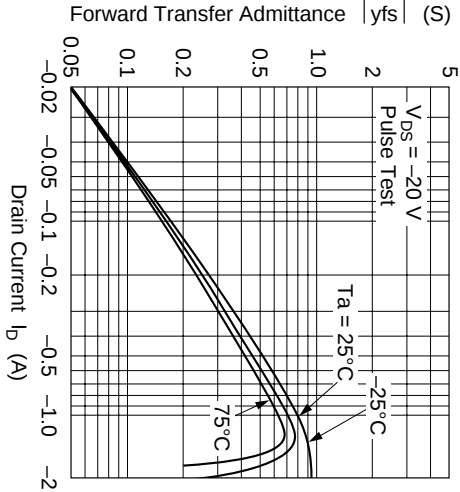
Static Drain to Source on State
Resistance vs. Drain Current



Static Drain to Source on State
Resistance vs. Temperature

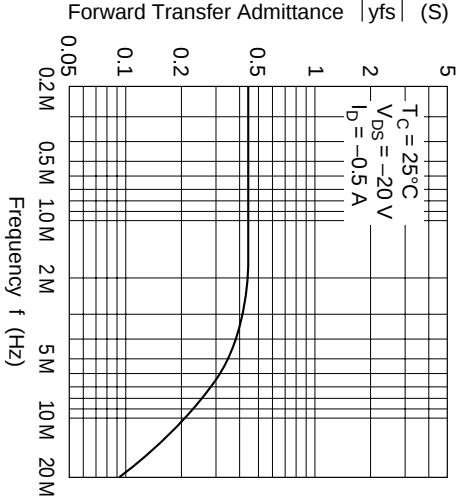


Forward Transfer Admittance
vs. Drain Current

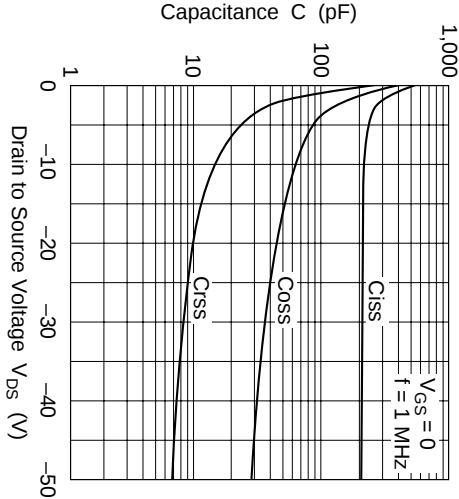


2SJ130(L), 2SJ130(S)

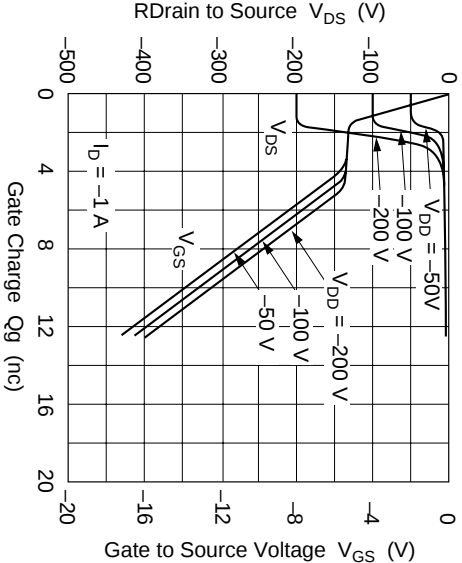
Forward Transfer Admittance
vs. Frequency



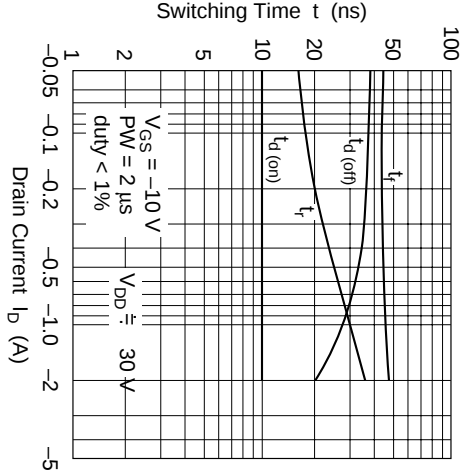
Typical Capacitance vs.
Drain to Source Voltage

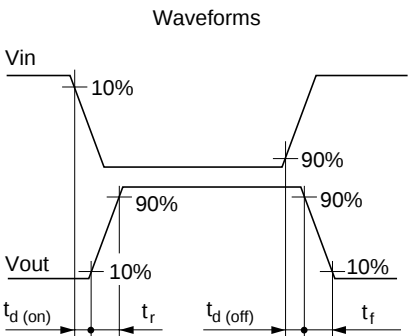
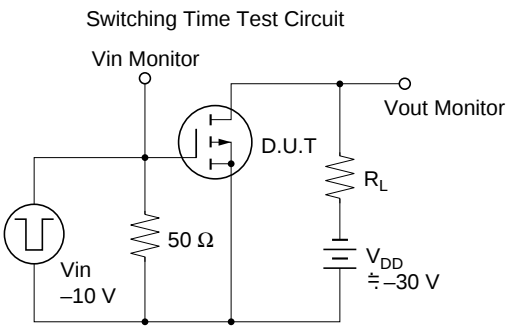
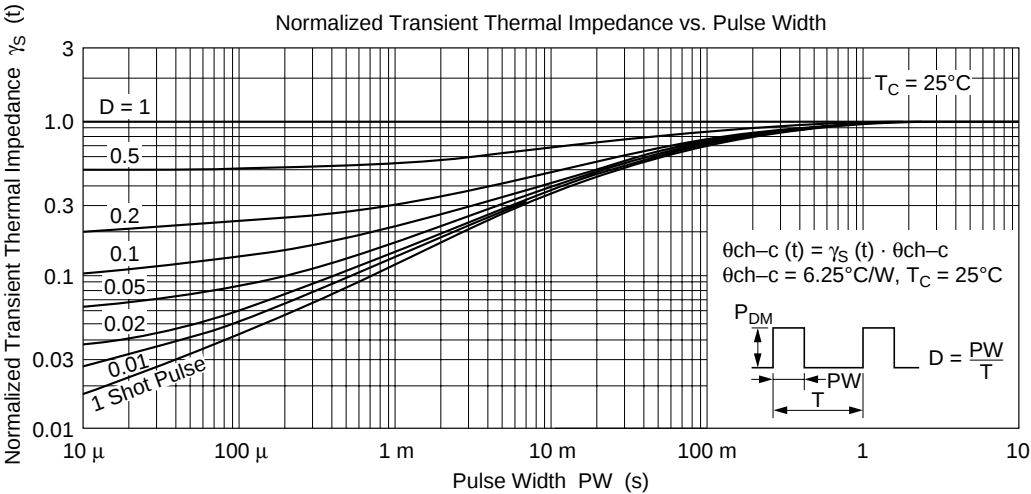
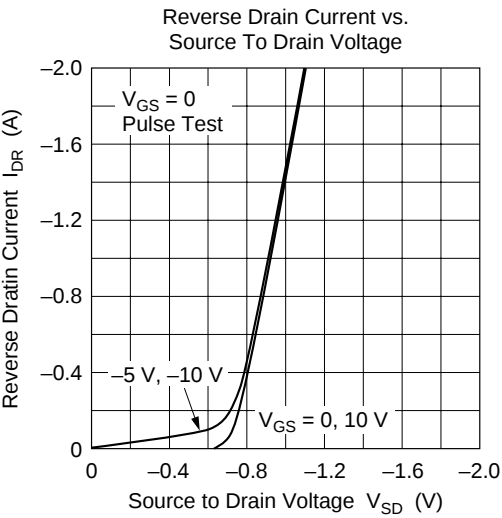


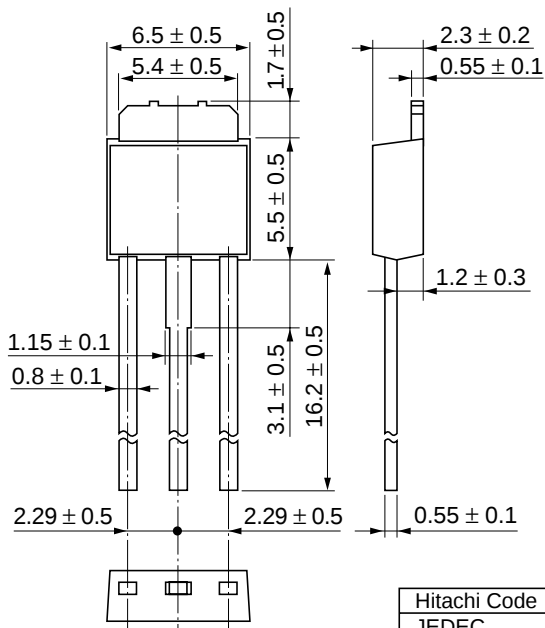
Dynamic Input Characteristics



Switching Characteristics







Hitachi Code	DPAK (L)-(1)
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.42 g

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