

# 2SJ484

Silicon P-Channel MOS FET  
High Speed Power Switching

# HITACHI

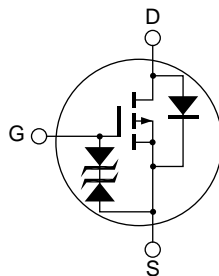
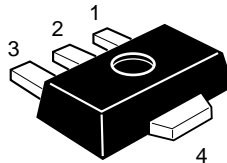
ADE-208-501A (Z)  
2nd. Edition  
Mar. 2001

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.18 \Omega$  typ. (at  $V_{GS} = -10V$ ,  $I_D = -1A$ )
- Low drive current
- High speed switching
- 4V gate drive devices.

## Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	-2	A
Drain peak current	$I_{D(pulse)}^{*1}$	-4	A
Body to drain diode reverse drain current	$I_{DR}$	-2	A
Channel dissipation	$Pch^{*2}$	1	W
Channel temperature	$Tch$	150	$^\circ\text{C}$
Storage temperature	$Tstg$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 100\mu\text{s}$ , duty cycle  $\leq 10\%$

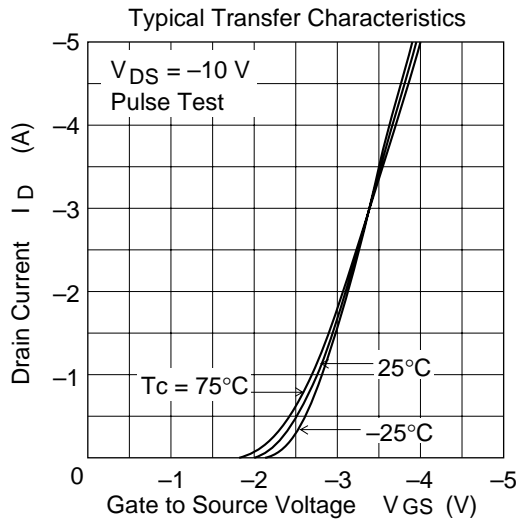
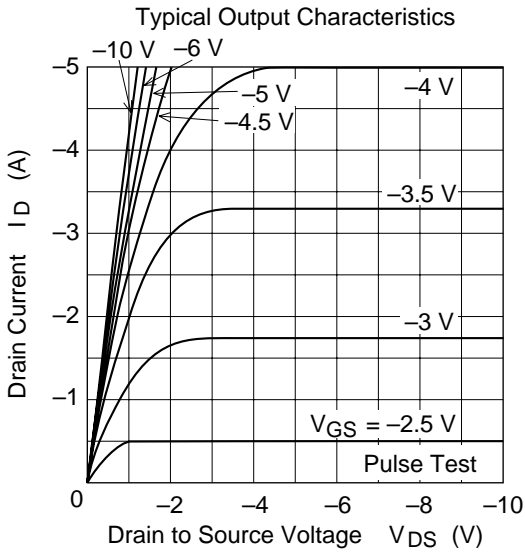
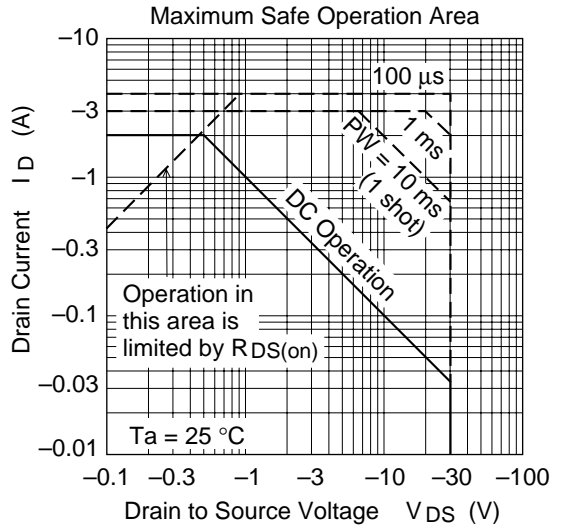
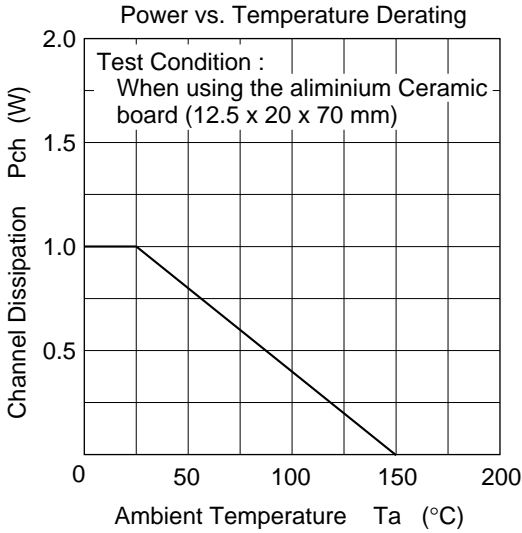
2. When using aluminium ceramic board (12.5 x 20 x 0.7 mm)

## Electrical Characteristics (Ta = 25°C)

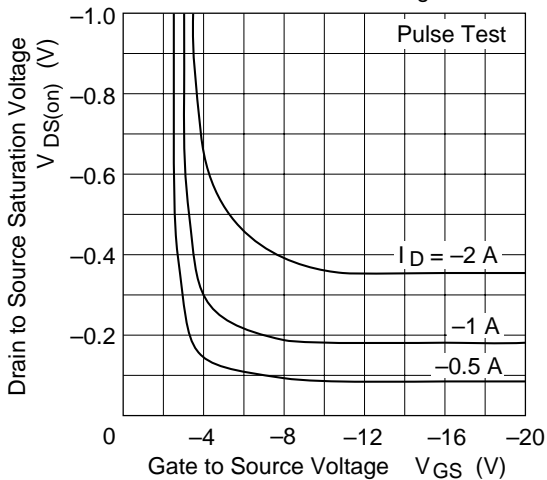
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	$\mu\text{A}$	$V_{DS} = -30\text{V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$ , $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.18	0.23	$\Omega$	$I_D = -1\text{A}$ , $V_{GS} = -10\text{V}^{*1}$
	$R_{DS(on)}$	—	0.3	0.45	$\Omega$	$I_D = -1\text{A}$ , $V_{GS} = -4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.2	2.0	—	S	$I_D = -1\text{A}$ , $V_{DS} = -10\text{V}^{*1}$
Input capacitance	$C_{iss}$	—	230	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	$C_{oss}$	—	140	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	50	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = -1\text{A}$ , $R_L = 30\Omega$
Rise time	$t_r$	—	30	—	ns	$V_{GS} = -10\text{V}$
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	$t_f$	—	30	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	-0.95	—	V	$I_F = -2\text{A}$ , $V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = -2\text{A}$ , $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

Notes: 1. Pulse test  
2. Marking is "WY".

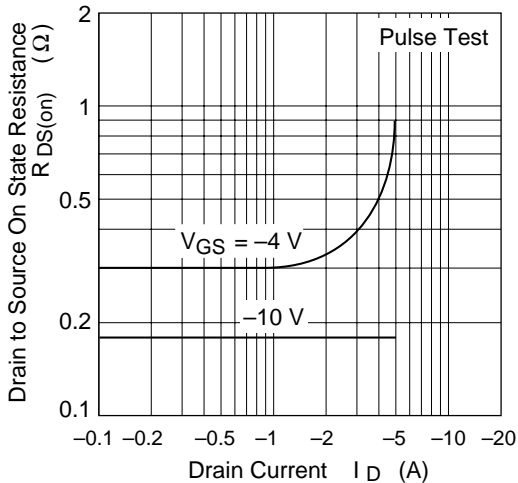
Main Characteristics



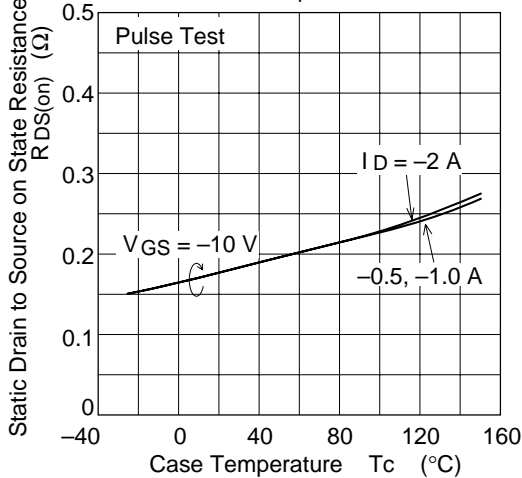
Drain to Source Saturation Voltage vs. Gate to Source Voltage



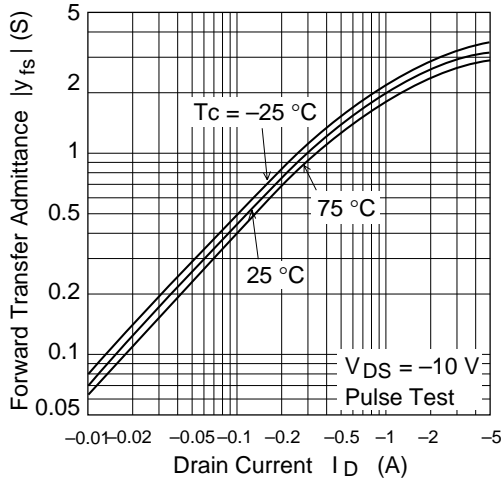
Static Drain to Source on State Resistance vs. Drain Current



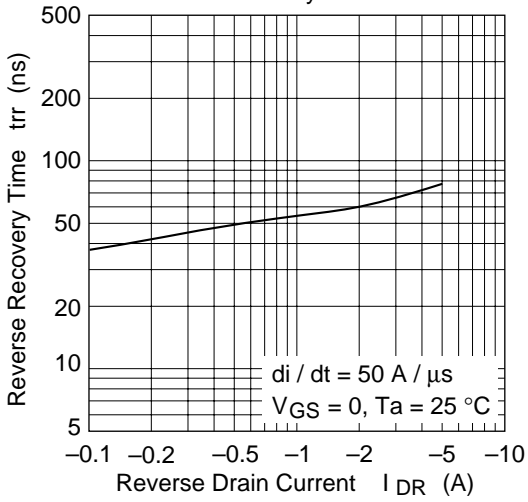
Static Drain to Source on State Resistance vs. Temperature



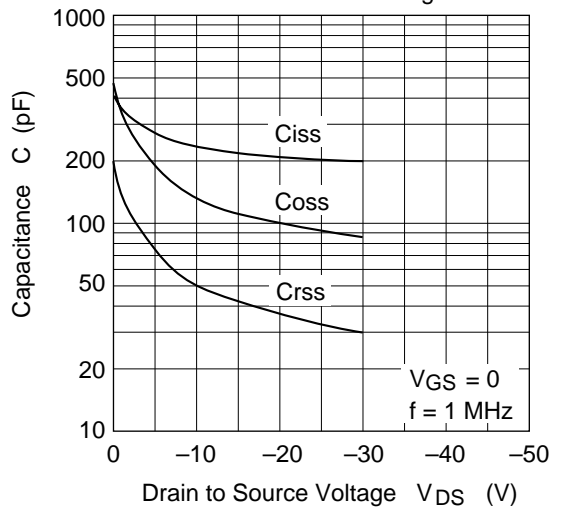
Forward Transfer Admittance vs. Drain Current



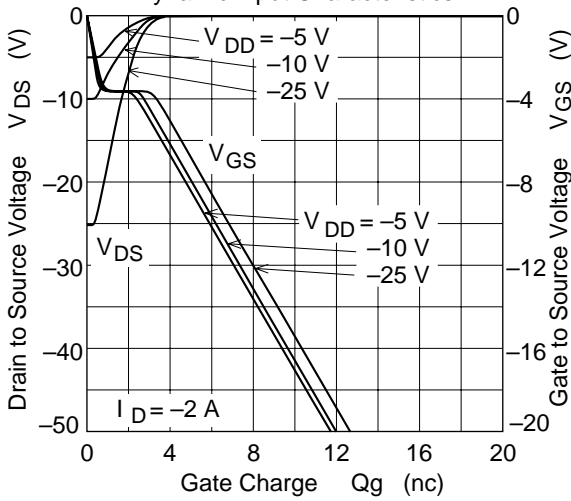
Body to Drain Diode Reverse Recovery Time



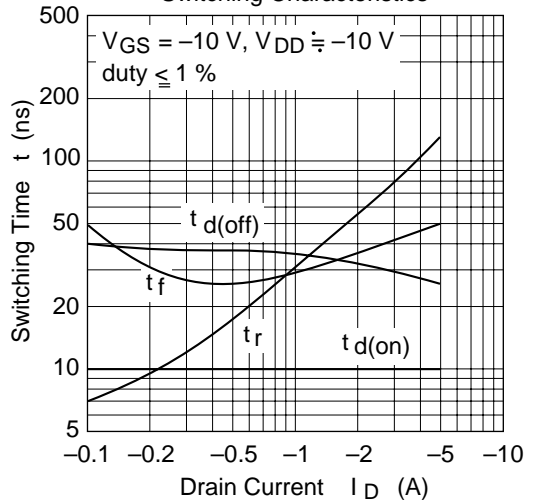
Typical Capacitance vs. Drain to Source Voltage

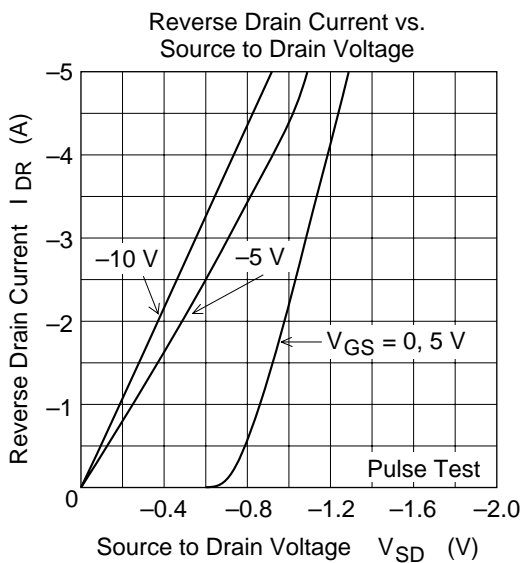


Dynamic Input Characteristics

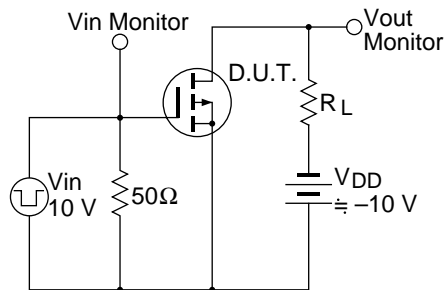


Switching Characteristics

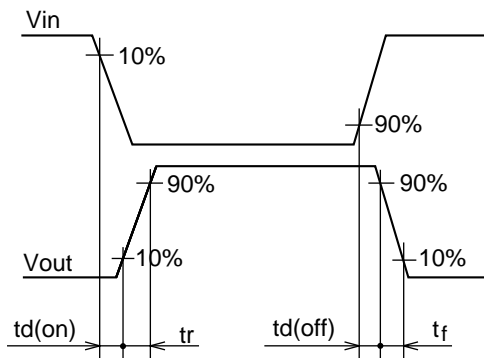




Switching Time Test Circuit

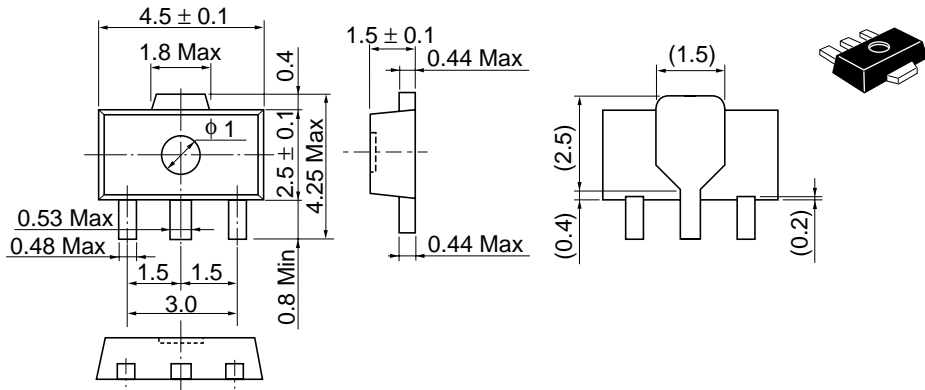


Switching Time Waveform



Package Dimensions

As of January, 2001  
Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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