

2SJ517

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

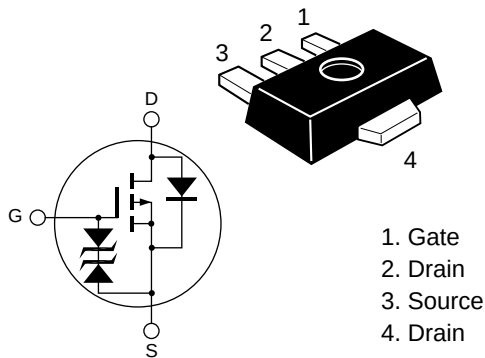
ADE-208-575B (Z)
3rd. Edition
Jun 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.18 \Omega$ typ. (at $V_{GS} = -4V$, $I_D = -1A$)
- Low drive current
- High speed switching
- 2.5V gate drive devices.

Outline

UPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	−20	V
Gate to source voltage	V _{GSS}	±10	V
Drain current	I _D	−2	A
Drain peak current	I _{D(pulse)} ^{Note1}	−4	A
Body-drain diode reverse drain current	I _{DR}	−2	A
Channel dissipation	Pch ^{Note2}	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

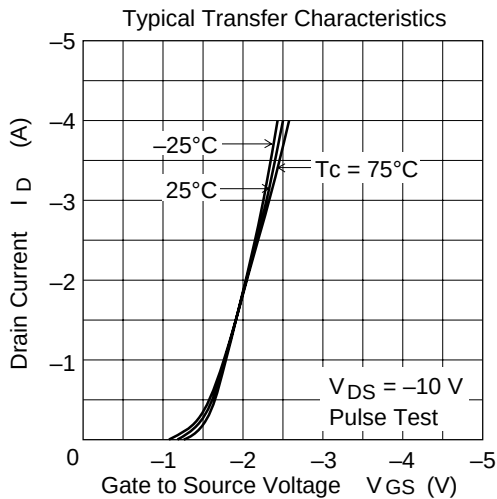
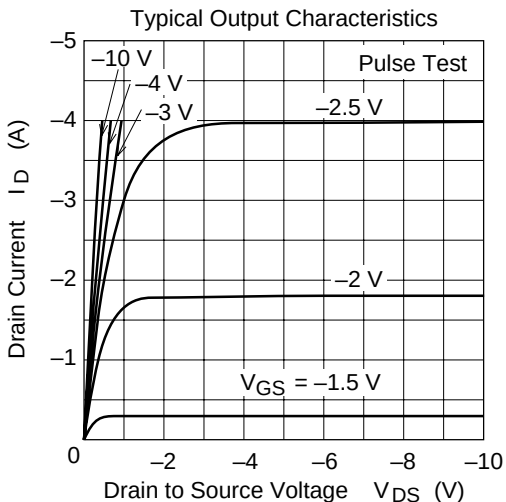
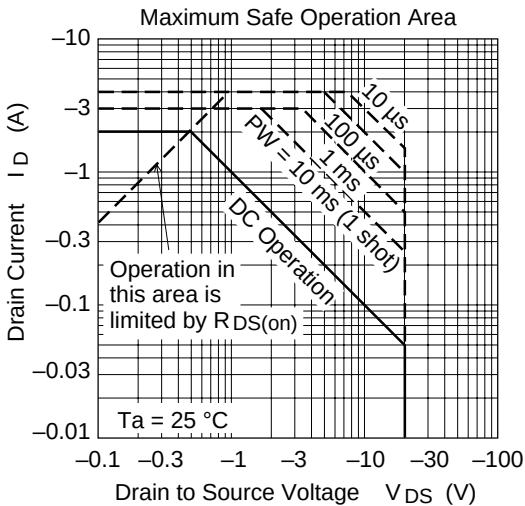
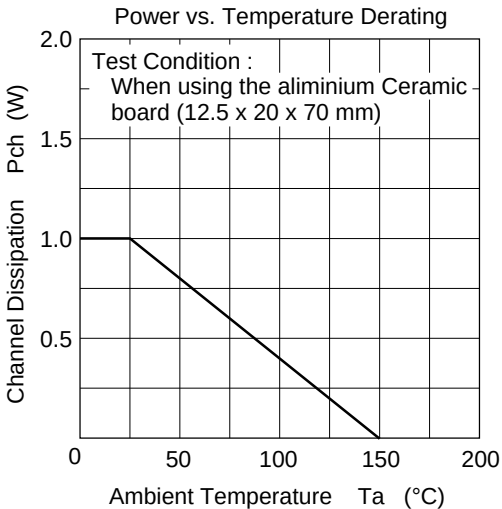
Note: 1. PW ≤ 100μs, duty cycle ≤ 10 %
2. When using aluminium ceramic board (12.5 x 20 x 0.7 mm)

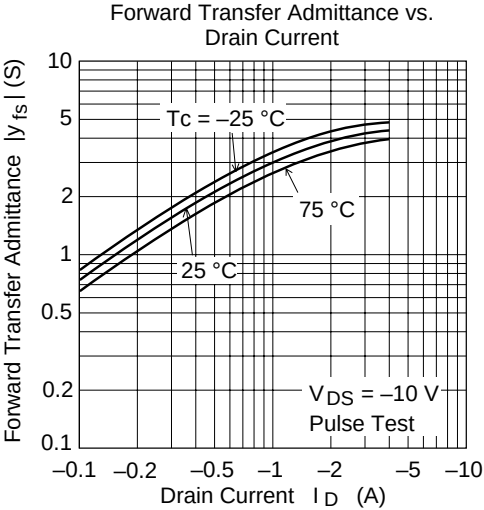
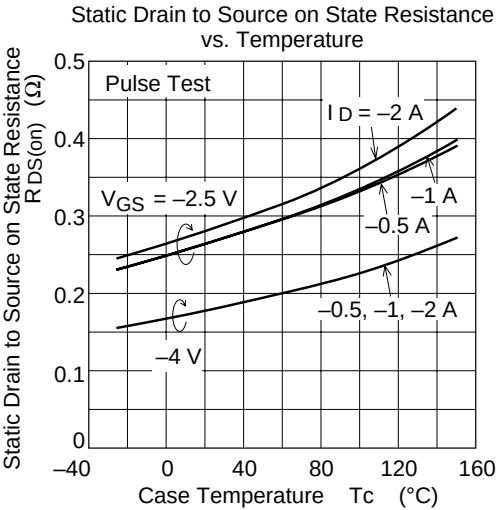
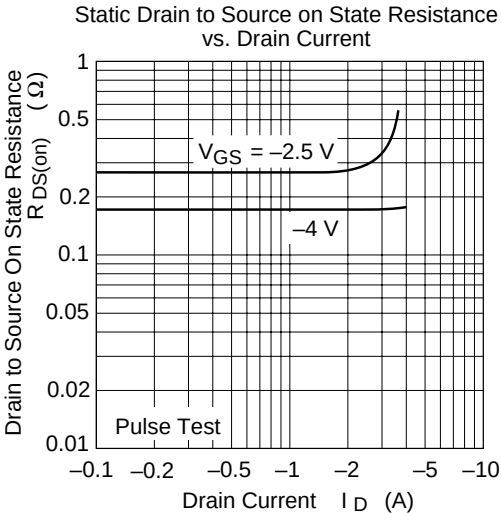
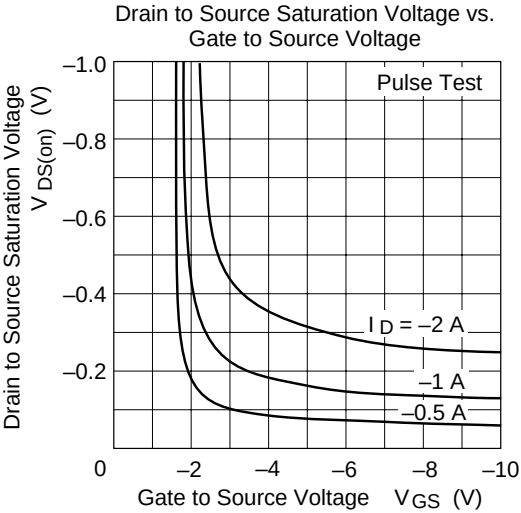
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	−20	—	—	V	I _D = −10mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±10	—	—	V	I _G = ±100μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	−10	μA	V _{DS} = −20 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±8V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	−0.5	—	−1.5	V	I _D = −1mA, V _{DS} = −10V
Static drain to source on state resistance	R _{DS(on)}	—	0.18	0.24	Ω	I _D = −1A, V _{GS} = −4V ^{Note3}
Static drain to source on state resistance	R _{DS(on)}	—	0.27	0.43	Ω	I _D = −1A, V _{GS} = −2.5V ^{Note3}
Forward transfer admittance	y _{fs}	1.8	3.0	—	S	I _D = −1A, V _{DS} = −10V ^{Note3}
Input capacitance	Ciss	—	320	—	pF	V _{DS} = −10V
Output capacitance	Coss	—	190	—	pF	V _{GS} = 0
Reverse transfer capacitance	Crss	—	90	—	pF	f = 1MHz
Turn-on delay time	t _{d(on)}	—	14	—	ns	I _D = −1A, R _L = 10Ω
Rise time	t _r	—	75	—	ns	V _{GS} = −4V
Turn-off delay time	t _{d(off)}	—	90	—	ns	
Fall time	t _f	—	90	—	ns	
Body–drain diode forward voltage	V _{DF}	—	−0.95	—	V	I _F = −2A, V _{GS} = 0
Body–drain diode reverse recovery time	t _{rr}	—	70	—	ns	I _F = −2A, V _{GS} = 0 diF/ dt =50A/μs

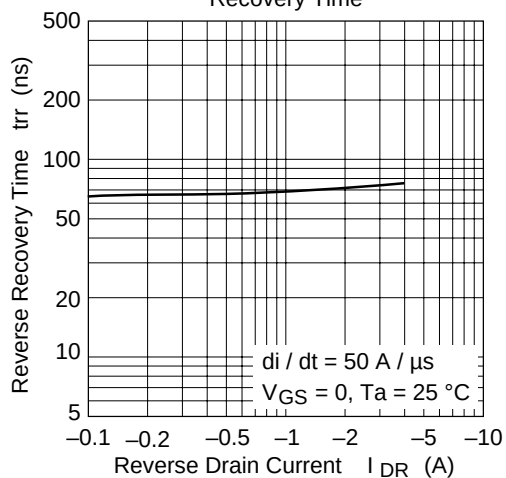
Note: 3. Pulse test
4. Marking is “YY”.

Main Characteristics

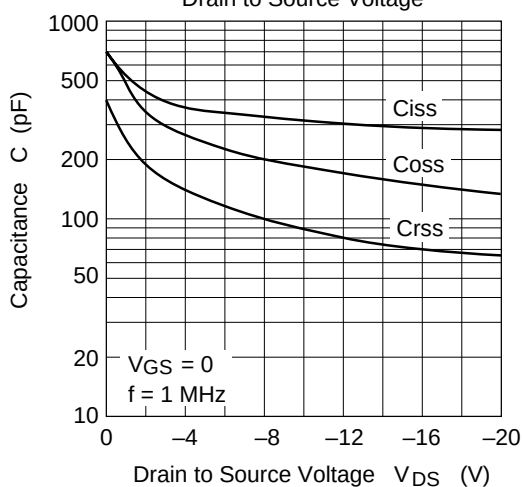




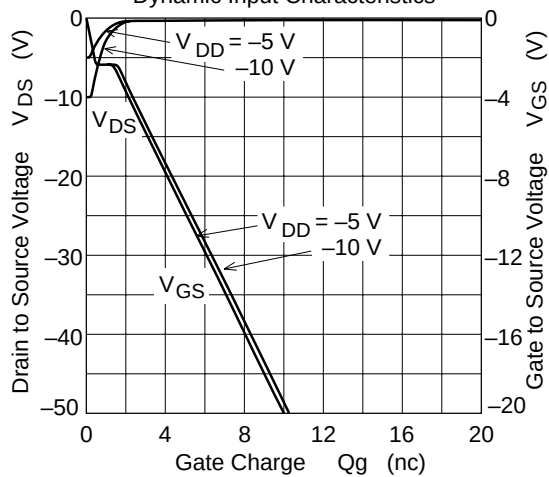
Body-Drain Diode Reverse Recovery Time



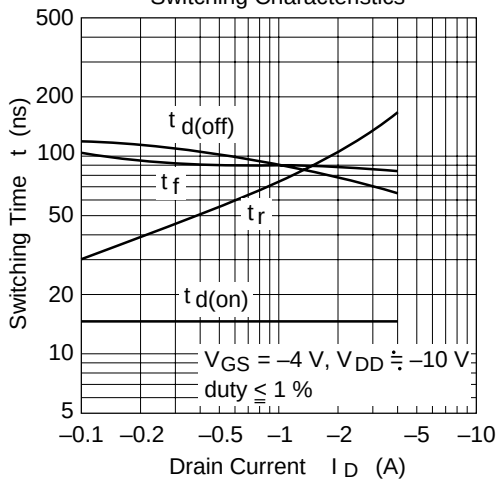
Typical Capacitance vs. Drain to Source Voltage

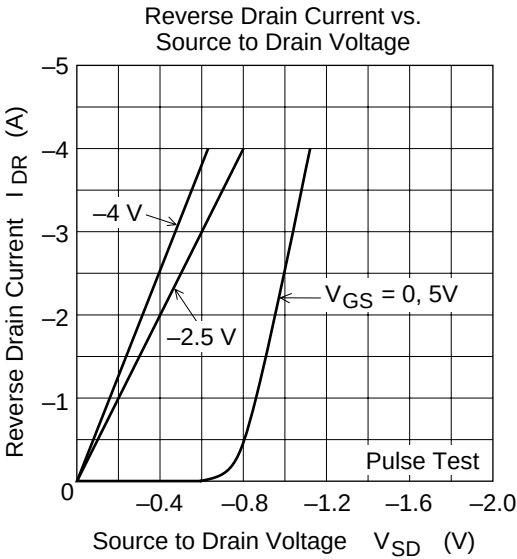


Dynamic Input Characteristics

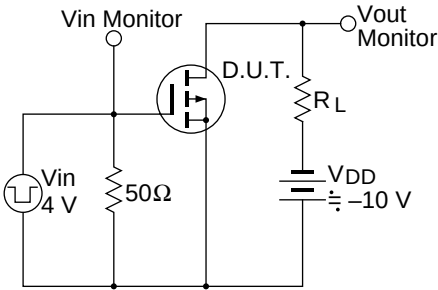


Switching Characteristics

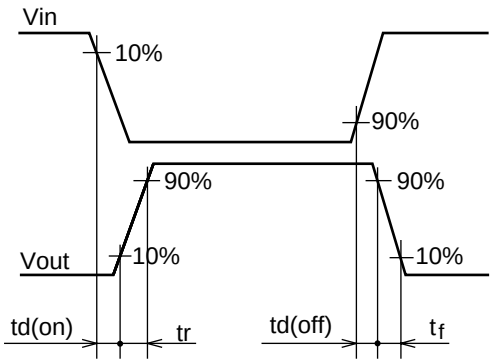




Switching Time Test Circuit

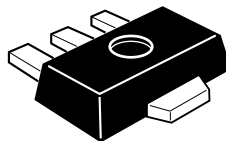
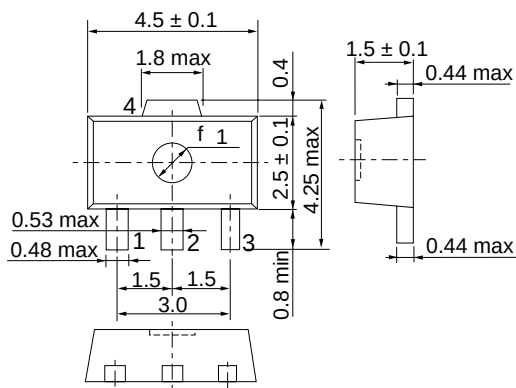


Waveform



Package Dimensions

Unit: mm



Hitachi Code	UPAK
EIAJ	SC-62
JEDEC	UPAK

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