

# 2SJ554

Silicon P Channel MOS FET  
High Speed Power Switching

# HITACHI

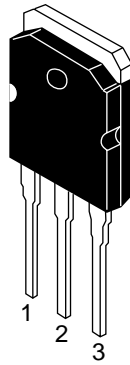
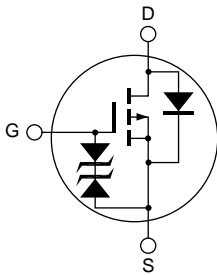
ADE-208-628B (Z)  
3rd. Edition  
Jun 1998

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.028\Omega$  typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

## Outline

TO-3P



1. Gate
2. Drain  
(Flange)
3. Source

**Absolute Maximum Ratings** (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	-60	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	-45	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	-180	A
Body-drain diode reverse drain current	I <sub>DR</sub>	-45	A
Avalanche current	I <sub>AP</sub> <sup>Note3</sup>	-45	A
Avalanche energy	E <sub>AR</sub> <sup>Note3</sup>	173	mJ
Channel dissipation	Pch <sup>Note2</sup>	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

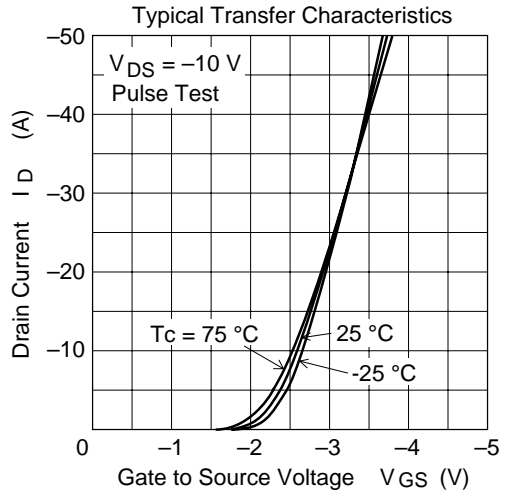
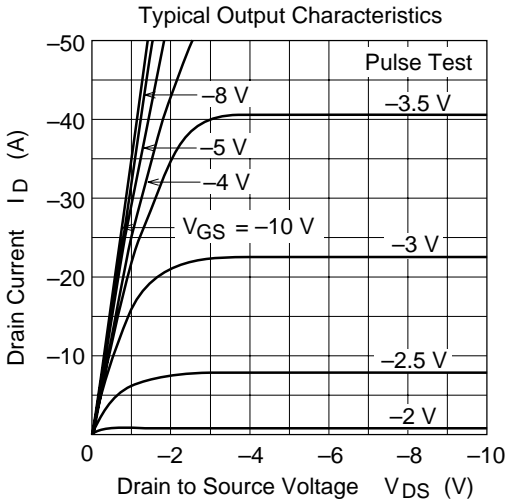
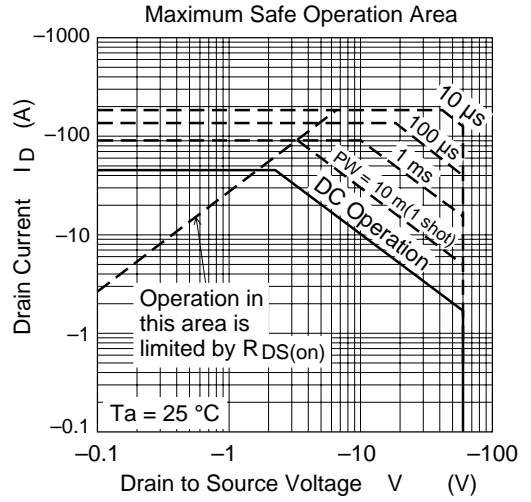
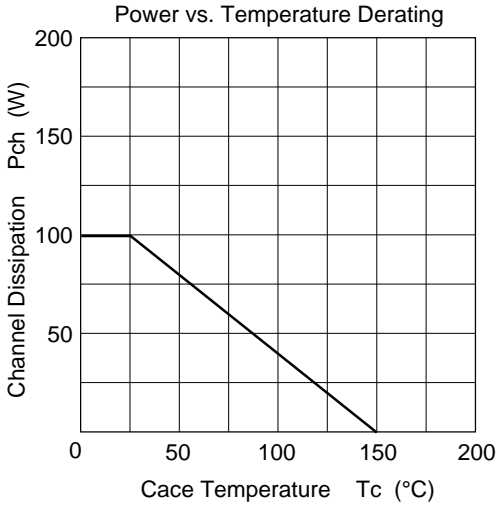
- Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %  
 2. Value at Tc = 25°C  
 3. Value at Tch = 25°C, Rg ≥ 50 Ω

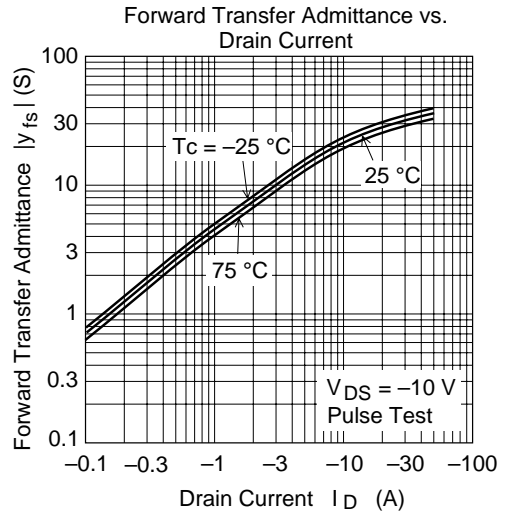
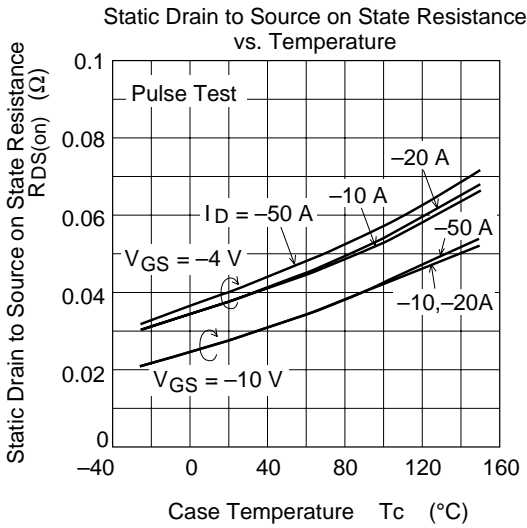
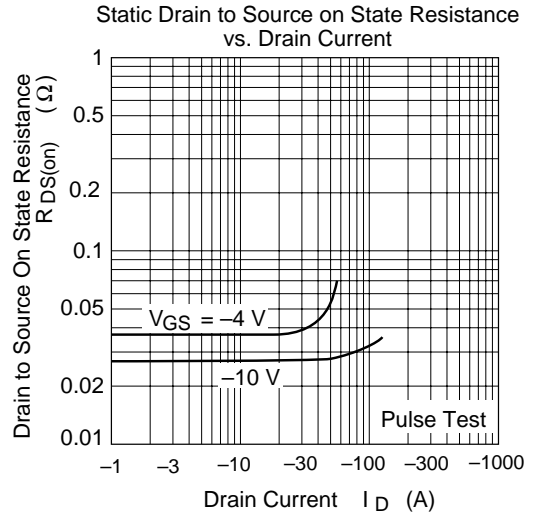
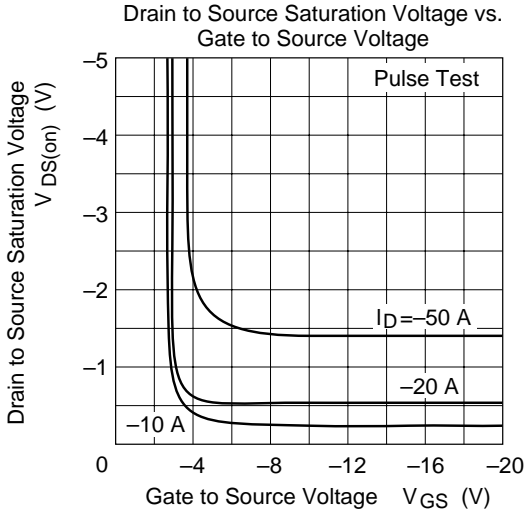
**Electrical Characteristics** (Ta = 25°C)

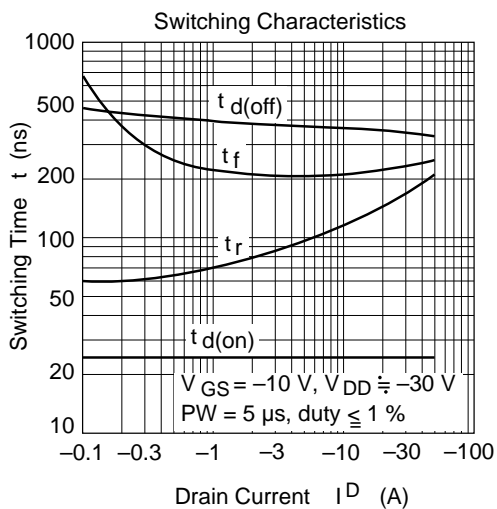
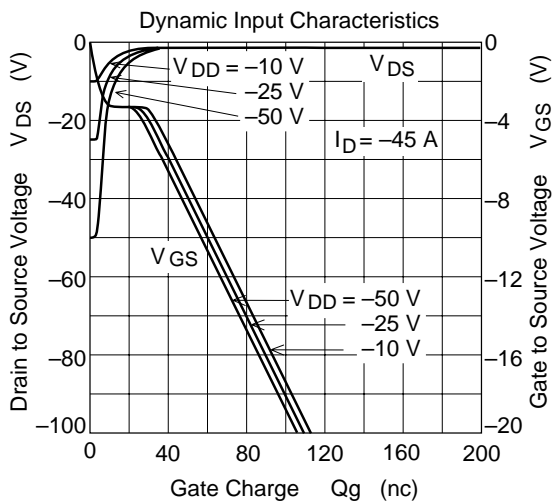
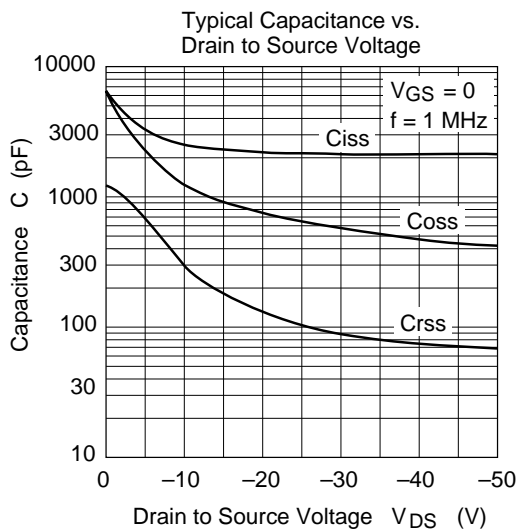
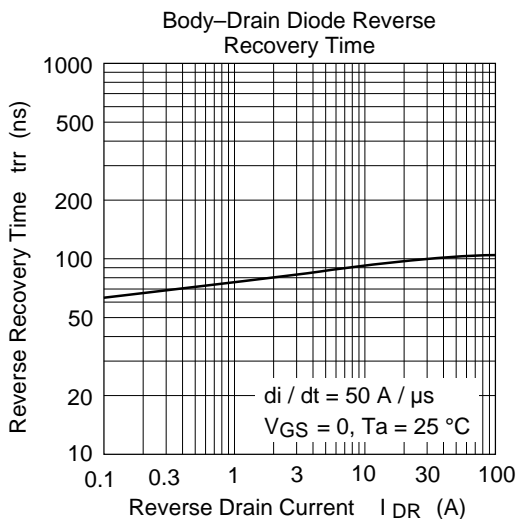
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	-60	—	—	V	I <sub>D</sub> = -10mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	±20	—	—	V	I <sub>G</sub> = ±100μA, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±16V, V <sub>DS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	-1.0	—	-2.0	V	I <sub>D</sub> = -1mA, V <sub>DS</sub> = -10V
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	0.028	0.037	Ω	I <sub>D</sub> = -25A, V <sub>GS</sub> = -10V <sup>Note4</sup>
	R <sub>DS(on)</sub>	—	0.038	0.055	Ω	I <sub>D</sub> = -25A, V <sub>GS</sub> = -4V <sup>Note4</sup>
Forward transfer admittance	y <sub>fs</sub>	18	30	—	S	I <sub>D</sub> = -25A, V <sub>DS</sub> = -10V <sup>Note4</sup>
Input capacitance	Ciss	—	2500	—	pF	V <sub>DS</sub> = -10V
Output capacitance	Coss	—	1300	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1MHz
Turn-on delay time	t <sub>d(on)</sub>	—	25	—	ns	V <sub>GS</sub> = -10V, I <sub>D</sub> = -25A
Rise time	t <sub>r</sub>	—	160	—	ns	R <sub>L</sub> = 1.2Ω
Turn-off delay time	t <sub>d(off)</sub>	—	350	—	ns	
Fall time	t <sub>f</sub>	—	240	—	ns	
Body-drain diode forward voltage	V <sub>DF</sub>	—	-1.1	—	V	I <sub>F</sub> = -45A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	100	—	ns	I <sub>F</sub> = -45A, V <sub>GS</sub> = 0 dI <sub>F</sub> / dt = 50A/μs

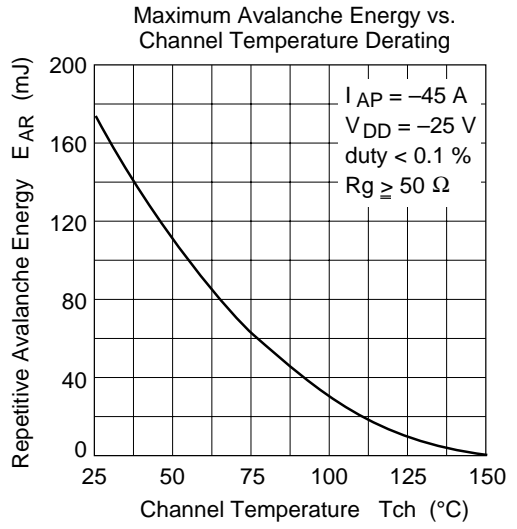
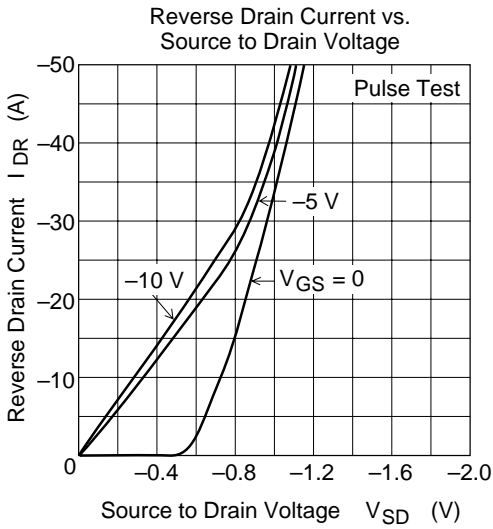
- Note: 4. Pulse test

Main Characteristics

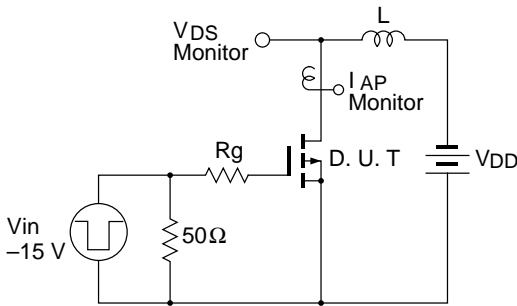






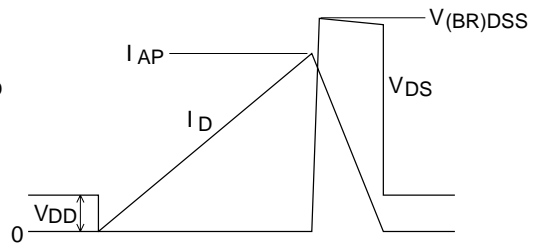


Avalanche Test Circuit

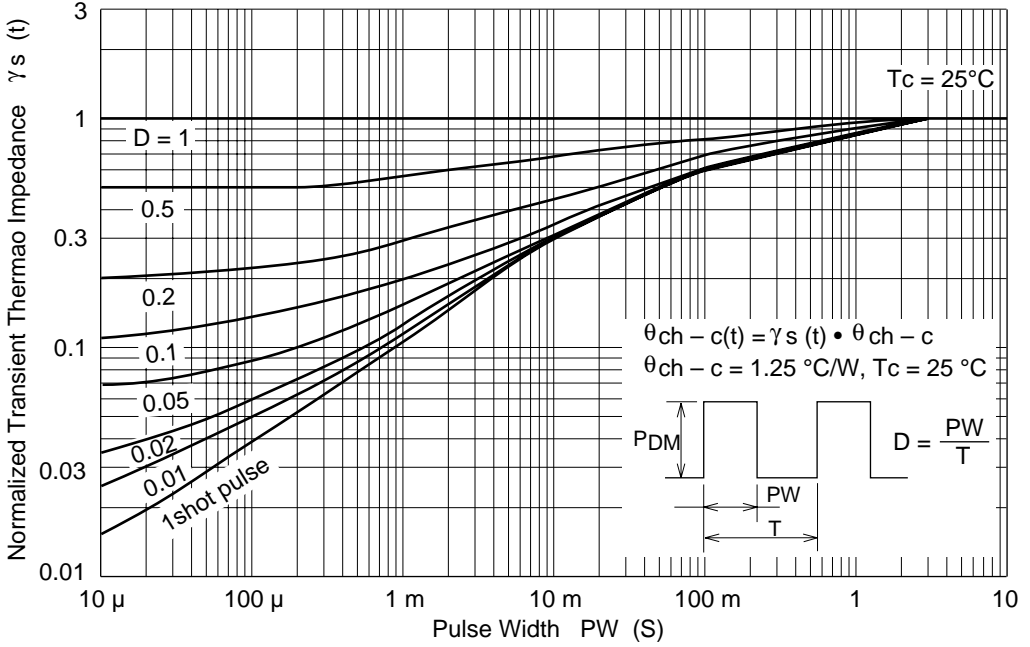


Avalanche Waveform

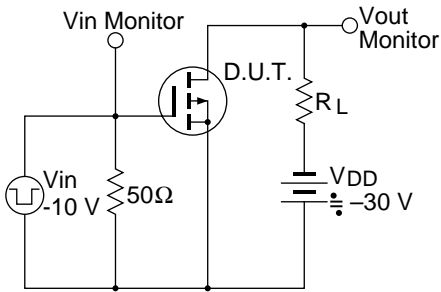
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



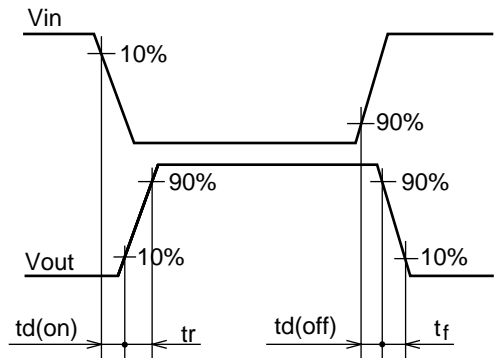
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

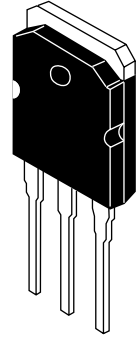
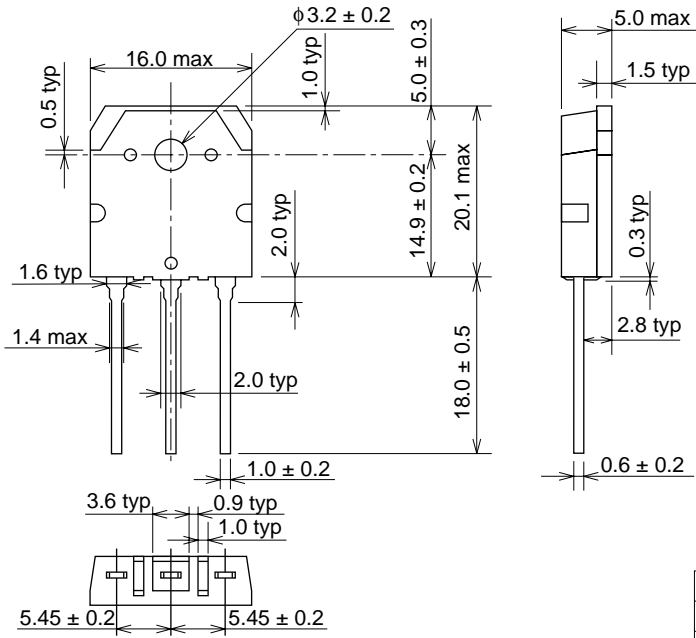


Waveform



Package Dimensions

Unit: mm



Hitachi Code	TO-3P
EIAJ	SC-65
JEDEC	—



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## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>  
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## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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