

2SJ586

Silicon P Channel MOS FET
High Speed Switching

HITACHI

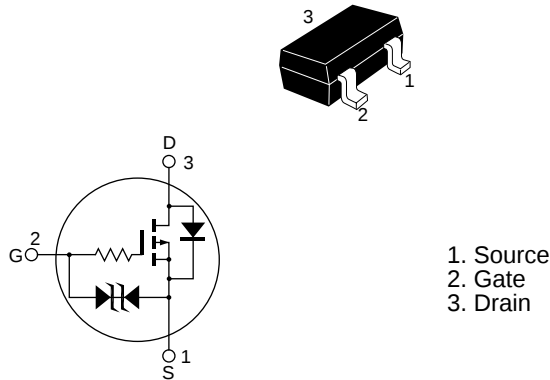
ADE-208-771A (Z)
2nd.Edition.
June 1999

Features

- Low on-resistance
 $R_{DS} = 4.1 \Omega$ typ. ($V_{GS} = -4 \text{ V}$, $I_D = -50 \text{ mA}$)
 $R_{DS} = 6.0 \Omega$ typ. ($V_{GS} = -2.5 \text{ V}$, $I_D = -50 \text{ mA}$)
- 2.5 V gate drive device.
- Small package (COMPAK)

Outline

COMPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-20	V
Gate to source voltage	V_{GSS}	± 10	V
Drain current	I_D	-100	mA
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-400	mA
Body-drain diode reverse drain current	I_{DR}	-100	mA
Channel dissipation	P_{ch} ^{Note 2}	300	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Note: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value on the alumina ceramic board (12.5x 20 x0.7 mm)

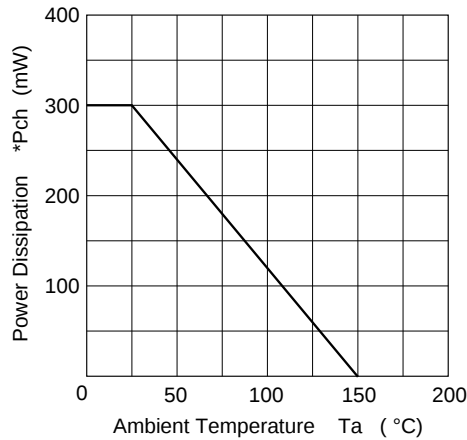
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 10	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 8 V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -20 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.8	—	-1.8	V	$I_D = -10 \mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.1	5.0	Ω	$I_D = -50 mA, V_{GS} = -4 V$ ^{Note 3}
	$R_{DS(on)}$	—	6.0	8.5	Ω	$I_D = -50 mA, V_{GS} = -2.5 V$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	94	144	—	mS	$I_D = -50 mA, V_{DS} = -10 V$ ^{Note 3}
Input capacitance	C_{iss}	—	28	—	pF	$V_{DS} = -10 V$
Output capacitance	C_{oss}	—	21	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	7	—	pF	$f = 1 MHz$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = -50 mA, V_{GS} = -4 V$
Rise time	t_r	—	90	—	ns	$R_L = 200 \Omega$
Turn-off delay time	$t_{d(off)}$	—	87	—	ns	
Fall time	t_f	—	97	—	ns	

Note: 3. Pulse test
4. Marking is CP

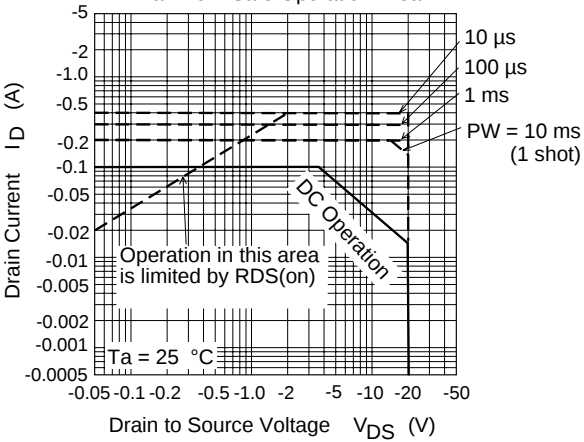
Main Characteristics

Power vs. Temperature Derating



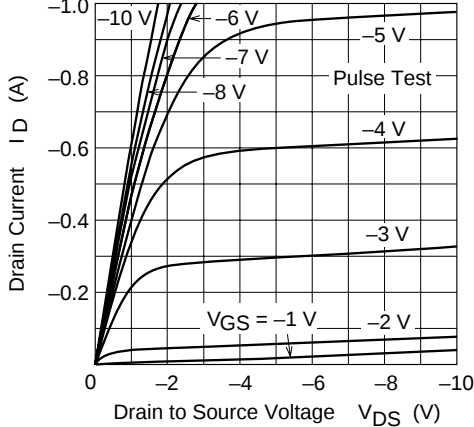
*Value on the alumina ceramic board.(12.5x20x0.7mm)

Maximum Safe Operation Area

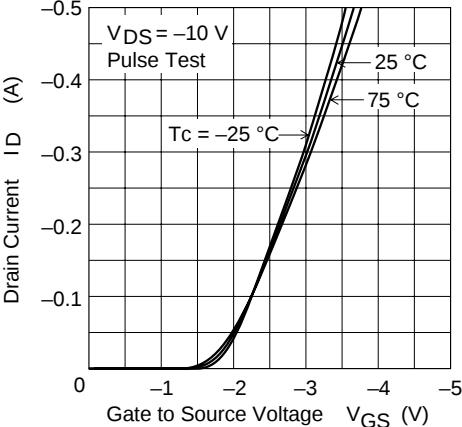


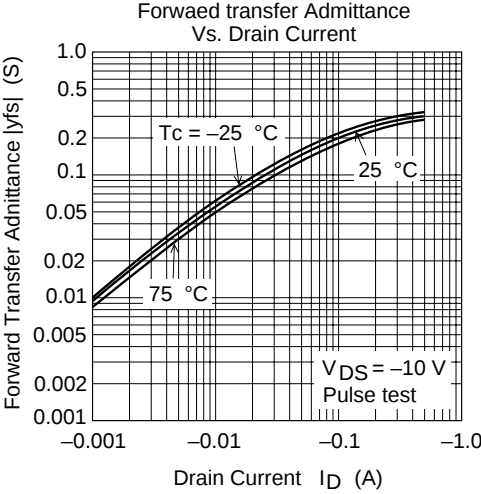
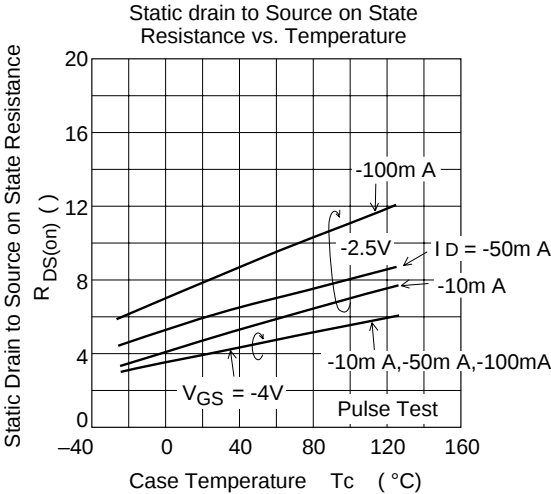
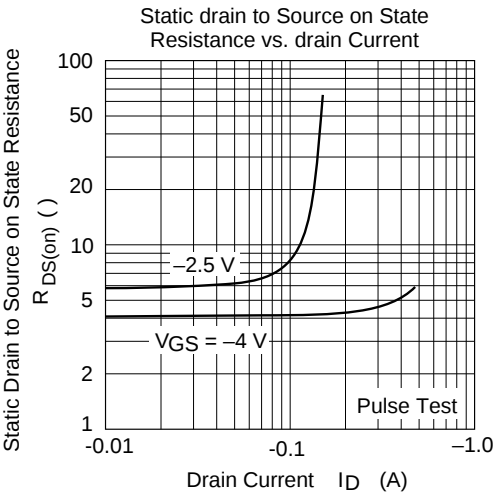
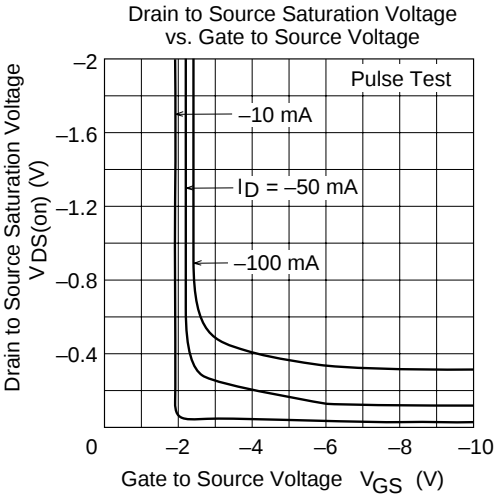
Value on the alumina ceramic board.(12.5x20x0.7mm)

Typical Output Characteristics

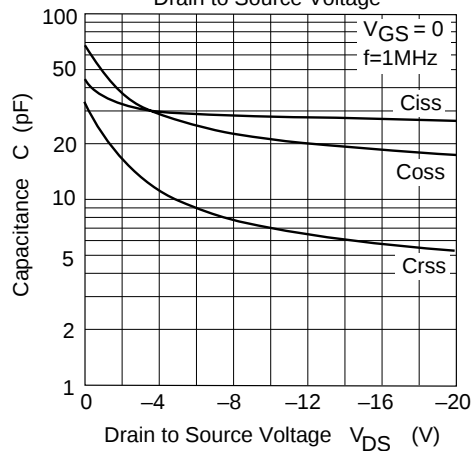


Typical Transfer Characteristics

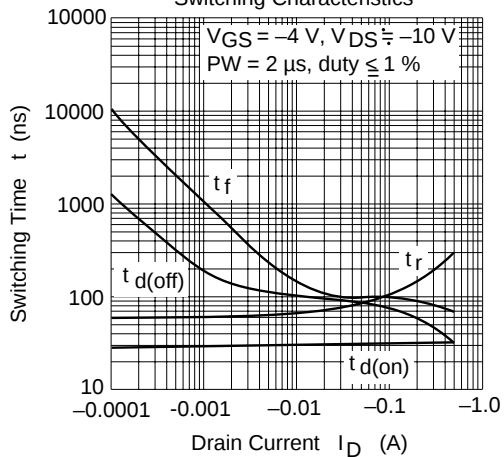




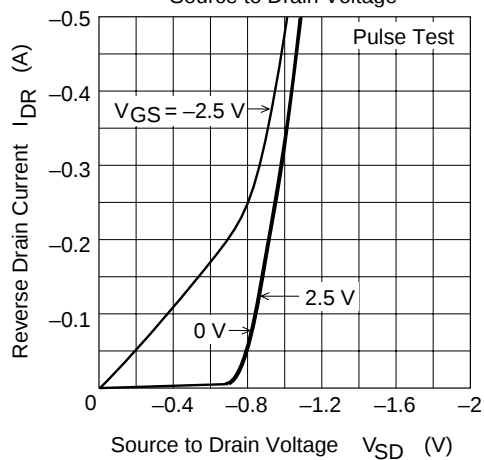
Typical Capacitance vs.
Drain to Source Voltage



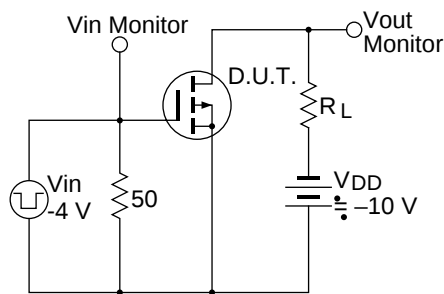
Switching Characteristics



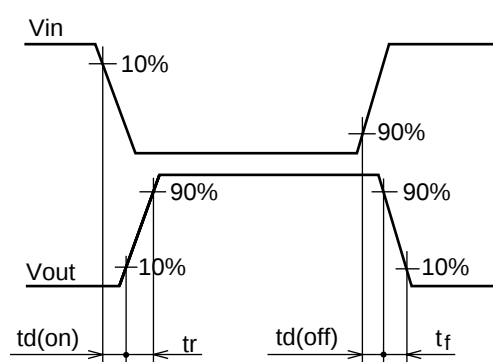
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit

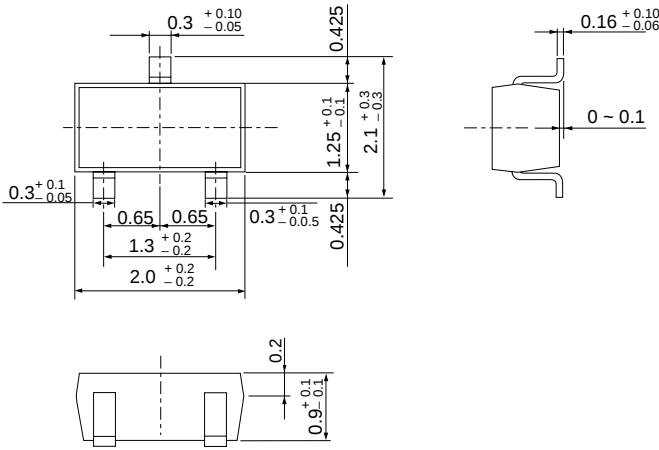


Waveforms



Package Dimensions

Unit: mm



Hitachi Code	CMPAK
EIAJ	SC-70
JEDEC	—

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