2SK1304

Silicon N-Channel MOS FET

HITACHI

ADE-208-1262 (Z)
1st. Edition
Mar. 2001

Application

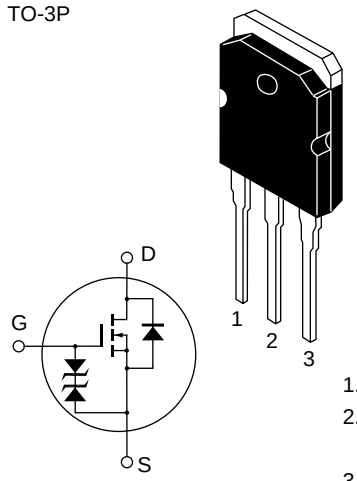
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  — Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

Outline

TO-3P



1. Gate
2. Drain
   (Flange)
3. Source

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*[1]	160	A
Body to drain diode reverse drain current	I_{DR}	40	A
Channel dissipation	Pch*[2]	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

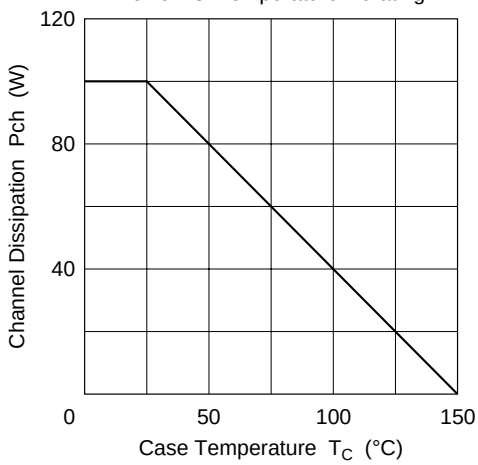
Notes: 1. PW 10 µs, duty cycle 1%
2. Value at T_C = 25°C

Electrical Characteristics (Ta = 25°C)

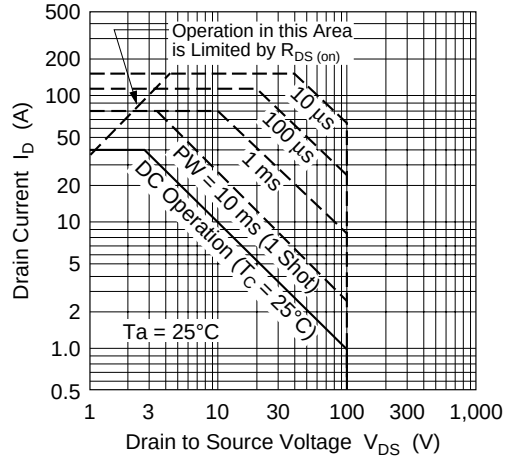
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.025	0.03		I_D = 20 A, V_{GS} = 10 V *[1]
		—	0.03	0.04		I_D = 20 A, V_{GS} = 4 V *[1]
Forward transfer admittance	|yfs|	22	35	—	S	I_D = 20 A, V_{DS} = 10 V *[1]
Input capacitance	Ciss	—	3500	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	1400	—	pF	
Reverse transfer capacitance	Crss	—	340	—	pF	
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	I_D = 20 A, V_{GS} = 10 V, R_L = 1.5
Rise time	t_r	—	170	—	ns	
Turn-off delay time	$t_{d(off)}$	—	730	—	ns	
Fall time	t_f	—	300	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	300	—	ns	I_F = 40 A, V_{GS} = 0, di_F/dt = 50 A/µs

Note: 1. Pulse test

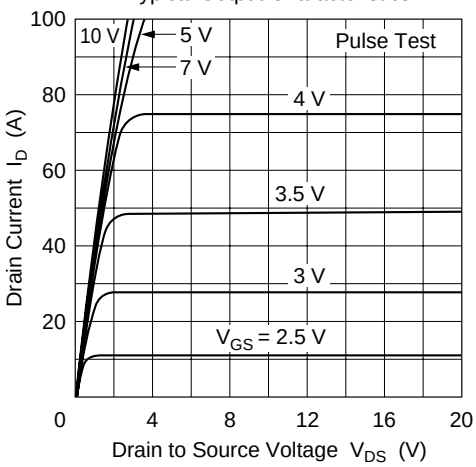
Power vs. Temperature Derating



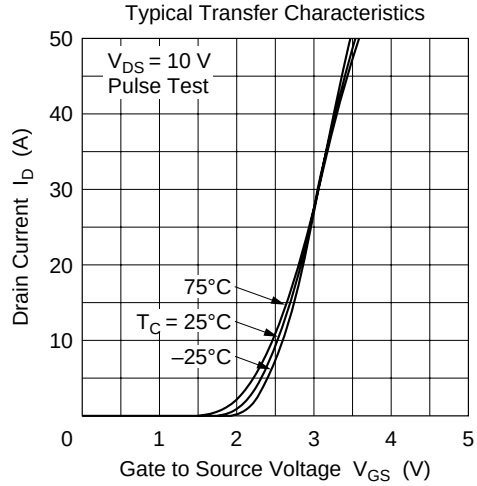
Maximum Safe Operation Area

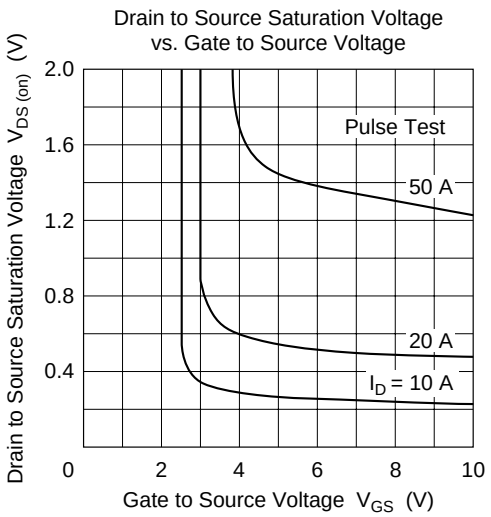


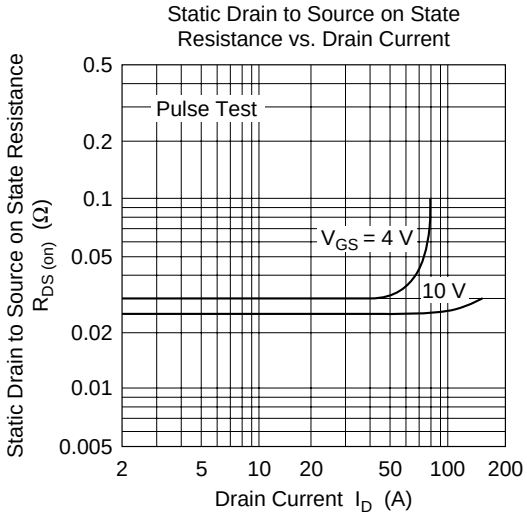
Typical Output Characteristics

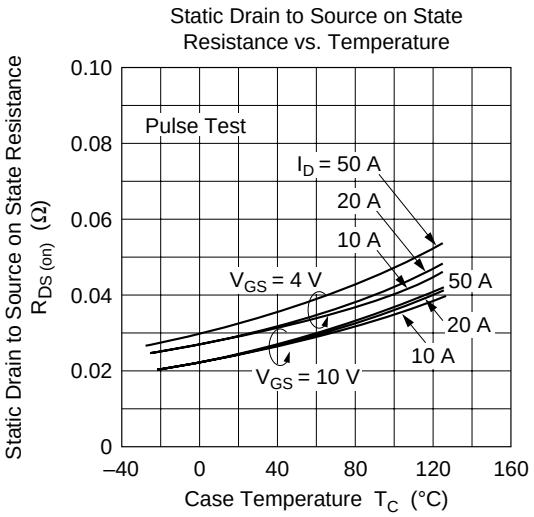


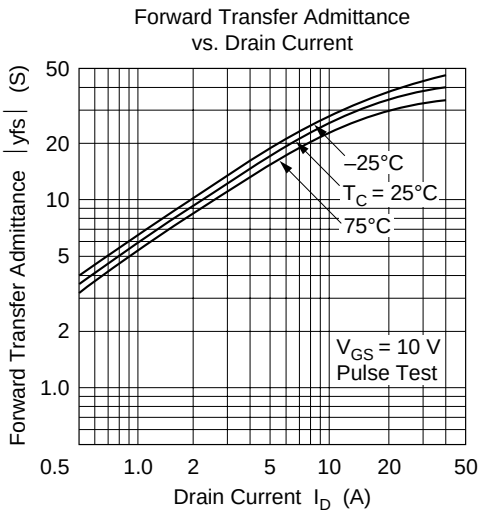
Typical Transfer Characteristics



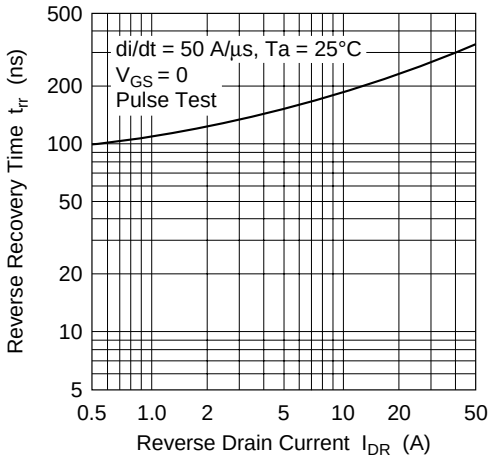

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS(on)}$ (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)
Pulse Test
50 A
20 A
I_D = 10 A


Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
$R_{DS(on)}$ (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I_D (A)
Pulse Test
V_{GS} = 4 V
10 V

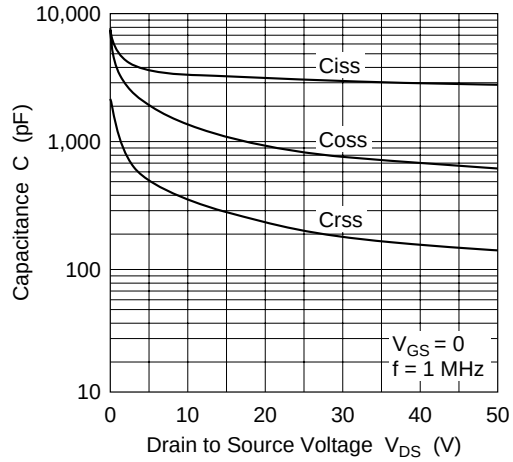

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
$R_{DS(on)}$ (Ω)
0.10
0.08
0.06
0.04
0.02
0
–40
0
40
80
120
160
Case Temperature T_C (°C)
Pulse Test
I_D = 50 A
20 A
10 A
V_{GS} = 4 V
50 A
20 A
10 A
V_{GS} = 10 V


Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1.0
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)
–25°C
T_C = 25°C
75°C
V_{GS} = 10 V
Pulse Test

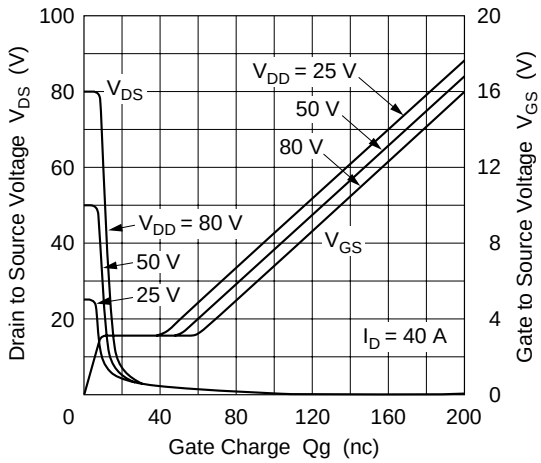
Body to Drain Diode Reverse Recovery Time



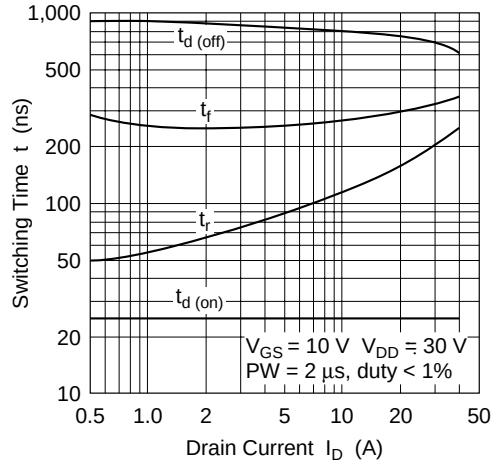
Typical Capacitance vs. Drain to Source Voltage



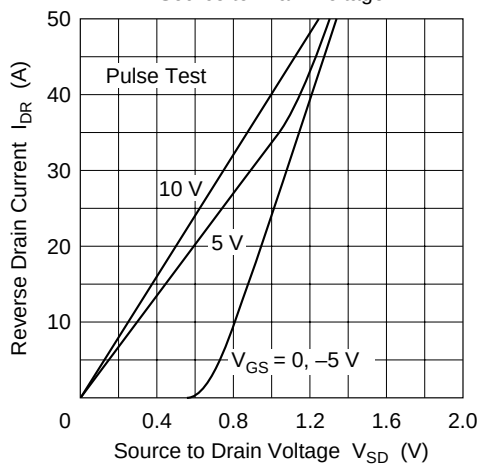
Dynamic Input Characteristics



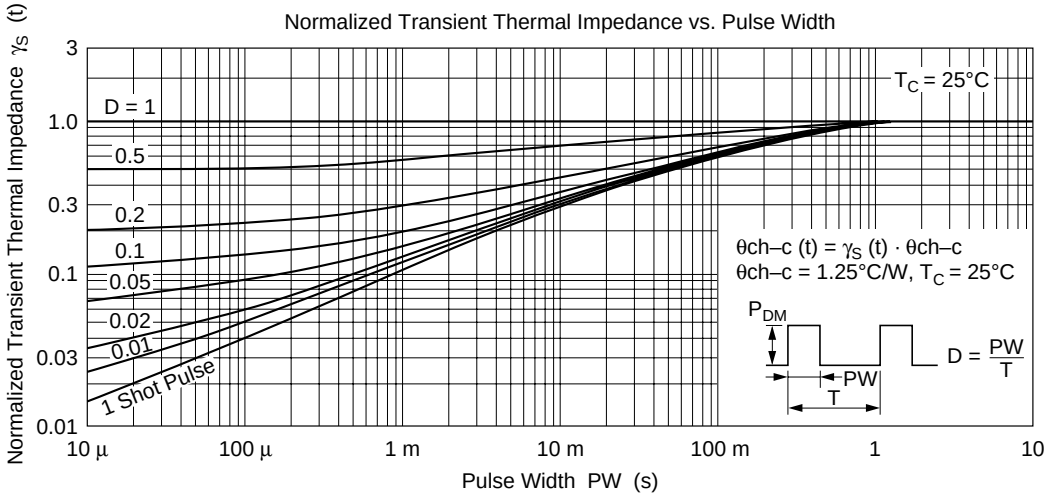
Switching Characteristics



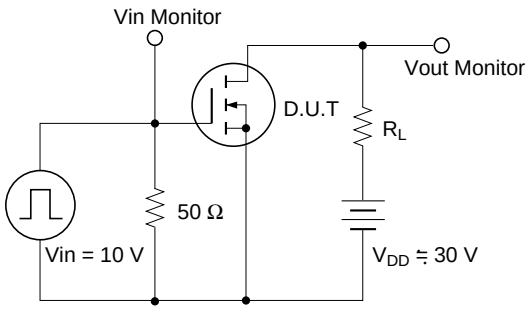
Reverse Drain Current vs.
Source to Drain Voltage



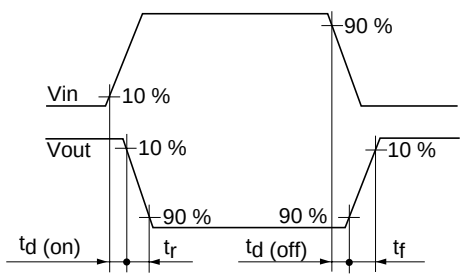
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



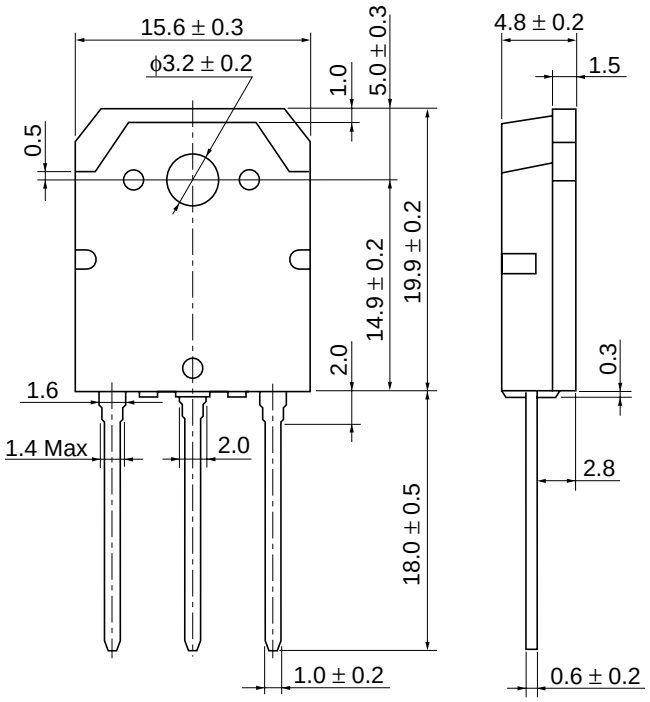
Wavewforms

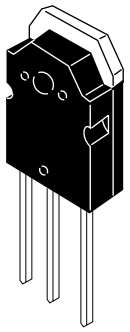


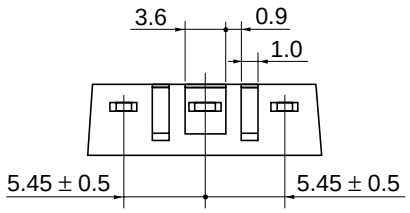
Package Dimensions

As of January, 2001

Unit: mm







Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

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