
2SK1579

Silicon N-Channel MOS FET

HITACHI

Application

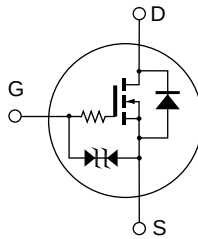
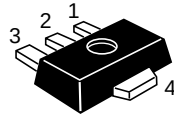
High speed power switching

Features

- Low on-resistance
- High speed switching
- Suitable for low voltage operation

Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C unless otherwise specified.)

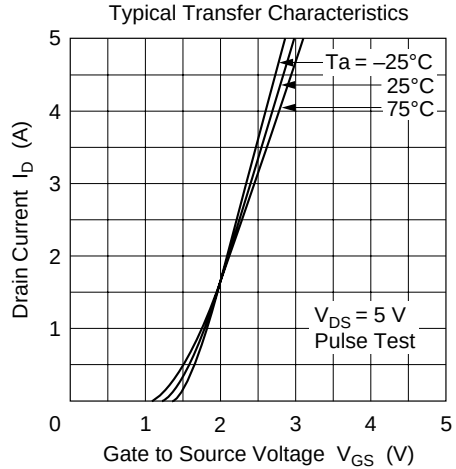
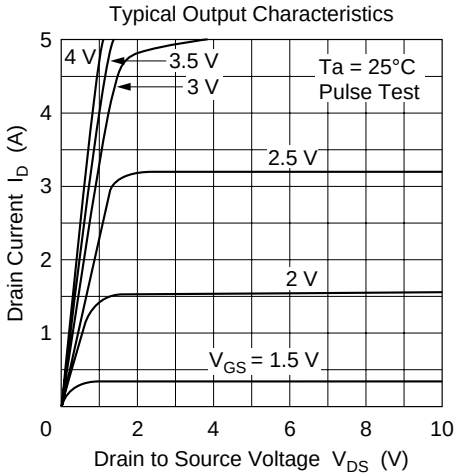
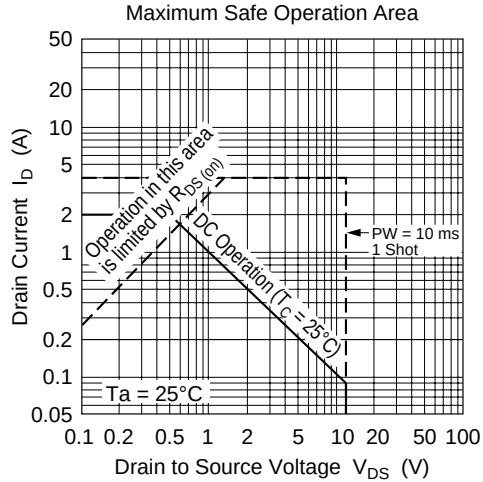
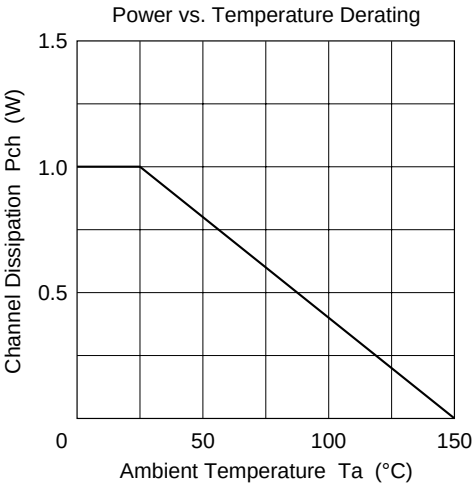
Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	12	V
Gate to source voltage	V _{GSS}	±7	V
Drain current	I _D	2	A
Drain peak current	I _{D(pulse)} ^{*1}	4	A
Body to drain diode reverse drain current	I _{DR}	2	A
Channel power dissipation	Pch ^{*2}	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

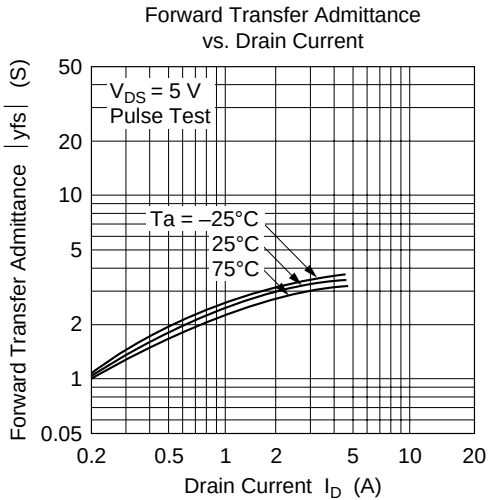
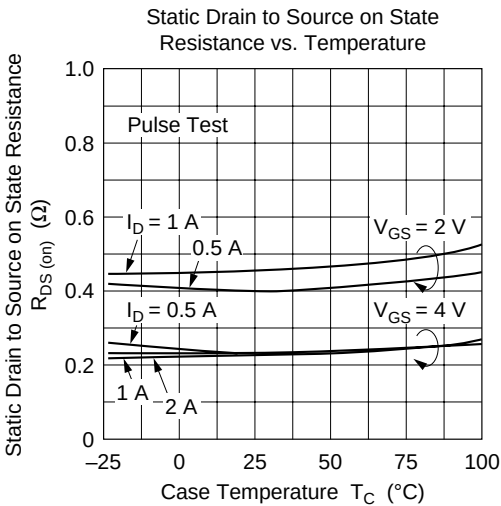
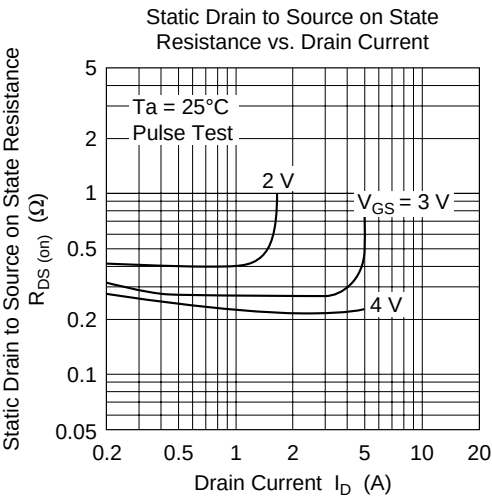
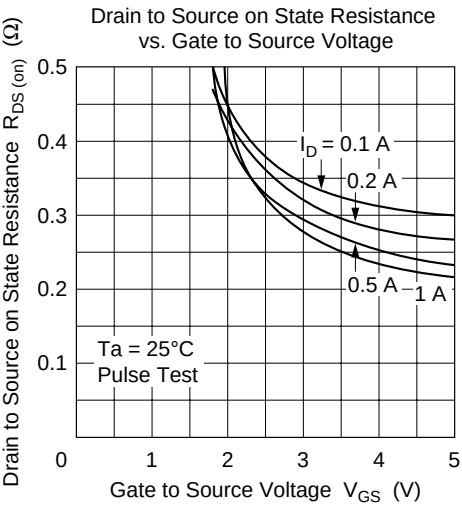
Notes 1. PW ≤ 100 μs, duty cycle ≤ 10%
2. Value on the alumina ceramic board (12.5 × 20 × 0.7 mm)

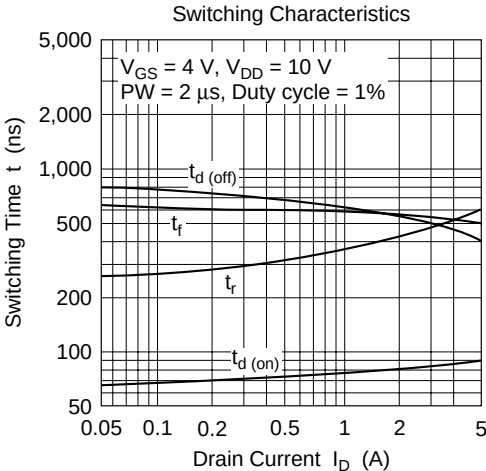
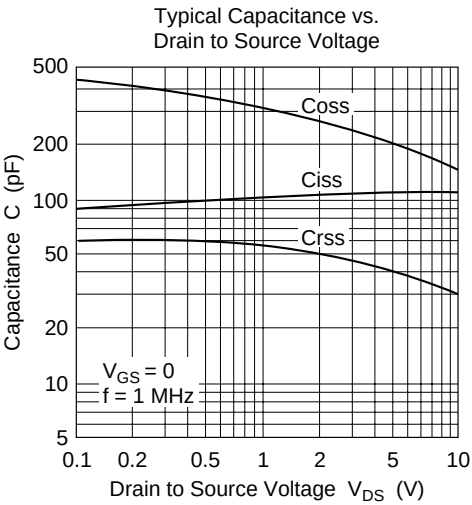
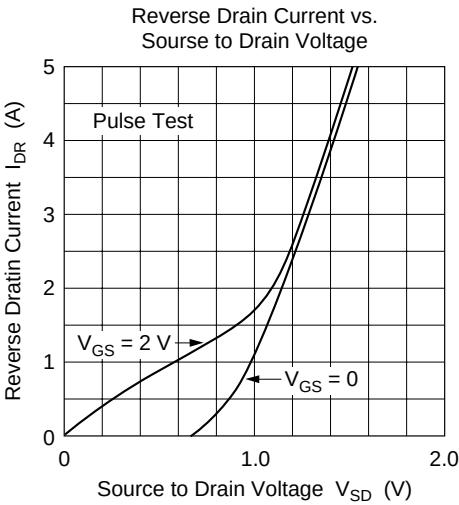
Electrical Characteristics (Ta = 25°C unless otherwise specified.)

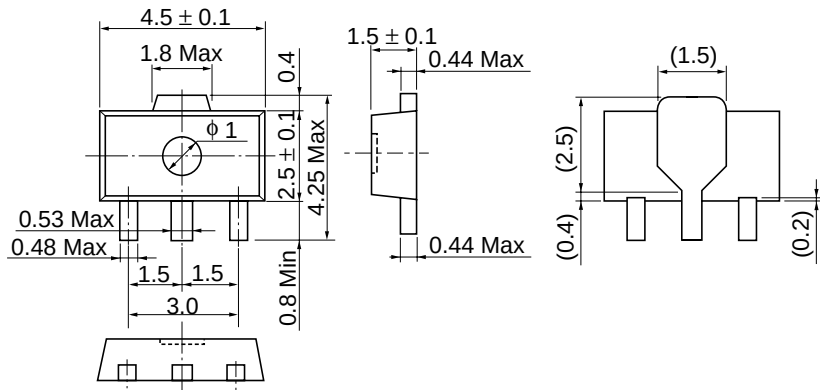
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source cutoff current	I_{DSS}	—	—	1	μA	$V_{DS} = 8 V, V_{GS} = 0$
Gate to source cutoff current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 6.5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 5 V, I_D = 100 \mu A$
Drain to source on resistance (1)	$R_{DS(on)1}$	—	0.36	0.7	Ω	$V_{GS} = 2.2 V, I_D = 0.5 A$
Drain to source on resistance (2)	$R_{DS(on)2}$	—	0.25	0.35	Ω	$V_{GS} = 4 V, I_D = 1 A$
DC forward transfer admittance	$ y_{fs} $	1	2.5	—	S	$V_{DS} = 5 V, I_D = 1 A,$ $\Delta V_{GS} = 0.1 V$
Input capacitance	C_{iss}	—	110	—	pF	$V_{DS} = 5 V, V_{GS} = 0,$ $f = 1 MHz$
Reverse transfer capacitance	C_{rss}	—	30	—	pF	
Output capacitance	C_{oss}	—	150	—	pF	
Turn-on time	$t_{(on)}$	—	500	—	ns	$I_D = 0.2 A, V_{GS} = 0,$
Turn-off time	$t_{(off)}$	—	1500	—	ns	$V_{in} = 4 V, R_L = 51 \Omega$

Note 1. Marking is "DY".









Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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