

# 2SK2247

Silicon N-Channel MOS FET

# HITACHI

ADE-208-1353 (Z)  
1st. Edition  
Mar. 2001

## Application

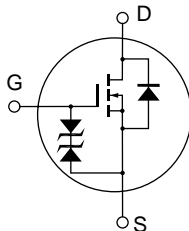
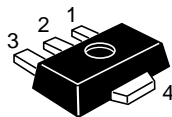
High speed power switching

## Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source.
- Suitable for DC-DC converter, motor drive, power switch, solenoid drive

## Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

**Absolute Maximum Ratings (Ta = 25°C)**

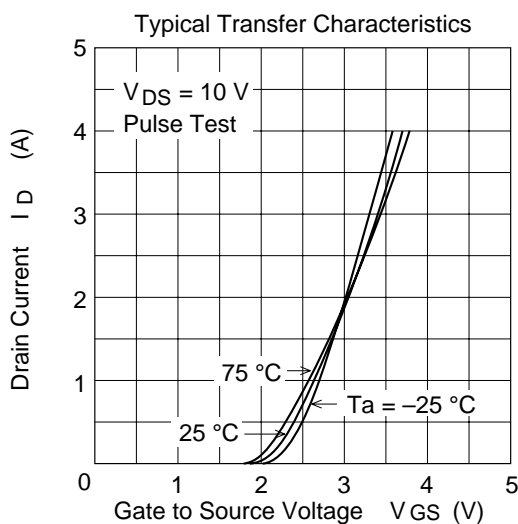
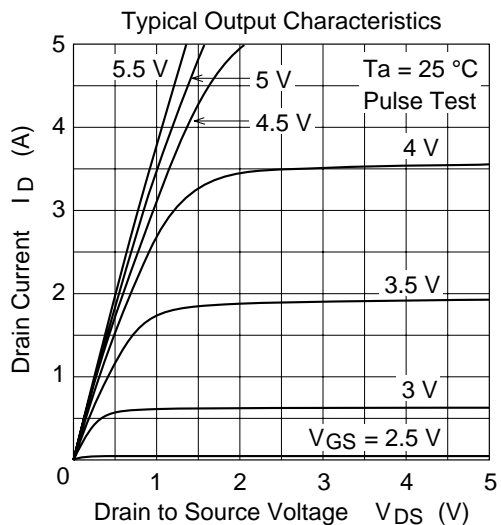
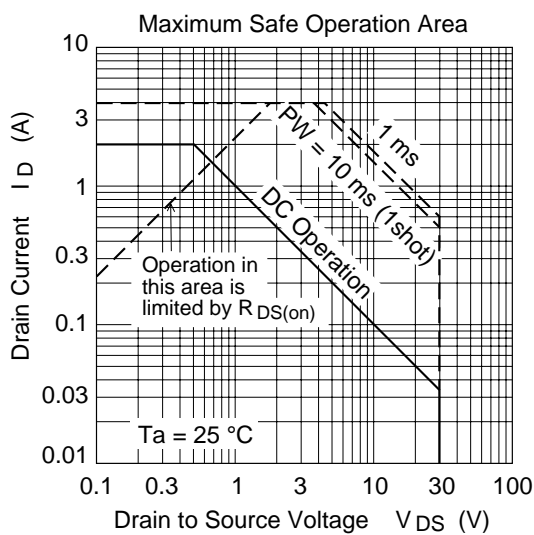
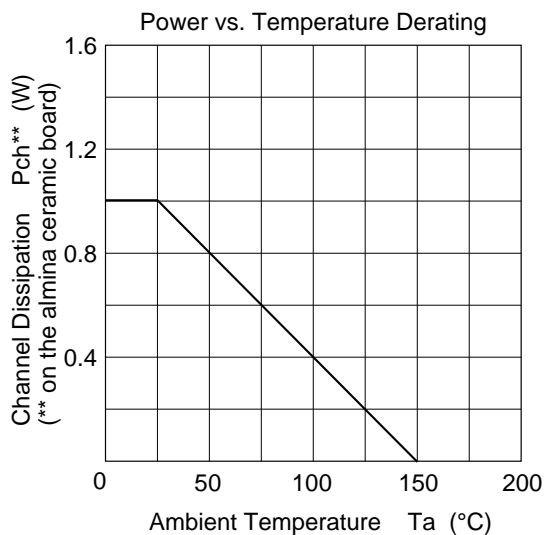
Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	2	A
Drain peak current	$I_{D(pulse)}^{*1}$	4	A
Body to drain diode reverse drain current	$I_{DR}$	2	A
Channel dissipation	Pch*2	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

- Notes
1.  $PW \leq 100 \mu s$ , duty cycle  $\leq 10 \%$
  2. When using the alumina ceramic board (12.5 × 20 × 0.7mm)
  3. Marking is "QY"

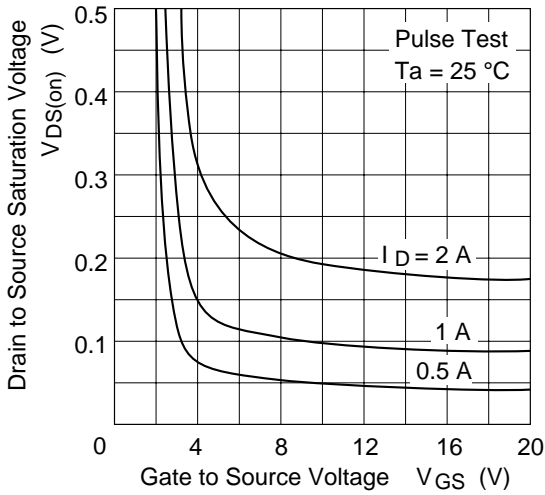
**Electrical Characteristics (Ta = 25°C)**

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 10 \mu A$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5	μA	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	μA	$V_{DS} = 24 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	1.5	2.0	V	$I_D = 100 \mu A$ , $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.45	Ω	$I_D = 1 \text{ A}$ $V_{GS} = 4 \text{ V}^{*1}$
		—	0.22	0.35	Ω	$I_D = 1 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.5	1.9	—	S	$I_D = 1 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	Ciss	—	177	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	116	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	43	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	8	—	ns	$I_D = 1 \text{ A}$
Rise time	$t_r$	—	14	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	37	—	ns	$R_L = 30 \Omega$
Fall time	$t_f$	—	33	—	ns	PW = 2 μs

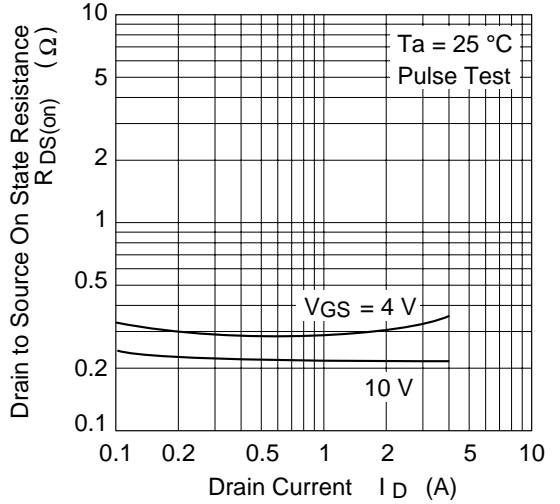
Note 1. Pulse Test



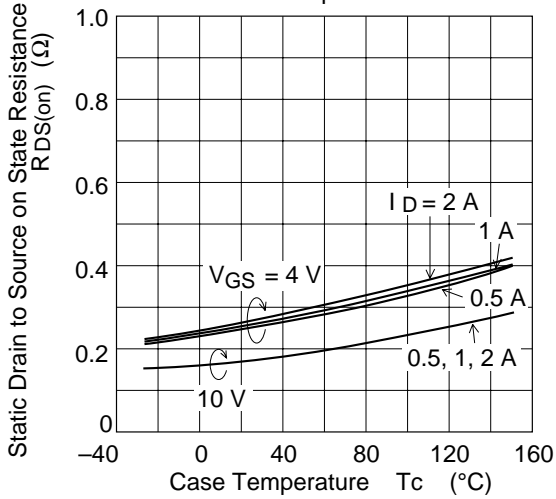
Drain to Source Saturation Voltage vs. Gate to Source Voltage



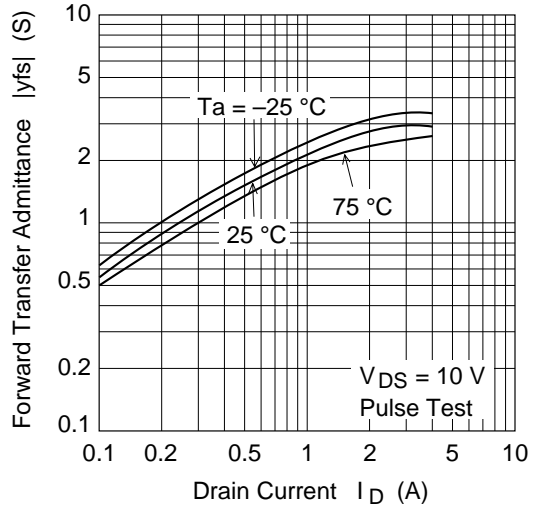
Static Drain to Source State Resistance vs. Drain Current



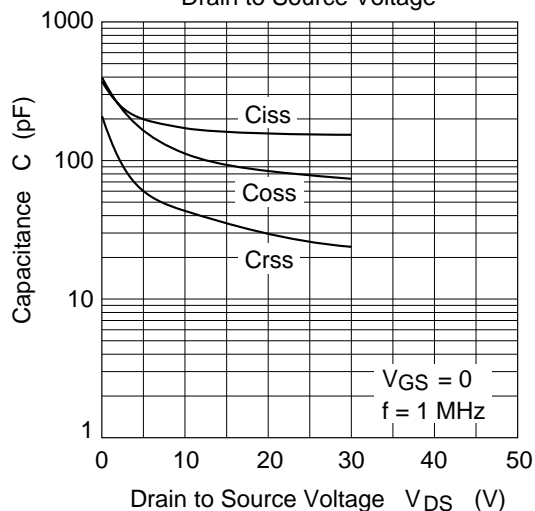
Static Drain to Source on State Resistance vs. Temperature



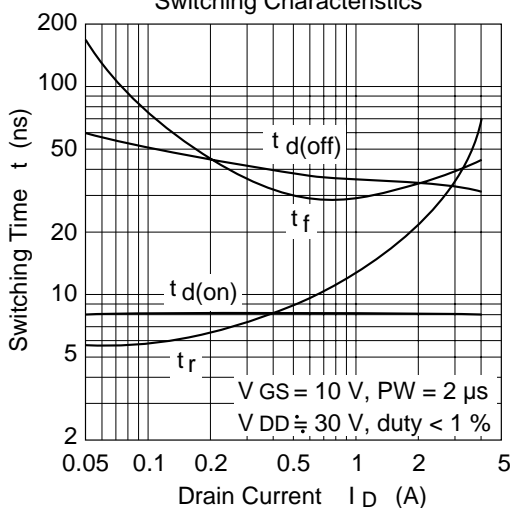
Forward Transfer Admittance vs. Drain Current



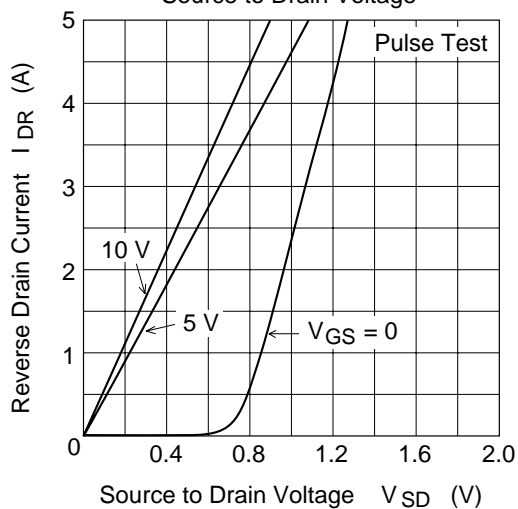
Typical Capacitance vs. Drain to Source Voltage



Switching Characteristics

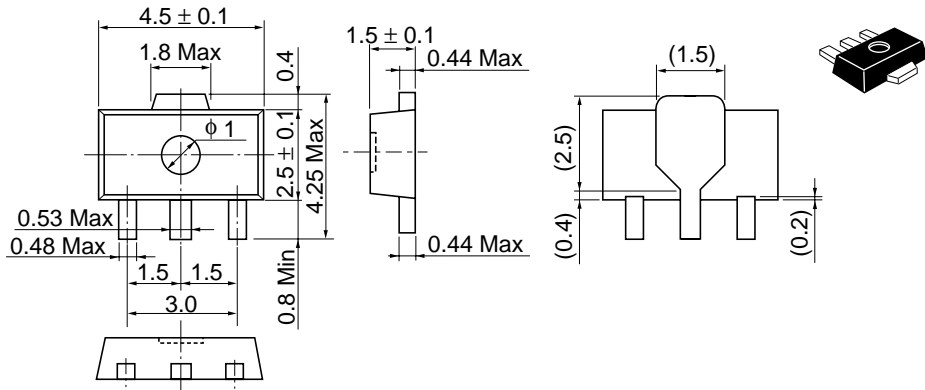


Reverse Drain Current vs. Source to Drain Voltage



Package Dimensions

As of January, 2001  
Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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