

2SK2788

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

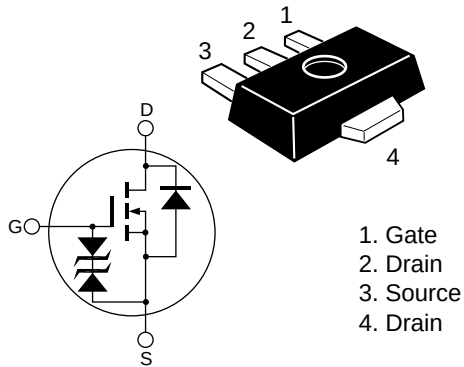
ADE-208-538
1st. Edition

Features

- Low on-resistance
 $R_{DS(on)} = 0.12\Omega$ typ ($V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$)
- Low drive current
- High speed switching
- 4V gate drive devices.

Outline

UPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	2	A
Drain peak current	I _{D(pulse)} ^{*1}	4	A
Body to drain diode reverse drain current	I _{DR}	2	A
Channel dissipation	Pch ^{*2}	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

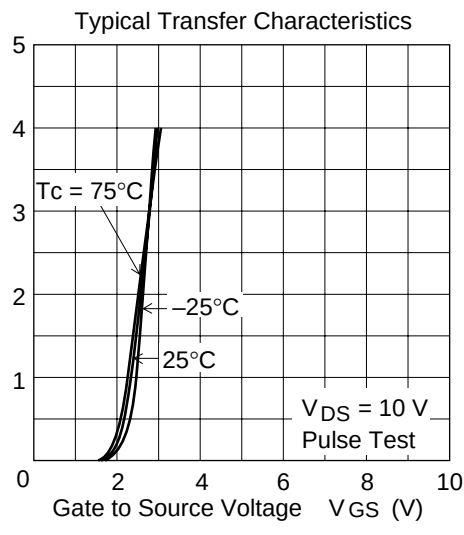
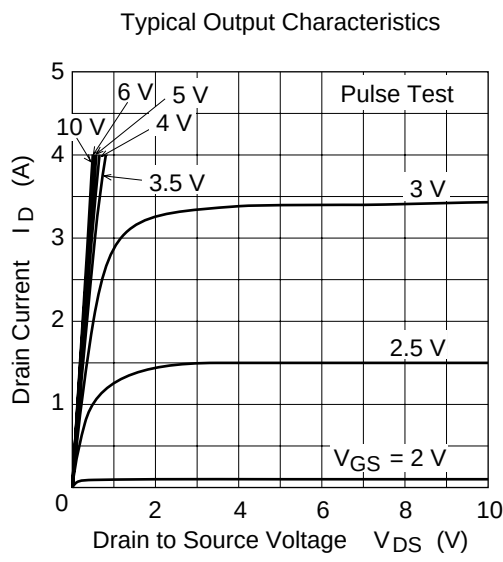
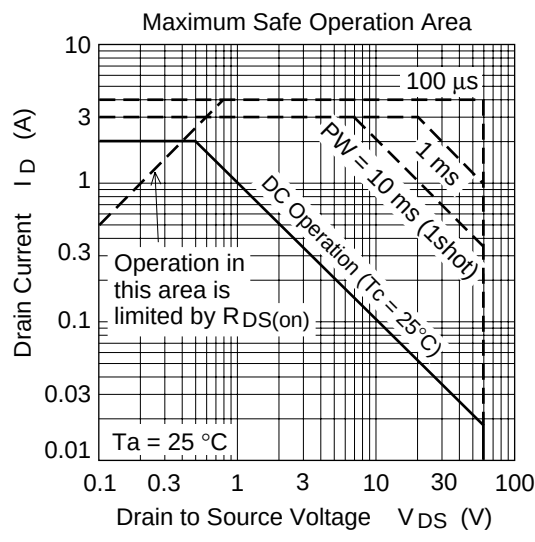
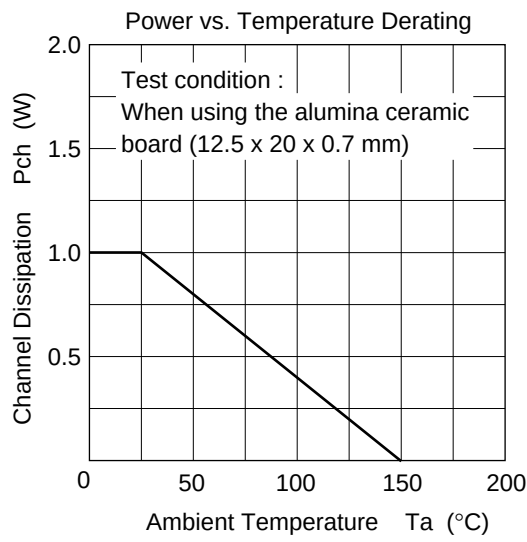
Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

Electrical Characteristics ($T_a = 25^\circ\text{C}$)

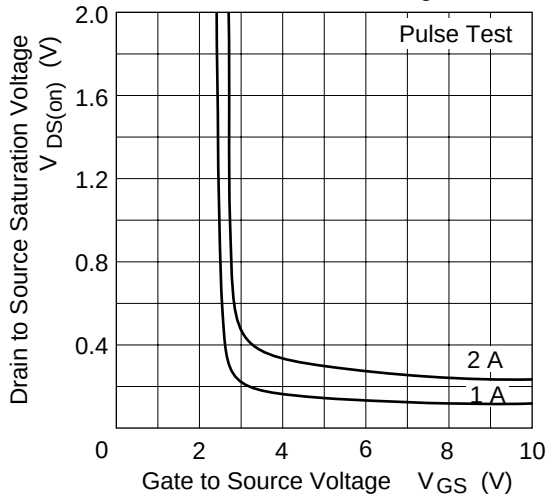
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	$I_D = 1\text{A}$, $V_{GS} = 10\text{V}^{*1}$
	$R_{DS(on)}$	—	0.16	0.25	Ω	$I_D = 1\text{A}$, $V_{GS} = 4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.6	2.8	—	S	$I_D = 1\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	C_{iss}	—	180	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	90	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	30	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	9	—	ns	$V_{GS} = 10\text{V}$, $I_D = 1\text{A}$
Rise time	t_r	—	15	—	ns	$R_L = 30\Omega$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	35	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_D = 2\text{A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 2\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

Notes: 1. Pulse test
2. Marking is "VY"

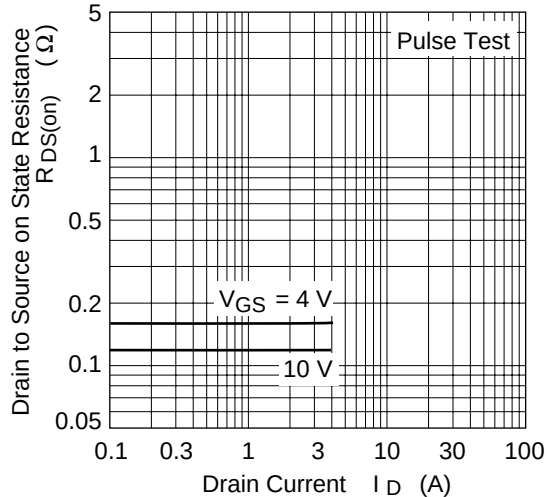
Main Characteristics



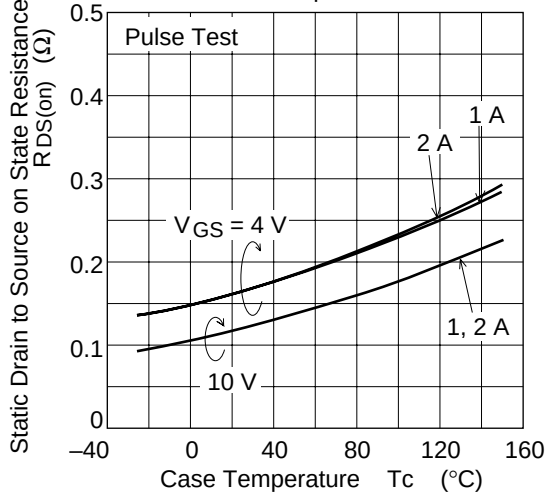
Drain to Source Saturation Voltage vs. Gate to Source Voltage



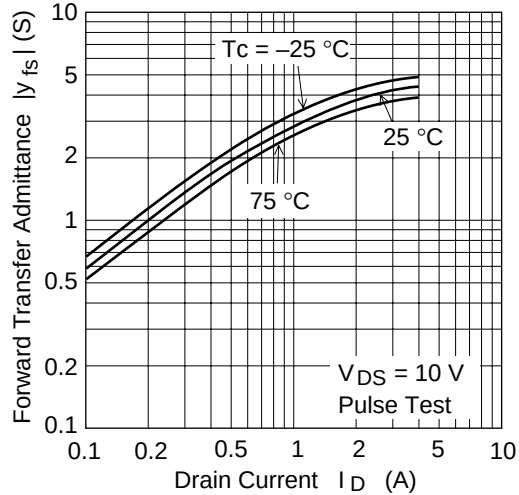
Static Drain to Source on State Resistance vs. Drain Current



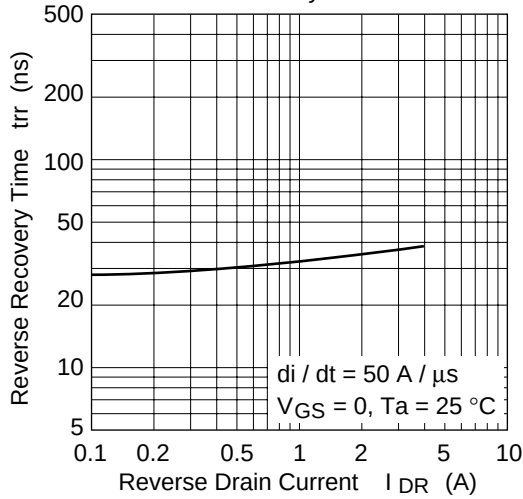
Static Drain to Source on State Resistance vs. Temperature



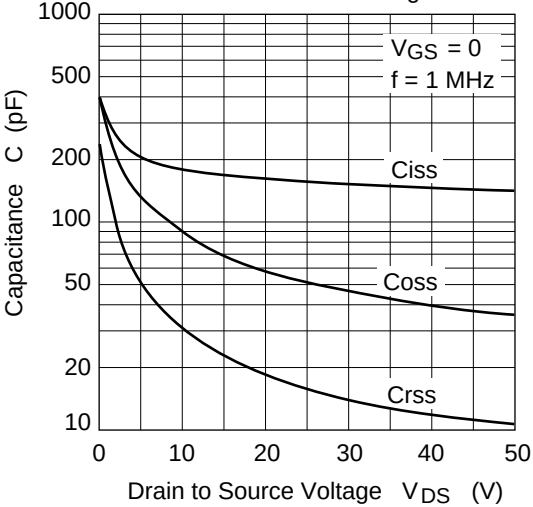
Forward Transfer Admittance vs. Drain Current



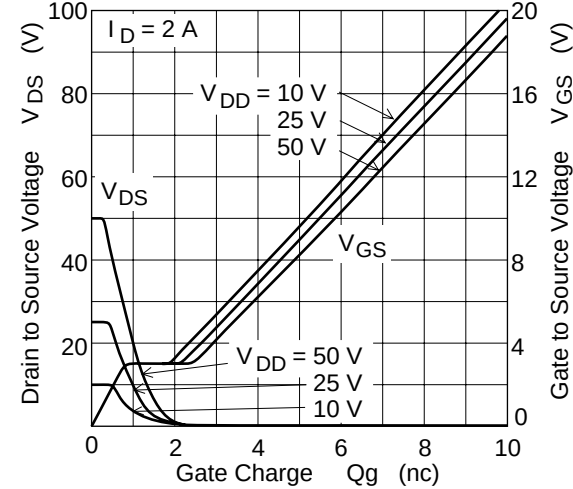
Body to Drain Diode Reverse Recovery Time



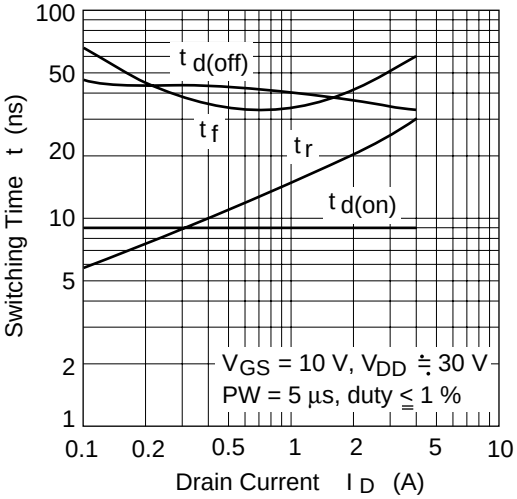
Typical Capacitance vs. Drain to Source Voltage

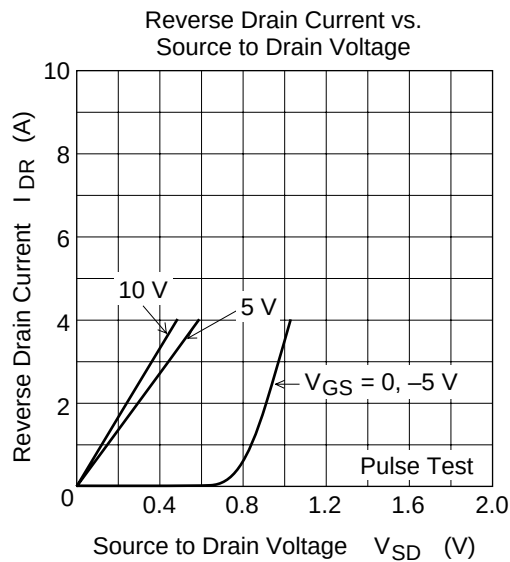


Dynamic Input Characteristics

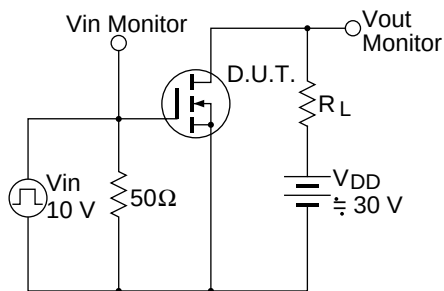


Switching Characteristics

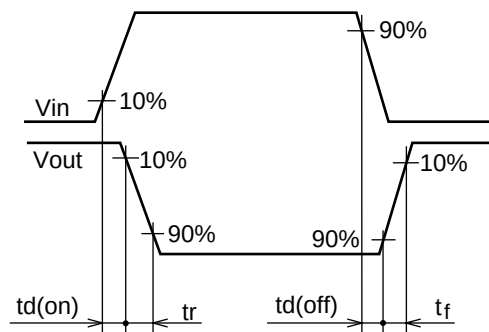




Switching Time Test Circuit

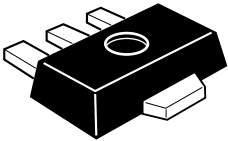
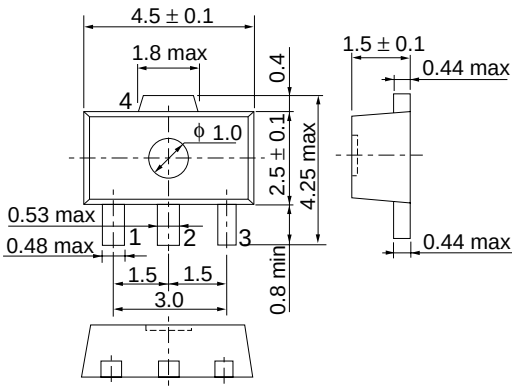


Waveform



Package Dimensions

Unit: mm



Hitachi Code	UPAK
EIAJ	SC-62
JEDEC	—

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
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Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533 Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building. No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180
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Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX
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