

# 2SK2796(L), 2SK2796(S)

Silicon N Channel MOS FET  
High Speed Power Switching

# HITACHI

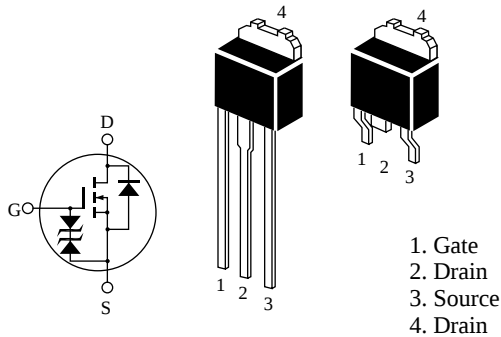
ADE-208-534C (Z)  
4th. Edition  
Jun 1998

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.12\Omega$  typ.
- 4V gate drive devices.
- High speed switching

## Outline

DPAK | 1



2SK2796(L), 2SK2796(S)

Absolute Maximum Ratings (Ta = 25°C)

| Item                                   | Symbol                 | Ratings     | Unit |
|----------------------------------------|------------------------|-------------|------|
| Drain to source voltage                | $V_{DSS}$              | 60          | V    |
| Gate to source voltage                 | $V_{GSS}$              | ±20         | V    |
| Drain current                          | $I_D$                  | 5           | A    |
| Drain peak current                     | $I_{D(pulse)}^{Note1}$ | 20          | A    |
| Body-drain diode reverse drain current | $I_{DR}$               | 5           | A    |
| Avalanche current                      | $I_{AP}^{Note3}$       | 5           | A    |
| Avalanche energy                       | $E_{AR}^{Note3}$       | 2.14        | mJ   |
| Channel dissipation                    | $P_{ch}^{Note2}$       | 20          | W    |
| Channel temperature                    | Tch                    | 150         | °C   |
| Storage temperature                    | Tstg                   | −55 to +150 | °C   |

- Note:
1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$

2. Value at Tc = 25°C

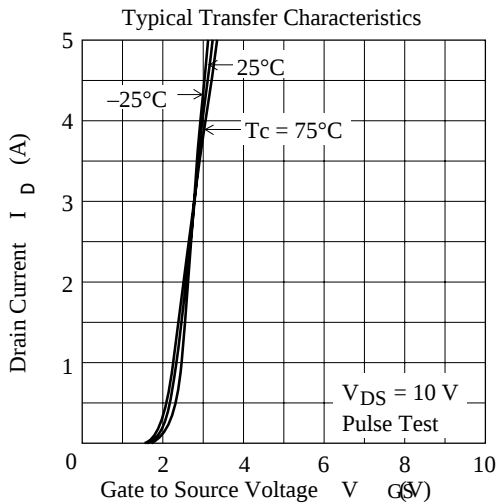
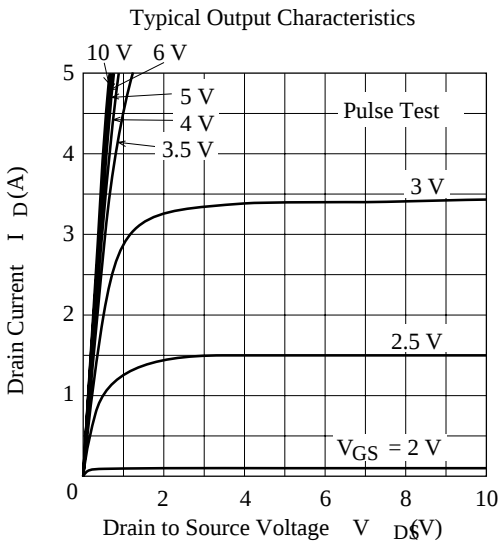
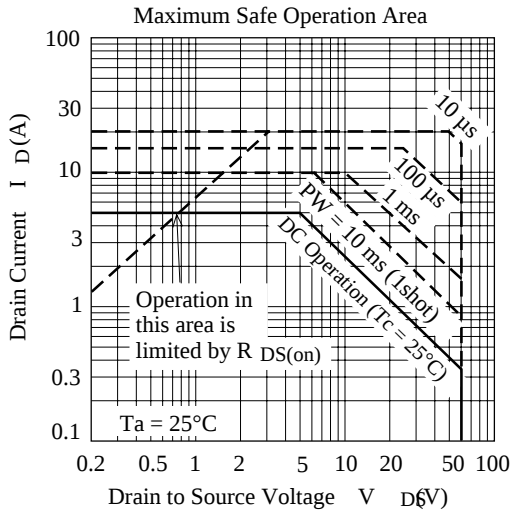
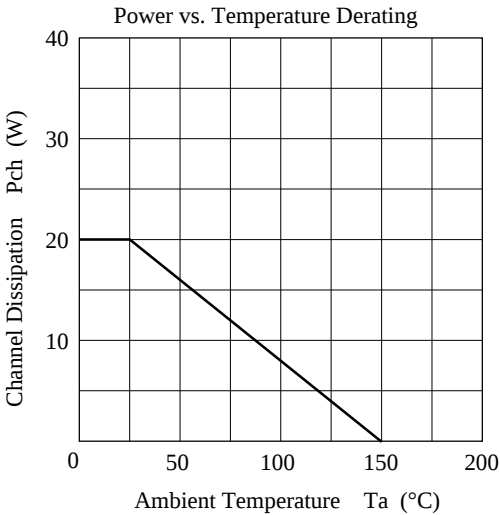
3. Value at Tch = 25°C, Rg  $\geq 50\ \Omega$

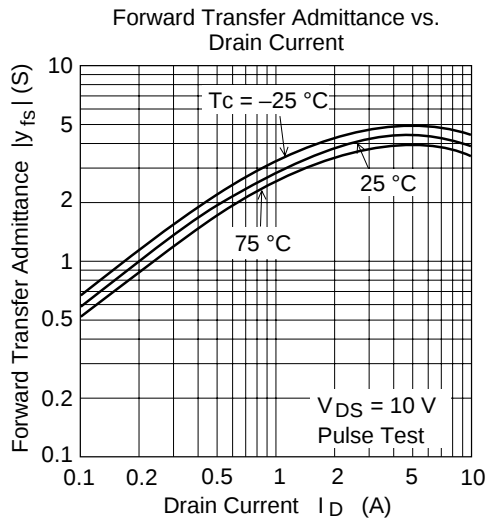
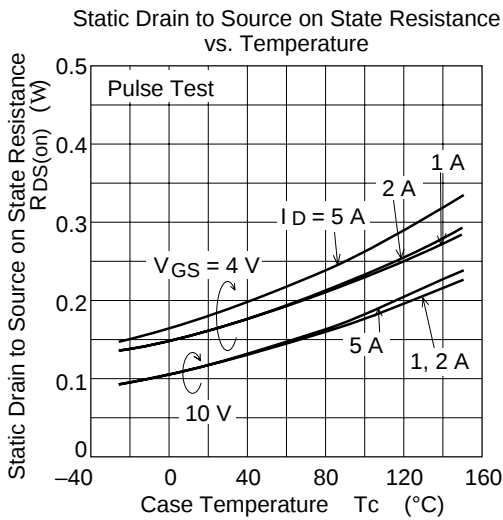
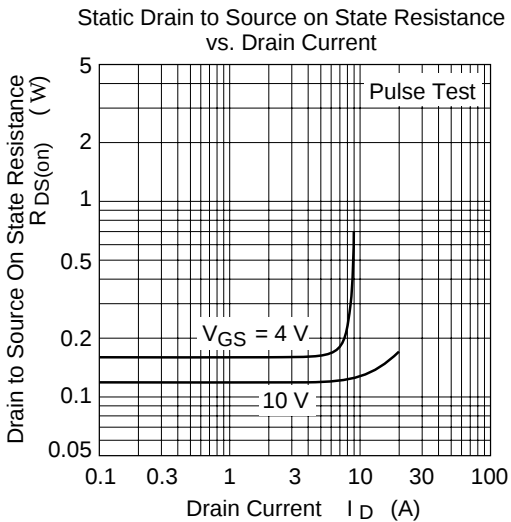
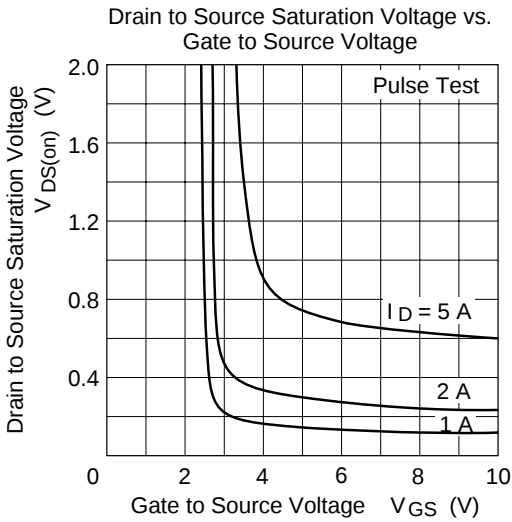
**Electrical Characteristics** (Ta = 25°C)

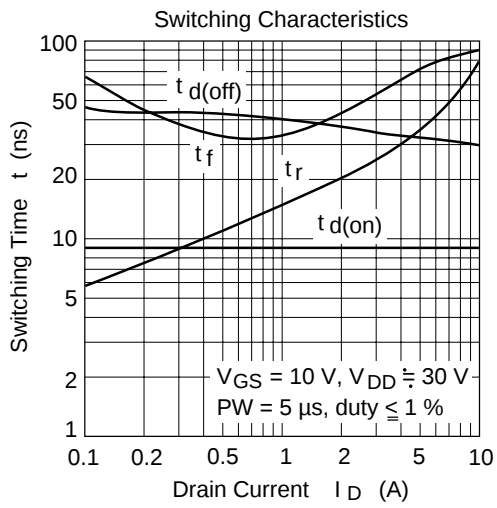
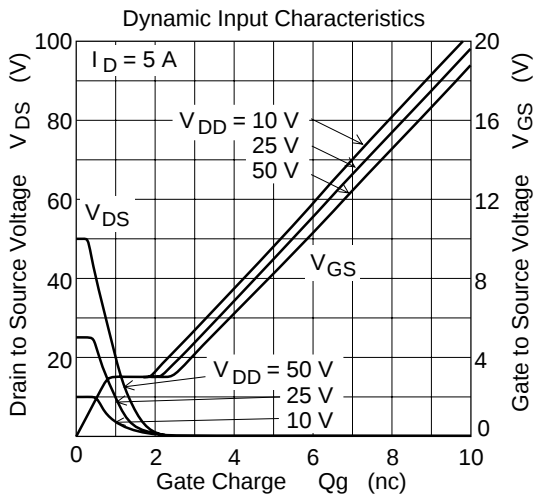
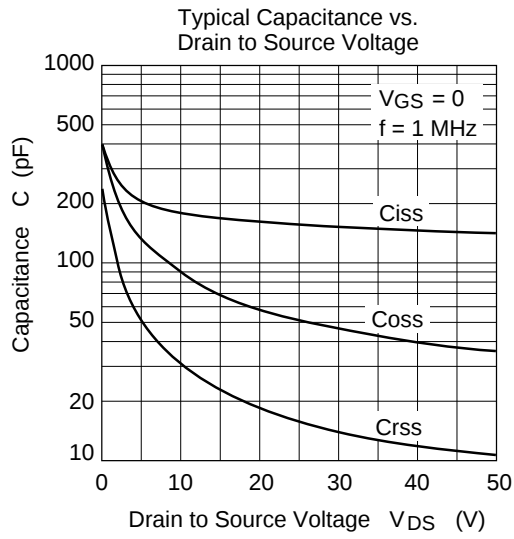
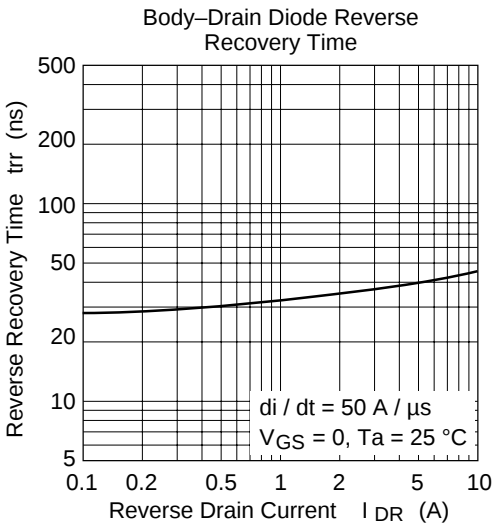
| Item                                       | Symbol        | Min      | Typ  | Max      | Unit          | Test Conditions                                                       |
|--------------------------------------------|---------------|----------|------|----------|---------------|-----------------------------------------------------------------------|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 60       | —    | —        | V             | $I_D = 10\text{mA}$ , $V_{GS} = 0$                                    |
| Gate to source breakdown voltage           | $V_{(BR)GSS}$ | $\pm 20$ | —    | —        | V             | $I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$                             |
| Zero gate voltage drain current            | $I_{DSS}$     | —        | —    | 10       | $\mu\text{A}$ | $V_{DS} = 60\text{V}$ , $V_{GS} = 0$                                  |
| Gate to source leak current                | $I_{GSS}$     | —        | —    | $\pm 10$ | $\mu\text{A}$ | $V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$                              |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 1.0      | —    | 2.0      | V             | $I_D = 1\text{mA}$ , $V_{DS} = 10\text{V}$                            |
| Static drain to source on state resistance | $R_{DS(on)}$  | —        | 0.12 | 0.16     | $\Omega$      | $I_D = 3\text{A}$ , $V_{GS} = 10\text{V}$ <sup>Note4</sup>            |
| Static drain to source on state resistance | $R_{DS(on)}$  | —        | 0.16 | 0.25     | $\Omega$      | $I_D = 3\text{A}$ , $V_{GS} = 4\text{V}$ <sup>Note4</sup>             |
| Forward transfer admittance                | $ y_{fs} $    | 2.5      | 4.0  | —        | S             | $I_D = 3\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note4</sup>            |
| Input capacitance                          | $C_{iss}$     | —        | 180  | —        | pF            | $V_{DS} = 10\text{V}$                                                 |
| Output capacitance                         | $C_{oss}$     | —        | 90   | —        | pF            | $V_{GS} = 0$                                                          |
| Reverse transfer capacitance               | $C_{rss}$     | —        | 30   | —        | pF            | $f = 1\text{MHz}$                                                     |
| Turn-on delay time                         | $t_{d(on)}$   | —        | 9    | —        | ns            | $V_{GS} = 10\text{V}$ , $I_D = 3\text{A}$                             |
| Rise time                                  | $t_r$         | —        | 25   | —        | ns            | $R_L = 10\Omega$                                                      |
| Turn-off delay time                        | $t_{d(off)}$  | —        | 35   | —        | ns            |                                                                       |
| Fall time                                  | $t_f$         | —        | 55   | —        | ns            |                                                                       |
| Body-drain diode forward voltage           | $V_{DF}$      | —        | 1.0  | —        | V             | $I_F = 5\text{A}$ , $V_{GS} = 0$                                      |
| Body-drain diode reverse recovery time     | $t_{rr}$      | —        | 40   | —        | ns            | $I_F = 5\text{A}$ , $V_{GS} = 0$<br>$diF/dt = 50\text{A}/\mu\text{s}$ |

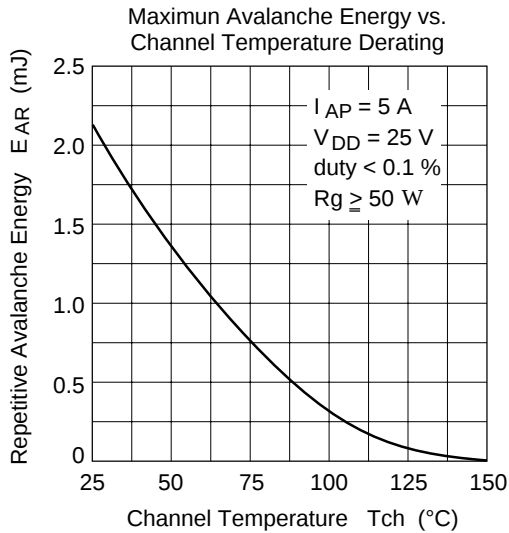
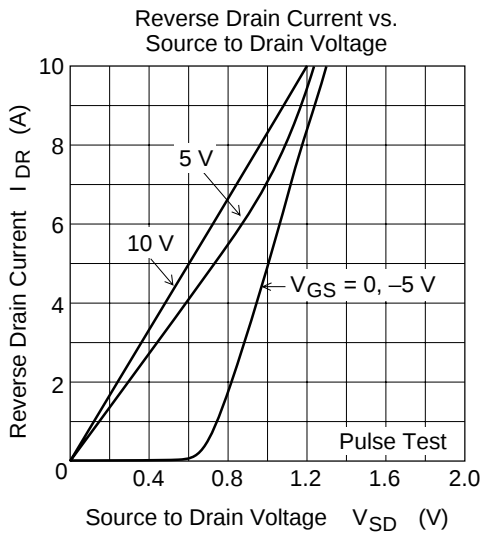
Note: 4. Pulse test

Main Characteristics

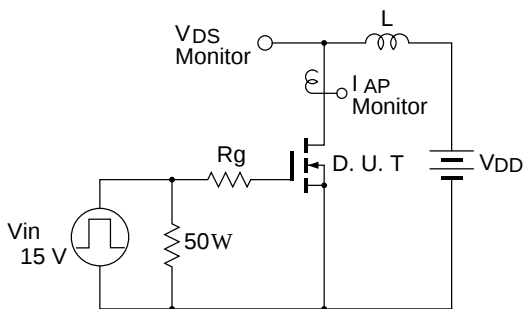






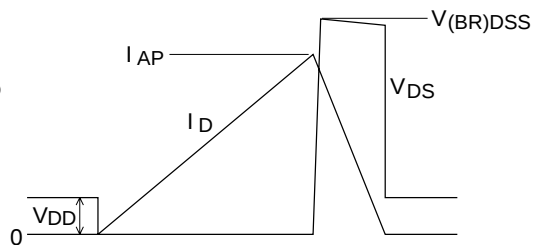


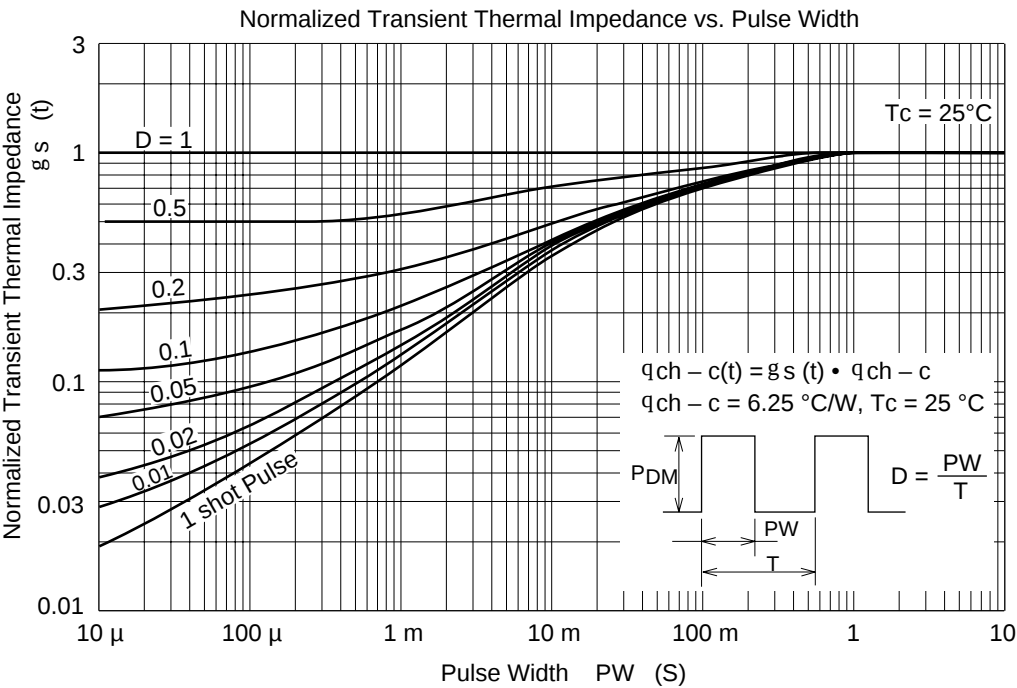
Avalanche Test Circuit



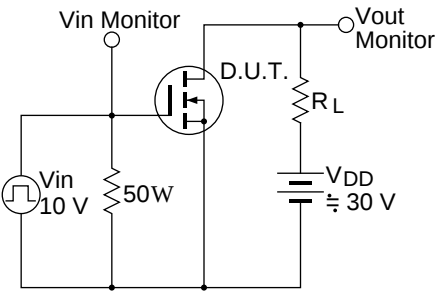
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

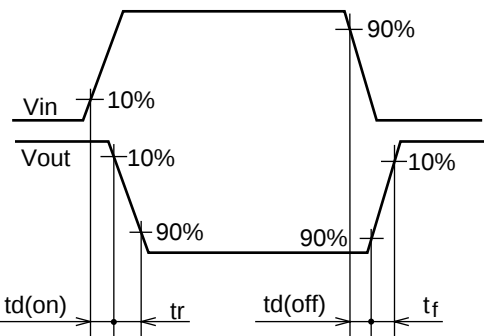




Switching Time Test Circuit

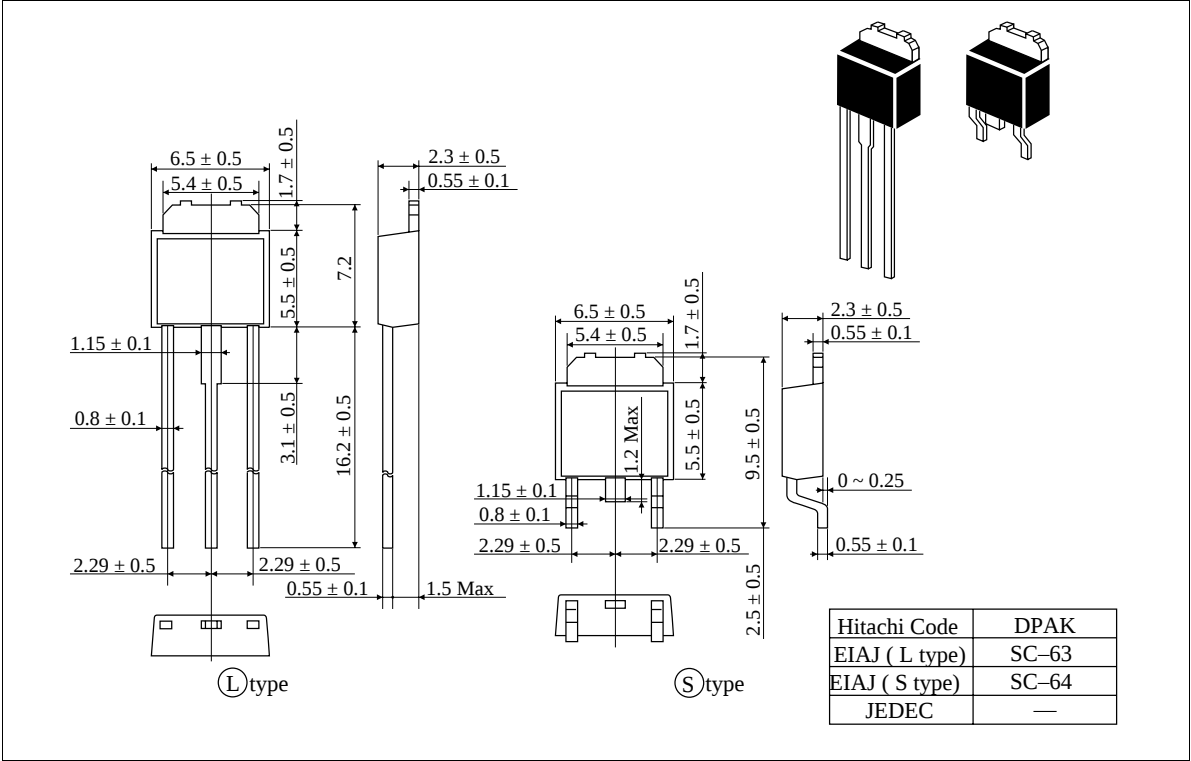


Waveform



Package Dimensions

Unit: mm



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