

# 2SK2926(L), 2SK2926(S)

Silicon N Channel MOS FET  
High Speed Power Switching

# HITACHI

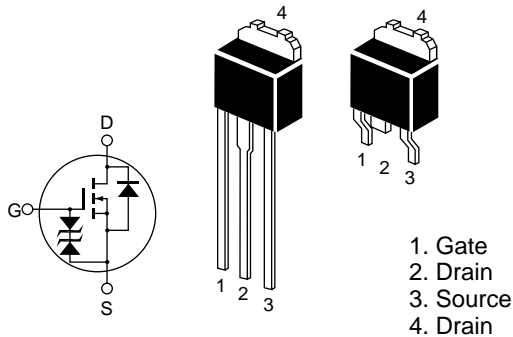
ADE-208-535  
1st. Edition

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.042\Omega$  typ.
- 4V gate drive devices.
- High speed switching

## Outline

DPAK-2



## 2SK2926(L), 2SK2926(S)

### Absolute Maximum Ratings (Ta = 25°C)

| Item                                      | Symbol              | Ratings     | Unit |
|---|---------------------|-------------|------|
| Drain to source voltage                   | $V_{DSS}$           | 60          | V    |
| Gate to source voltage                    | $V_{GSS}$           | ±20         | V    |
| Drain current                             | $I_D$               | 15          | A    |
| Drain peak current                        | $I_{D(pulse)}^{*1}$ | 60          | A    |
| Body to drain diode reverse drain current | $I_{DR}$            | 15          | A    |
| Avalanche current                         | $I_{AP}^{*3}$       | 15          | A    |
| Avalanche energy                          | $E_{AR}^{*3}$       | 19          | mJ   |
| Channel dissipation                       | $Pch^{*2}$          | 25          | W    |
| Channel temperature                       | Tch                 | 150         | °C   |
| Storage temperature                       | Tstg                | -55 to +150 | °C   |

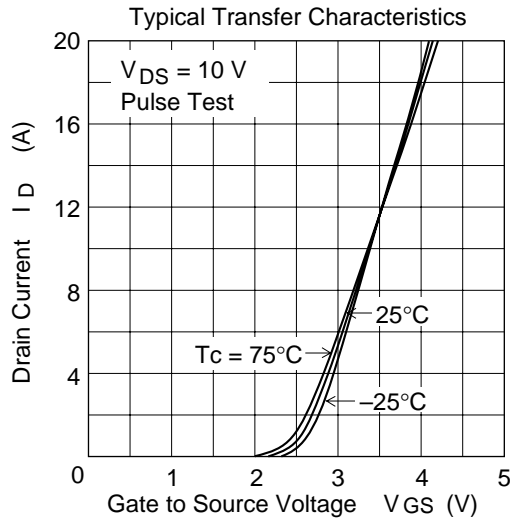
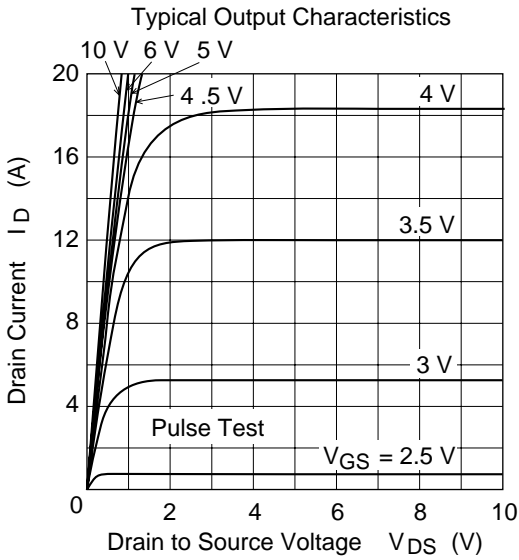
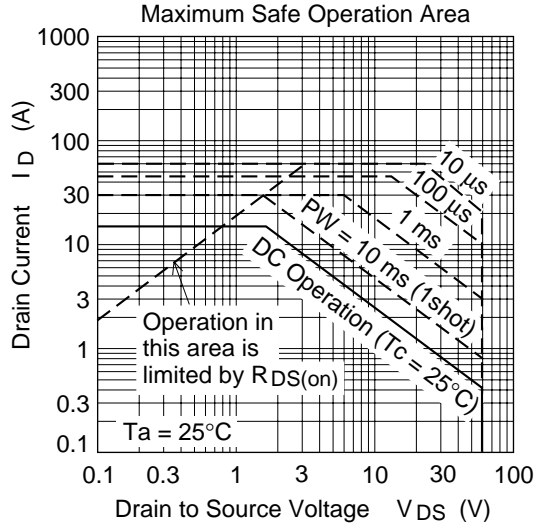
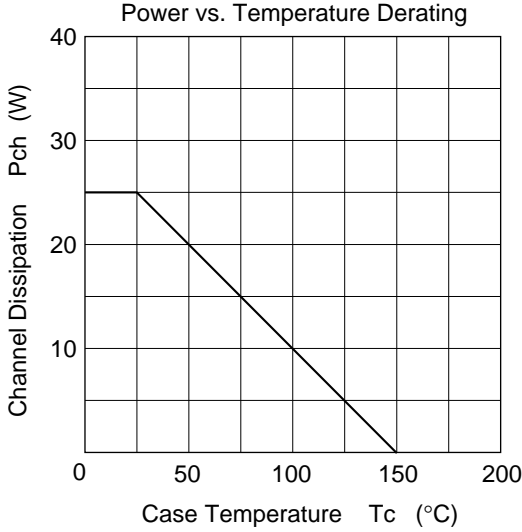
- Notes: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
2. Value at Ta = 25°C  
3. Value at Ta = 25°C, Rg  $\geq 50\ \Omega$

**Electrical Characteristics (Ta = 25°C)**

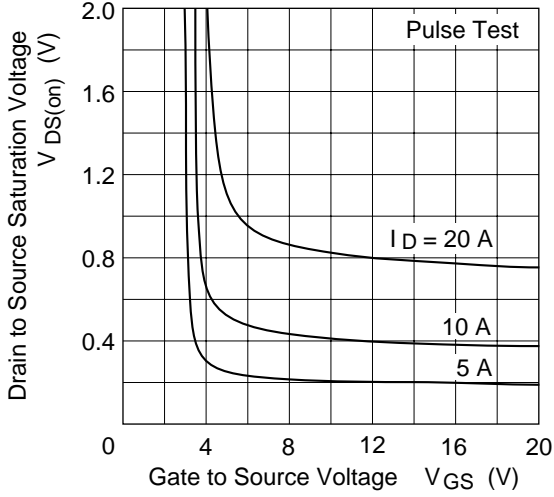
| Item                                       | Symbol        | Min | Typ   | Max   | Unit | Test Conditions  |
|--|---------------|-----|-------|-------|------|--|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 60  | —     | —     | V    | $I_D = 10\text{mA}, V_{GS} = 0$                                      |
| Gate to source breakdown voltage           | $V_{(BR)GSS}$ | ±20 | —     | —     | V    | $I_G = \pm 100\mu\text{A}, V_{DS} = 0$                               |
| Zero gate voltage drain current            | $I_{DSS}$     | —   | —     | 10    | μA   | $V_{DS} = 60\text{V}, V_{GS} = 0$                                    |
| Gate to source leak current                | $I_{GSS}$     | —   | —     | ±10   | μA   | $V_{GS} = \pm 16\text{V}, V_{DS} = 0$                                |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 1.5 | —     | 2.5   | V    | $I_D = 1\text{mA}, V_{DS} = 10\text{V}$                              |
| Static drain to source on state resistance | $R_{DS(on)}$  | —   | 0.042 | 0.055 | Ω    | $I_D = 8\text{A}, V_{GS} = 10\text{V}^{*1}$                          |
|  | $R_{DS(on)}$  | —   | 0.065 | 0.11  | Ω    | $I_D = 8\text{A}, V_{GS} = 4\text{V}^{*1}$                           |
| Forward transfer admittance                | $ y_{fs} $    | 7   | 11    | —     | S    | $I_D = 8\text{A}, V_{DS} = 10\text{V}^{*1}$                          |
| Input capacitance                          | $C_{iss}$     | —   | 500   | —     | pF   | $V_{DS} = 10\text{V}$  |
| Output capacitance                         | $C_{oss}$     | —   | 260   | —     | pF   | $V_{GS} = 0$   |
| Reverse transfer capacitance               | $C_{rss}$     | —   | 110   | —     | pF   | $f = 1\text{MHz}$  |
| Turn-on delay time                         | $t_{d(on)}$   | —   | 10    | —     | ns   | $V_{GS} = 10\text{V}, I_D = 8\text{A}$                               |
| Rise time                                  | $t_r$         | —   | 80    | —     | ns   | $R_L = 3.75\Omega$   |
| Turn-off delay time                        | $t_{d(off)}$  | —   | 100   | —     | ns   |  |
| Fall time                                  | $t_f$         | —   | 110   | —     | ns   |  |
| Body to drain diode forward voltage        | $V_{DF}$      | —   | 1.0   | —     | V    | $I_F = 15\text{A}, V_{GS} = 0$                                       |
| Body to drain diode reverse recovery time  | $t_{rr}$      | —   | 55    | —     | ns   | $I_F = 15\text{A}, V_{GS} = 0$<br>$di_F/dt = 50\text{A}/\mu\text{s}$ |

Note: 1. Pulse test

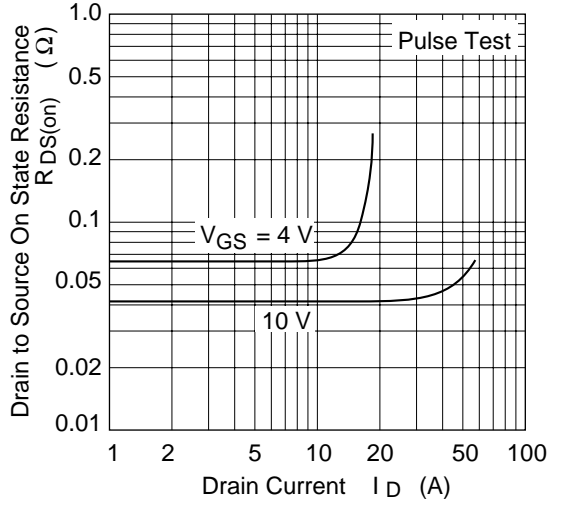
## Main Characteristics



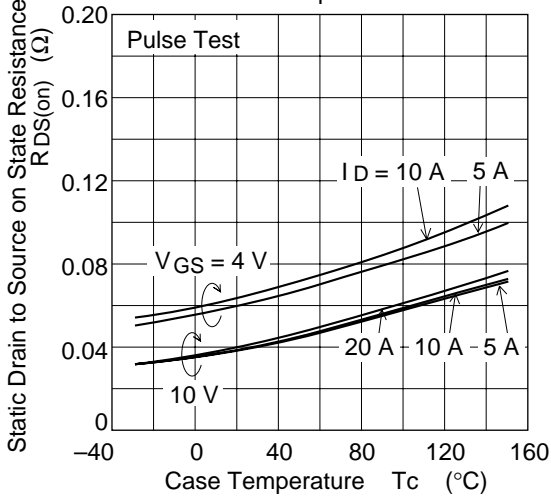
Drain to Source Saturation Voltage vs. Gate to Source Voltage



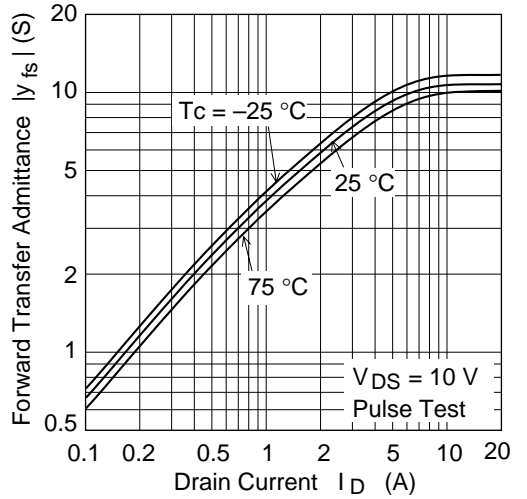
Static Drain to Source on State Resistance vs. Drain Current



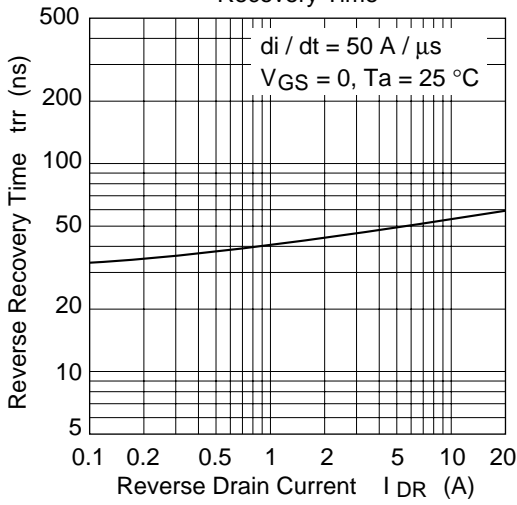
Static Drain to Source on State Resistance vs. Temperature



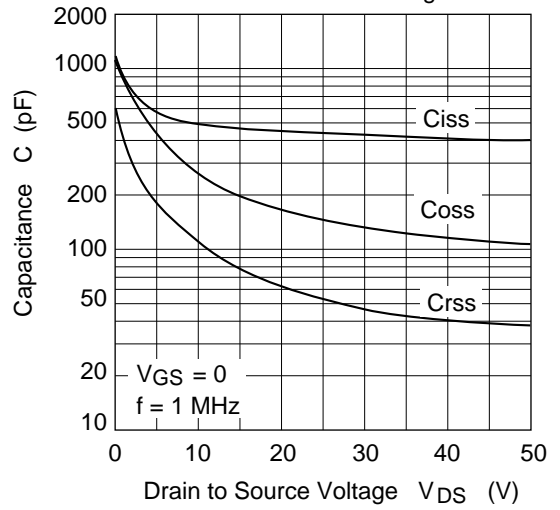
Forward Transfer Admittance vs. Drain Current



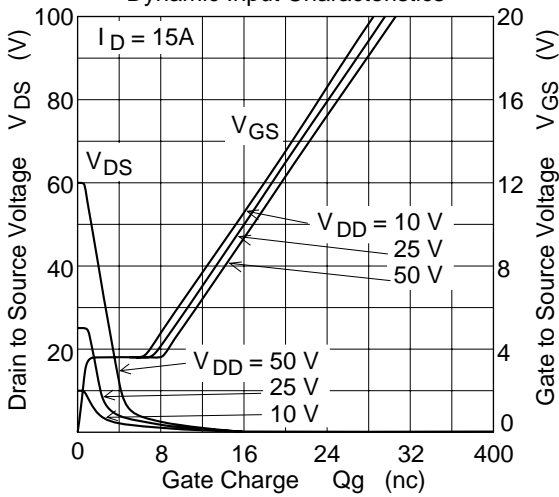
**Body to Drain Diode Reverse Recovery Time**



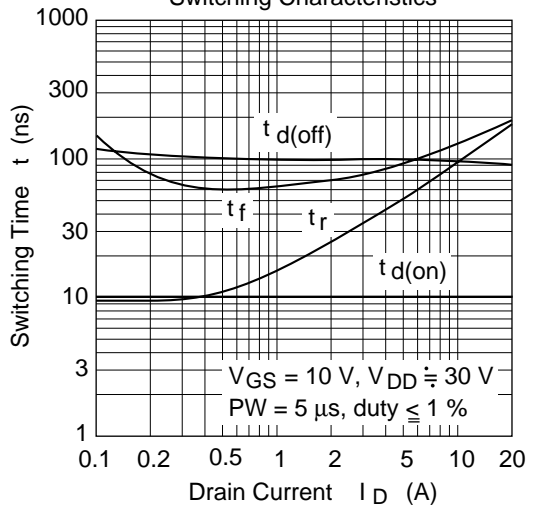
**Typical Capacitance vs. Drain to Source Voltage**

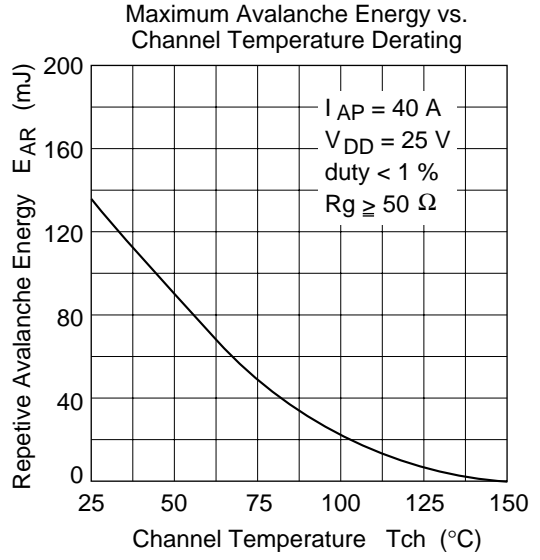
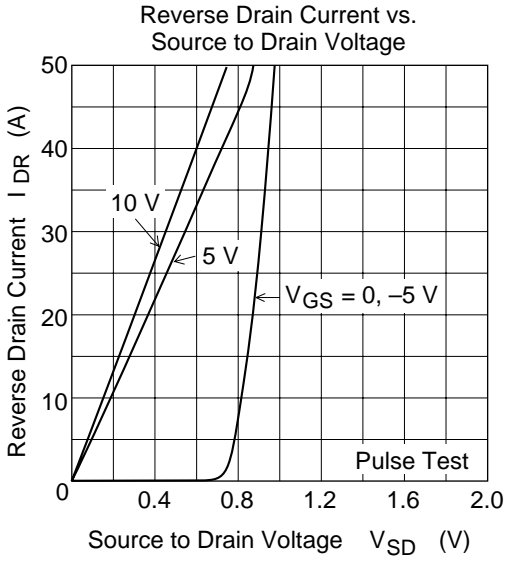


**Dynamic Input Characteristics**

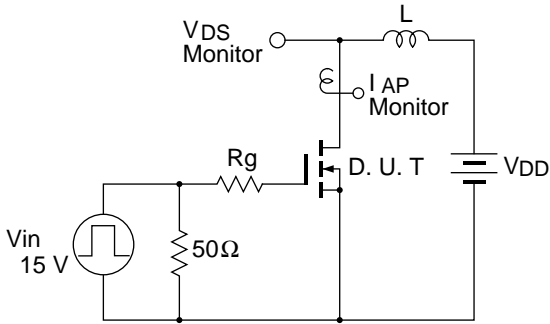


**Switching Characteristics**



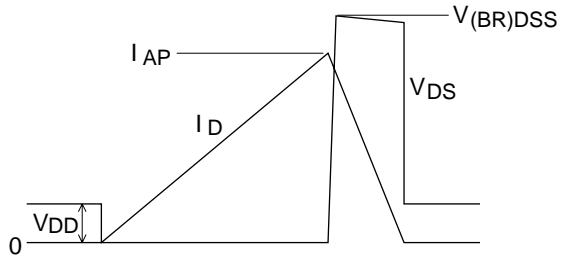


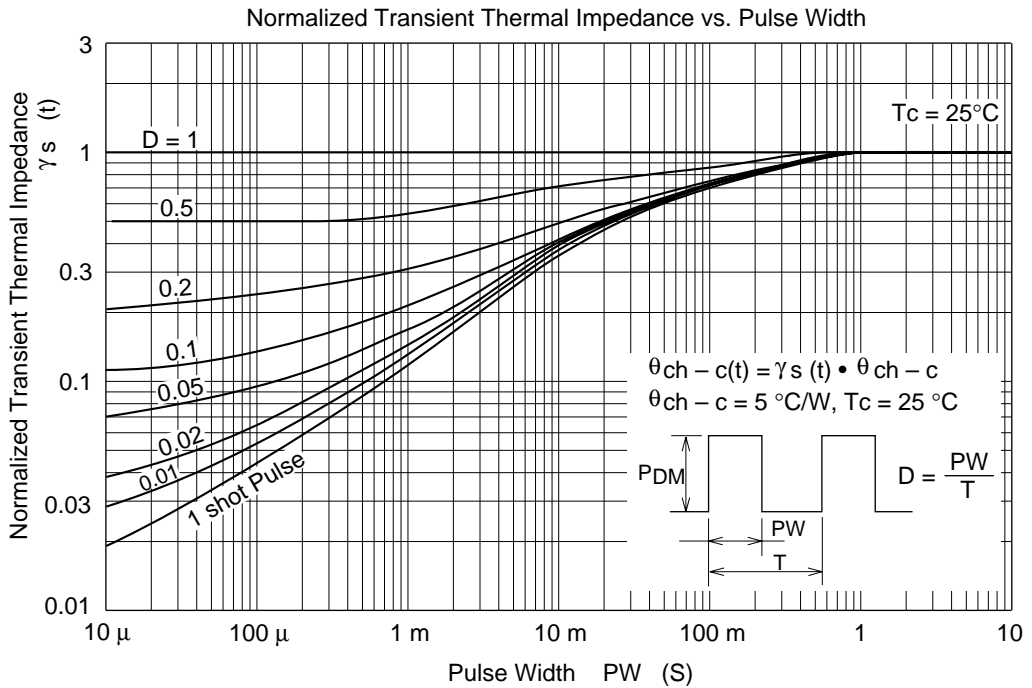
Avalanche Test Circuit



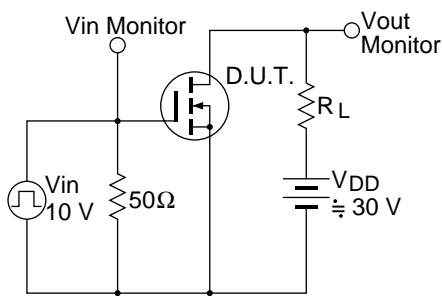
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

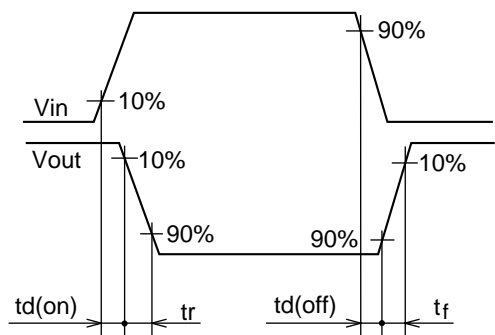




Switching Time Test Circuit



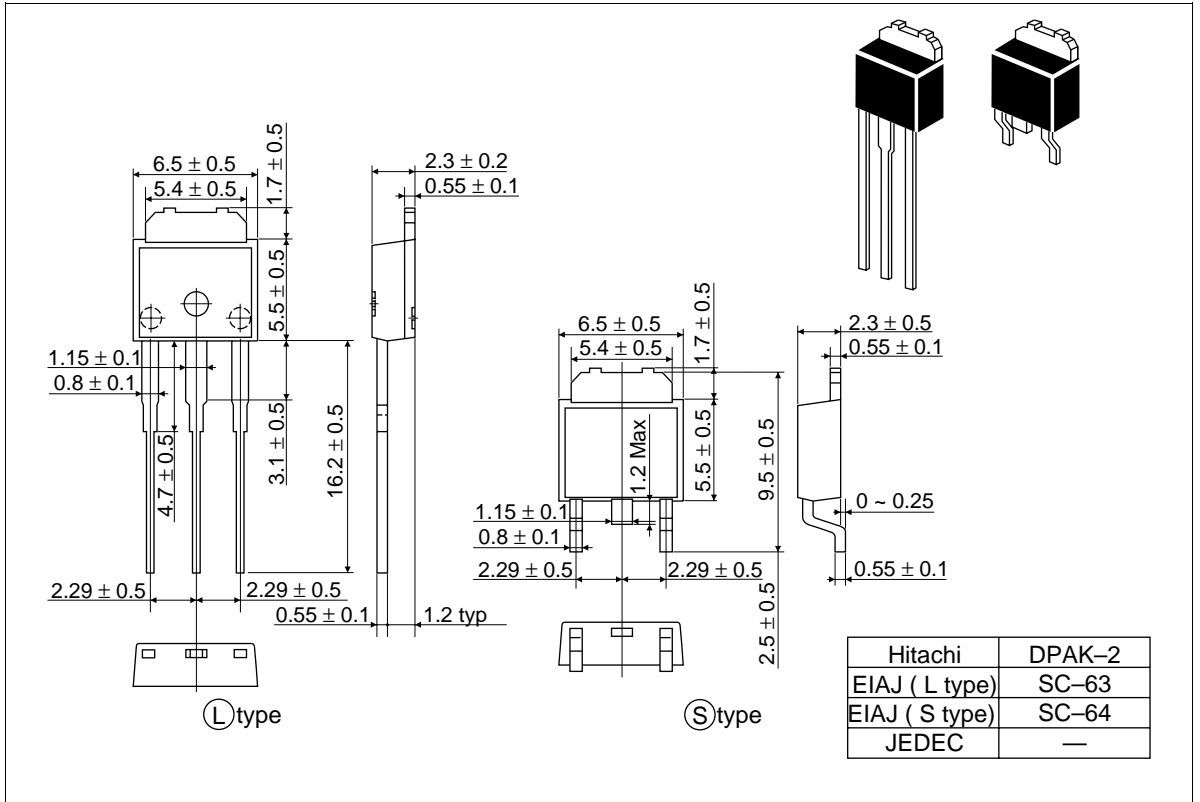
Switching Time Waveform





Package Dimensions

Unit: mm



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