

2SK3070(L),2SK3070(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

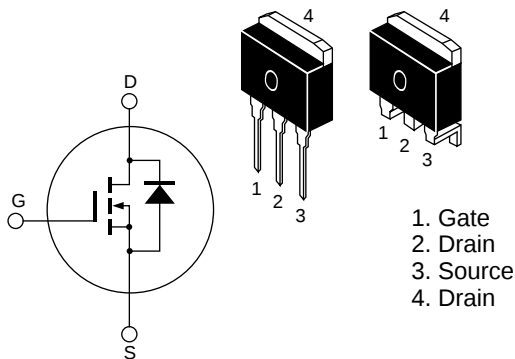
ADE-208-684G (Z)
8th. Edition
February 1999

Features

- Low on-resistance
 $R_{DS(on)} = 4.5 \text{ m}\Omega$ typ.
- Low drive current
- 4 V gate drive device can be driven from 5 V source

Outline

LDPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	40	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	75	A
Drain peak current	I _{D(pulse)} ^{Note1}	300	A
Body-drain diode reverse drain current	I _{DR}	75	A
Avalanche current	I _{AP} ^{Note3}	50	A
Avalanche energy	E _{AR} ^{Note3}	333	mJ
Channel dissipation	P _{ch} ^{Note2}	100	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

Note:

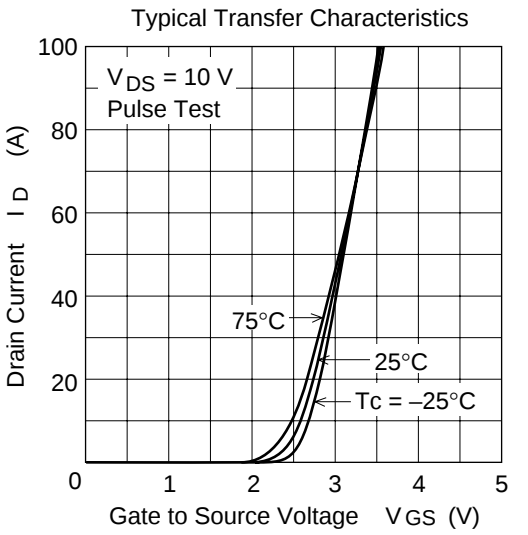
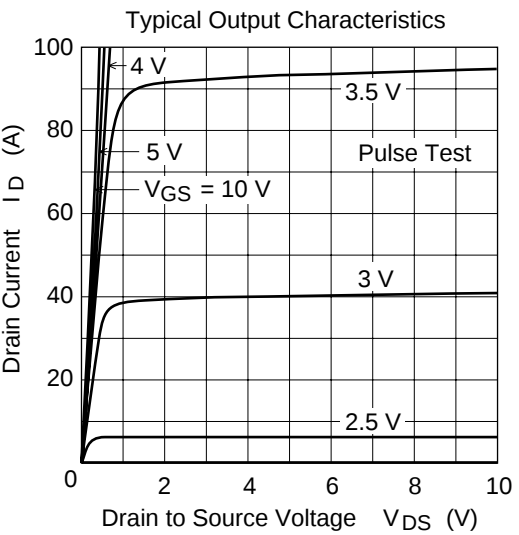
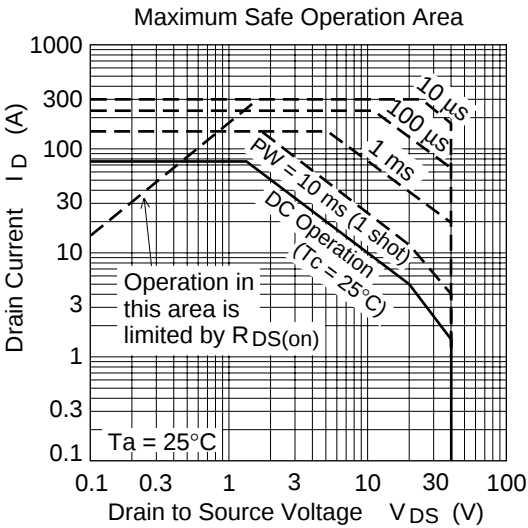
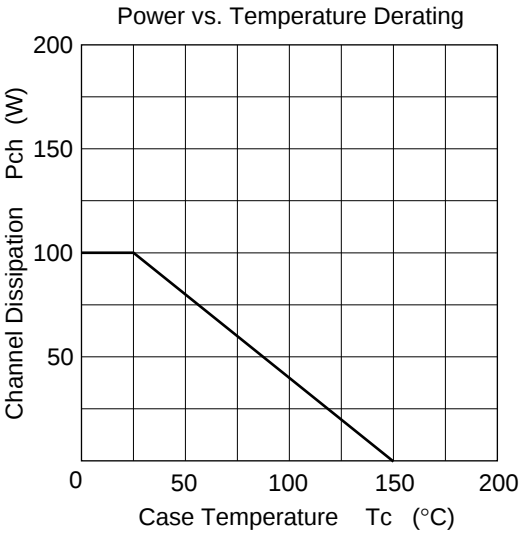
- 1. PW ≤ 10 μs, duty cycle ≤ 1%
- 2. Value at Tc = 25°C
- 3. Value at Tch = 25°C, Rg ≥ 50 Ω

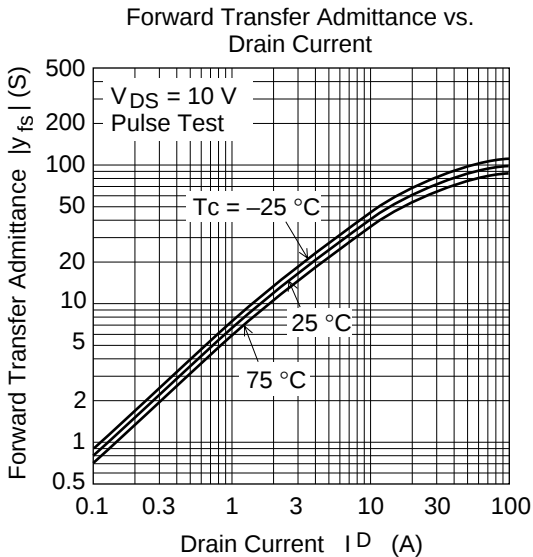
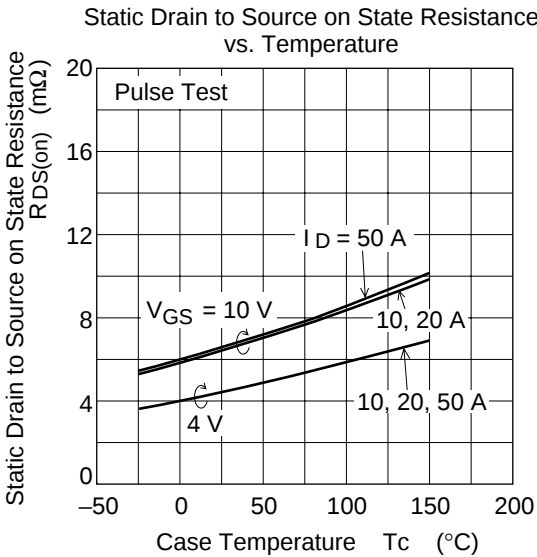
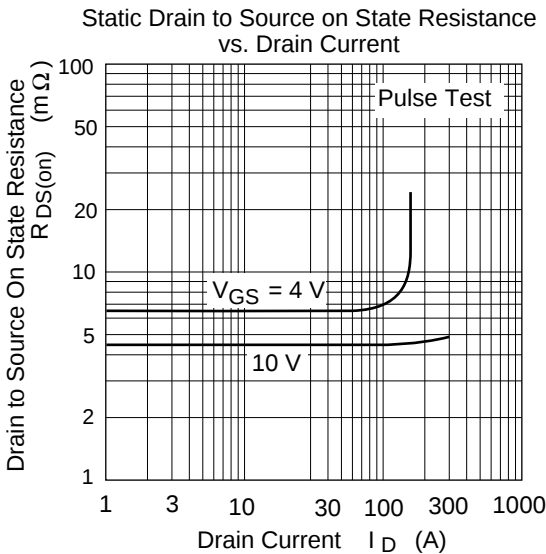
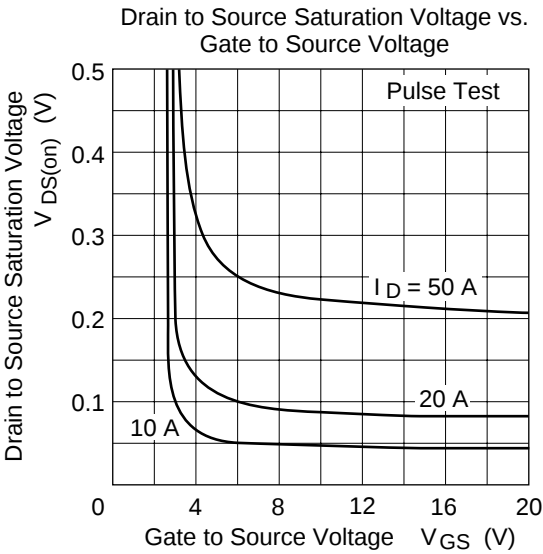
Electrical Characteristics (Ta = 25°C)

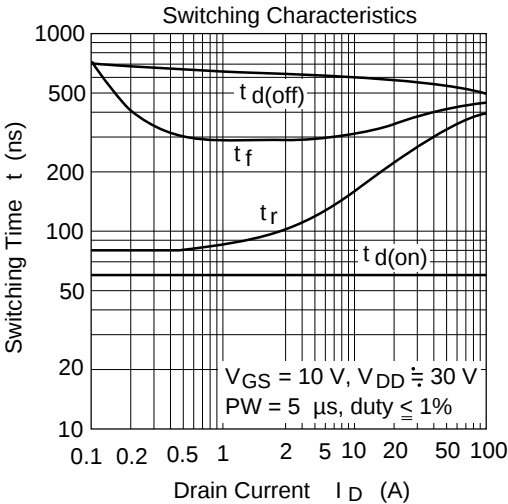
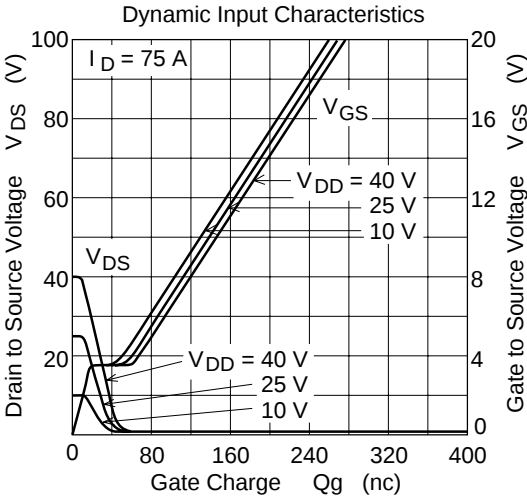
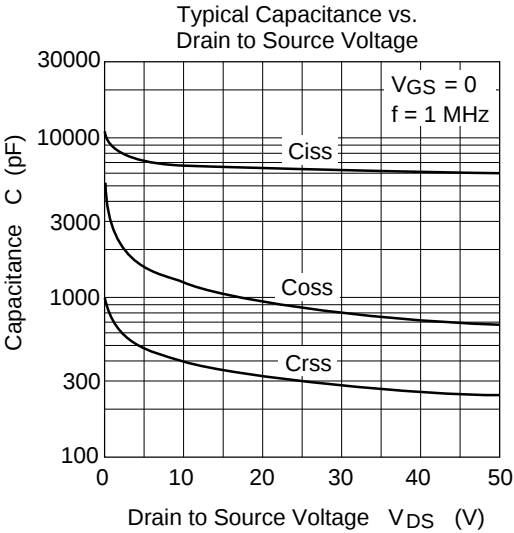
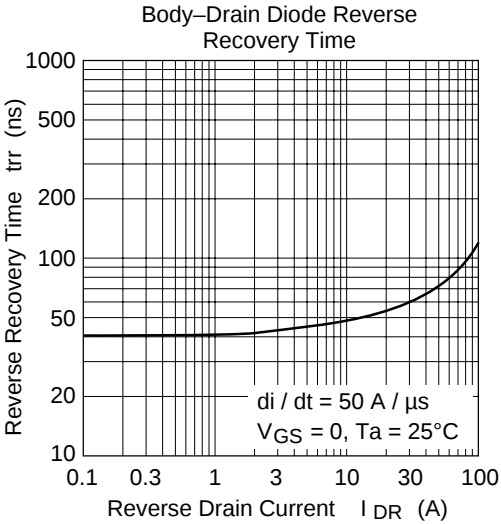
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10\text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 40\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1\text{ mA}$, $V_{DS} = 10\text{ V}$ ^{Note1}
Static drain to source on state	$R_{DS(on)}$	—	4.5	5.8	$\text{m}\Omega$	$I_D = 40\text{ A}$, $V_{GS} = 10\text{ V}$ ^{Note1}
resistance		—	6.5	10	$\text{m}\Omega$	$I_D = 40\text{ A}$, $V_{GS} = 4\text{ V}$ ^{Note1}
Forward transfer admittance	$ y_{fs} $	50	80	—	S	$I_D = 40\text{ A}$, $V_{DS} = 10\text{ V}$ ^{Note1}
Input capacitance	C_{iss}	—	6800	—	pF	$V_{DS} = 10\text{ V}$
Output capacitance	C_{oss}	—	1300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	380	—	pF	$f = 1\text{ MHz}$
Total gate charge	Q_g	—	130	—	nc	$V_{DD} = 25\text{ V}$
Gate to source charge	Q_{gs}	—	25	—	nc	$V_{GS} = 10\text{ V}$
Gate to drain charge	Q_{gd}	—	30	—	nc	$I_D = 75\text{ A}$
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$
Rise time	t_r	—	300	—	ns	$R_L = 0.75\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	550	—	ns	
Fall time	t_f	—	400	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	$I_F = 75\text{ A}$, $V_{GS} = 0$
Body–drain diode reverse recovery time	t_{rr}	—	90	—	ns	$I_F = 75\text{ A}$, $V_{GS} = 0$ $diF/dt = 50\text{ A}/\mu\text{s}$

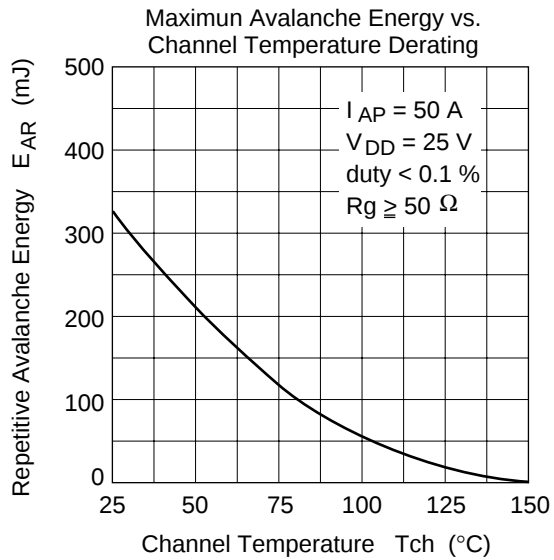
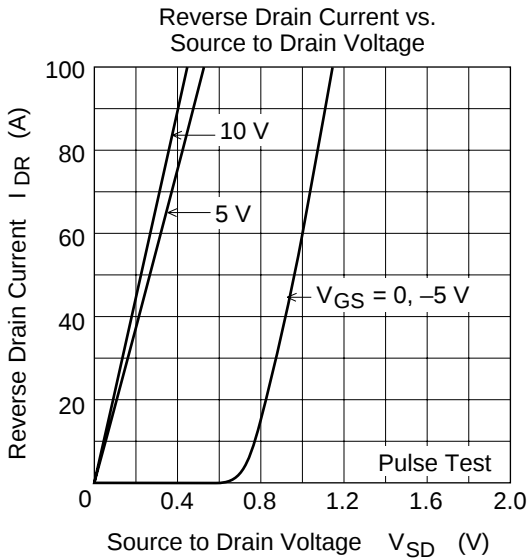
Note: 1. Pulse test

Main Characteristics

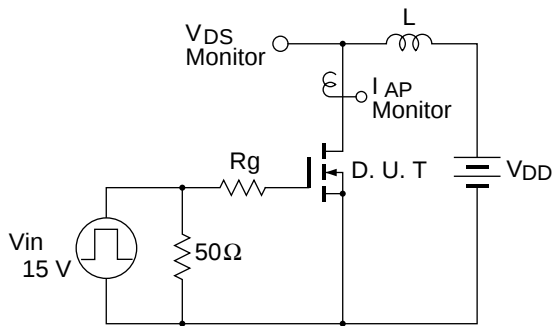






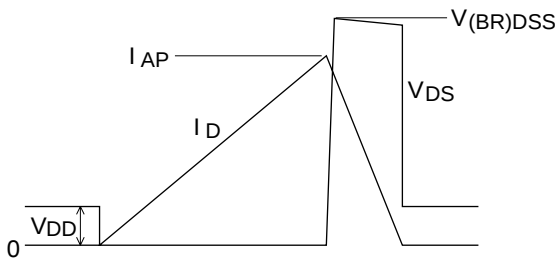


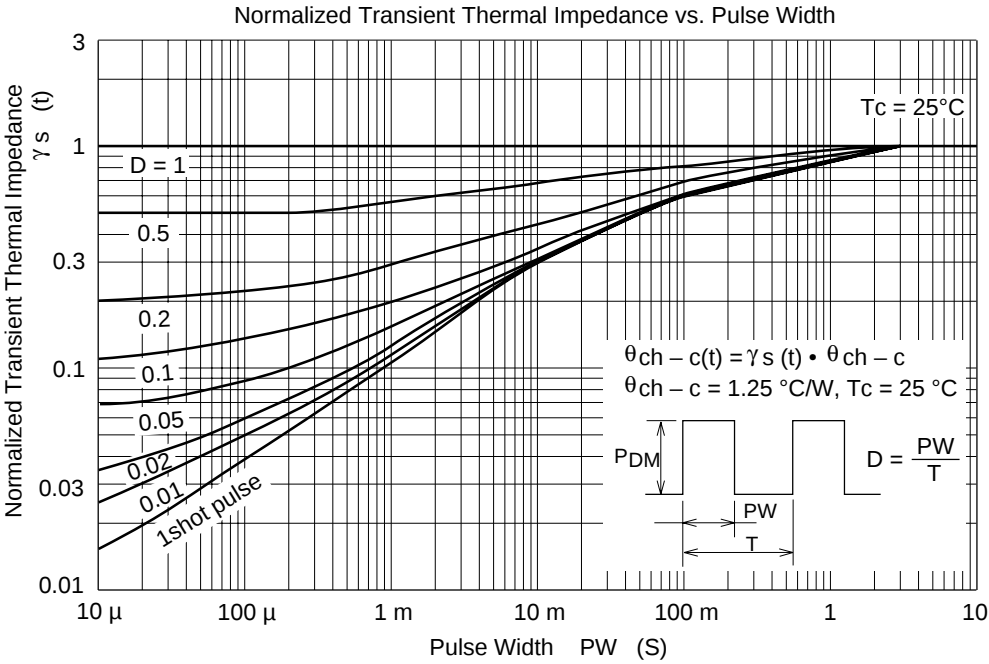
Avalanche Test Circuit



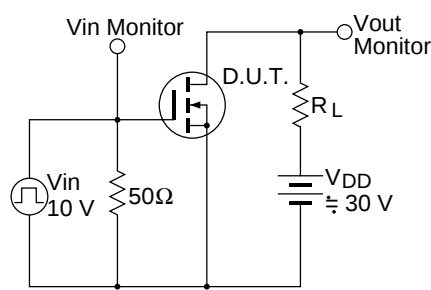
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

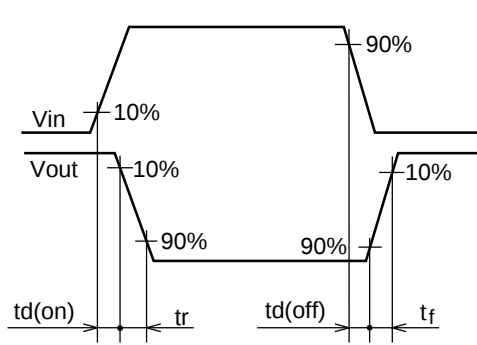




Switching Time Test Circuit

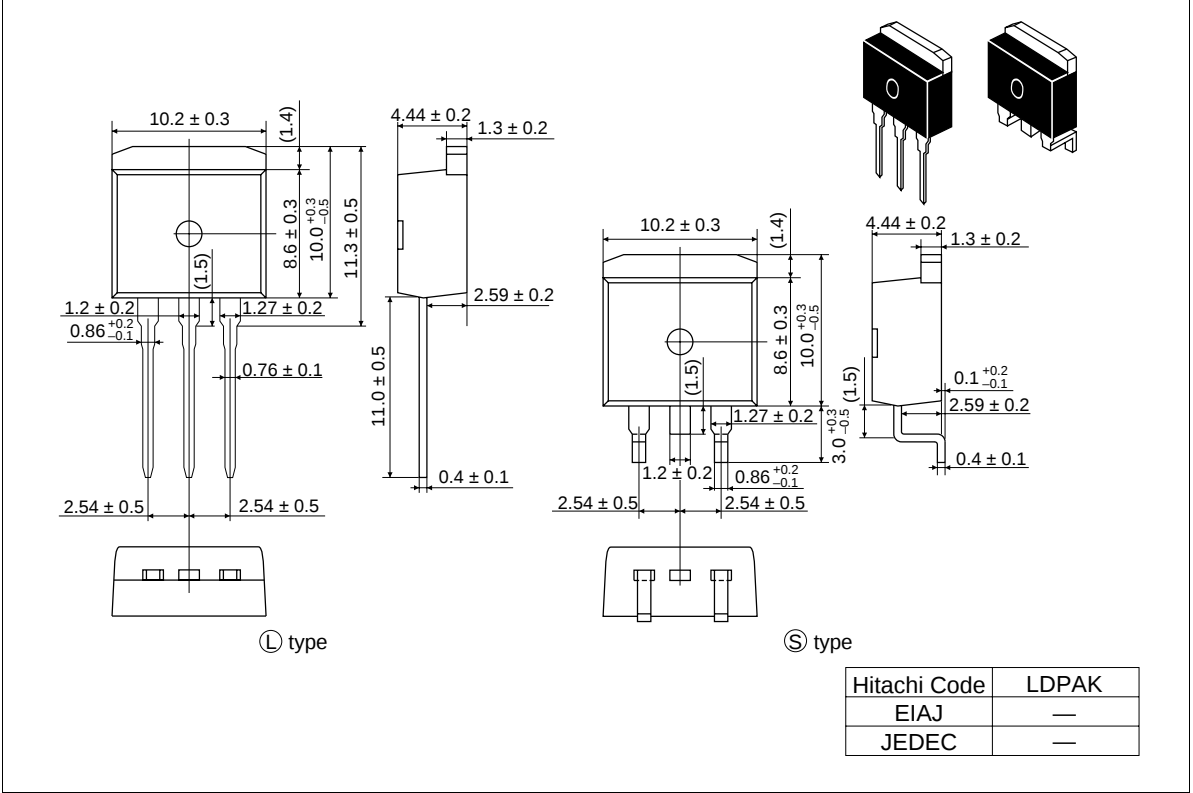


Waveform



Package Dimensions

Unit: mm



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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
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Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533 Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building, No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180
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Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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