

# 2SK3348

Silicon N Channel MOS FET  
High Speed Switching

# HITACHI

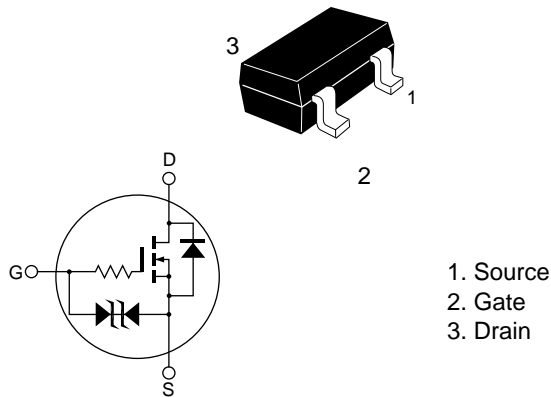
ADE-208-772 A (Z)  
2nd.Edition.  
June 1999

## Features

- Low on-resistance  
 $R_{DS} = 1.6 \Omega$  typ. ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 50 \text{ mA}$ )  
 $R_{DS} = 2.2 \Omega$  typ. ( $V_{GS} = 2.5 \text{ V}$ ,  $I_D = 50 \text{ mA}$ )
- 2.5 V gate drive device.
- Small package (CMPAK)

## Outline

CMPAK



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	20	V
Gate to source voltage	$V_{GSS}$	±10	V
Drain current	$I_D$	100	mA
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	400	mA
Body-drain diode reverse drain current	$I_{DR}$	100	mA
Channel dissipation	Pch <sup>Note 2</sup>	300	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. Value on the alumina ceramic board (12.5x20x0.7mm)

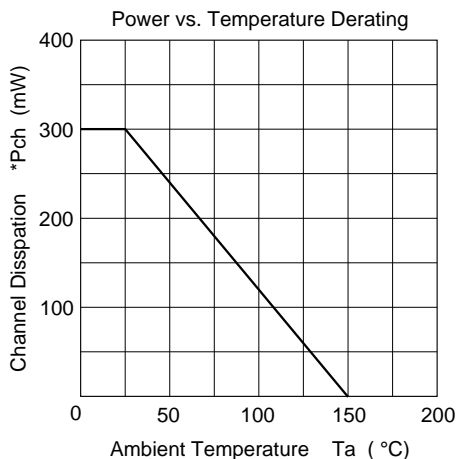
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5	μA	$V_{GS} = \pm 8 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	μA	$V_{DS} = 20 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.8	—	1.8	V	$I_D = 10 \mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.6	1.9	Ω	$I_D = 50 mA, V_{GS} = 4 V$ <sup>Note 3</sup>
	$R_{DS(on)}$	—	2.2	3.2	Ω	$I_D = 50 mA, V_{GS} = 2.5 V$ <sup>Note 3</sup>
Forward transfer admittance	$ y_{fs} $	143	220	—	mS	$I_D = 50 mA, V_{DS} = 10 V$ <sup>Note 3</sup>
Input capacitance	Ciss	—	18	—	pF	$V_{DS} = 10 V$
Output capacitance	Coss	—	15	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	5	—	pF	$f = 1 MHz$
Turn-on delay time	$t_{d(on)}$	—	73	—	ns	$I_D = 50 mA, V_{GS} = 4 V$
Rise time	$t_r$	—	290	—	ns	$R_L = 200 \Omega$
Turn-off delay time	$t_{d(off)}$	—	360	—	ns	
Fall time	$t_f$	—	360	—	ns	

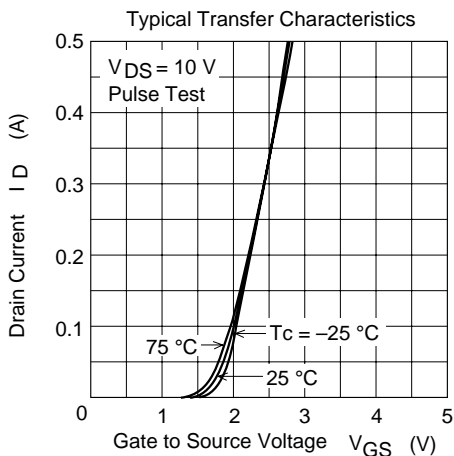
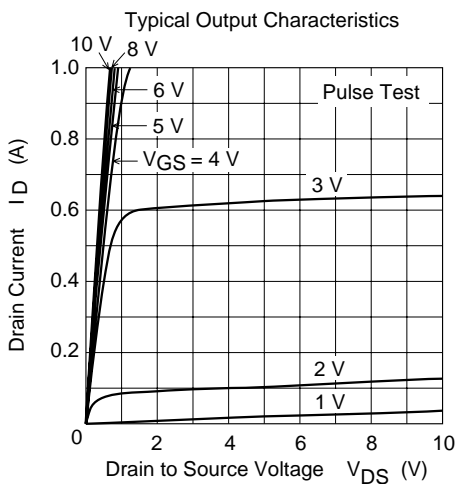
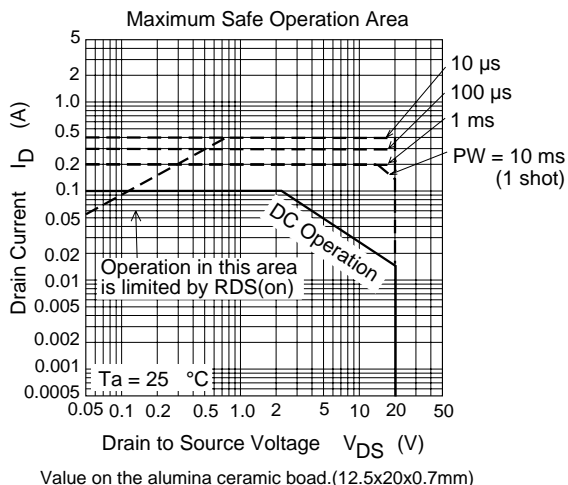
Note: 3. Pulse test

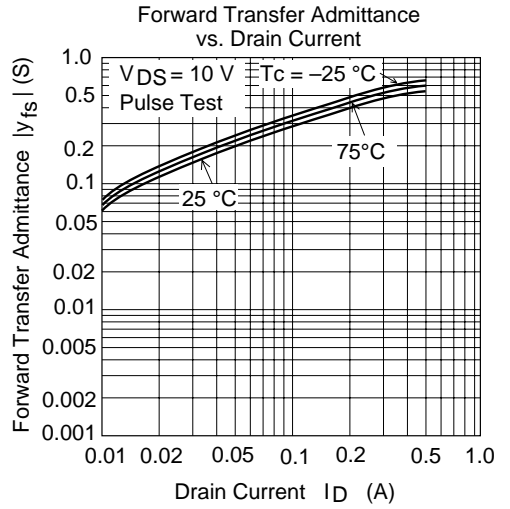
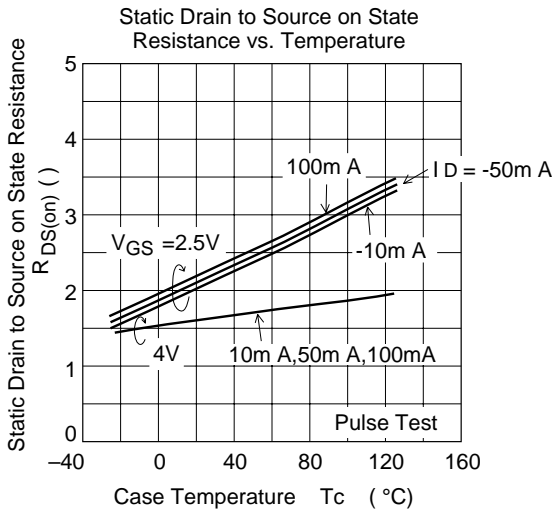
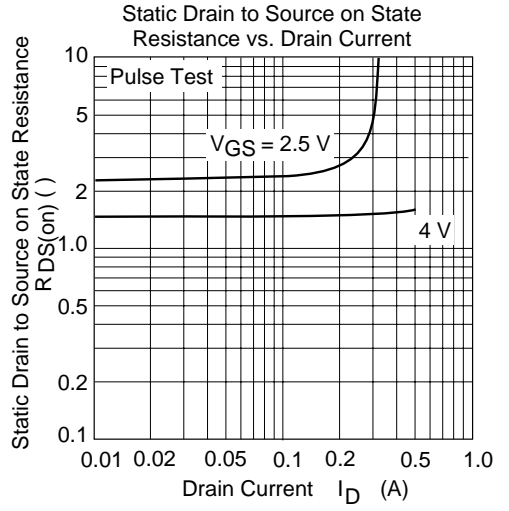
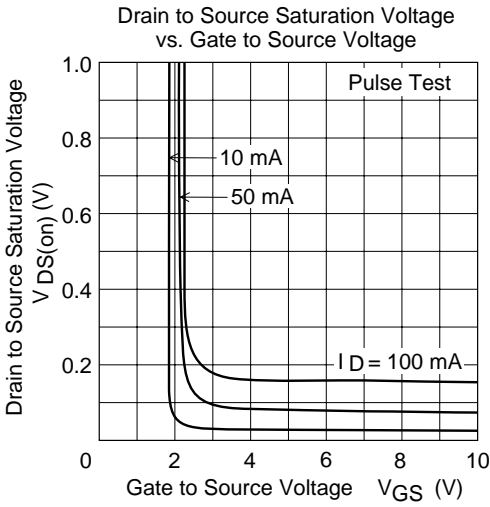
4. Marking is CN

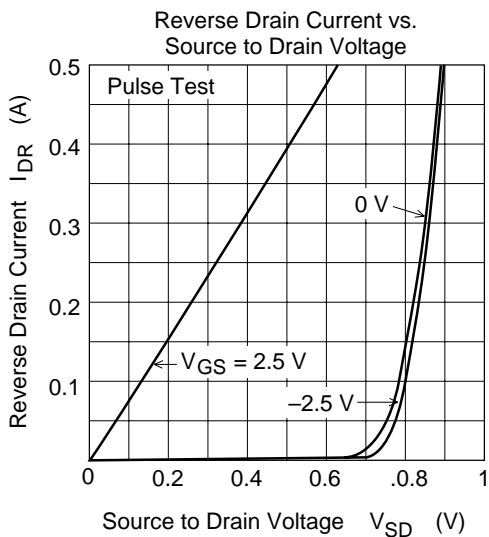
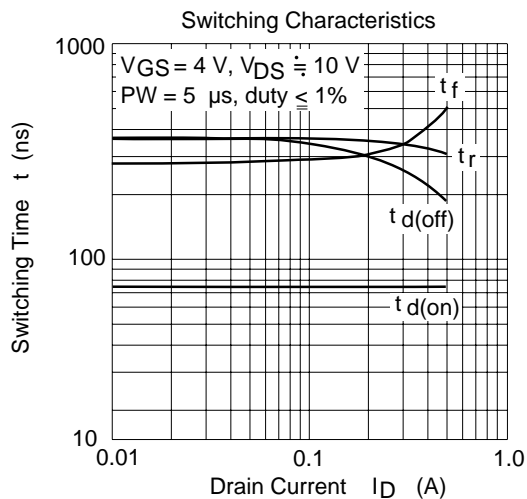
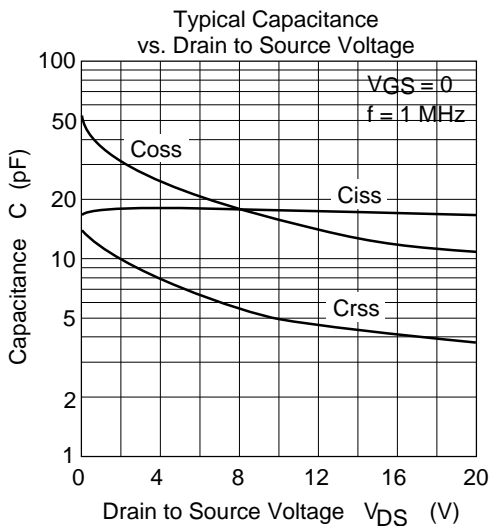
## Main Characteristics



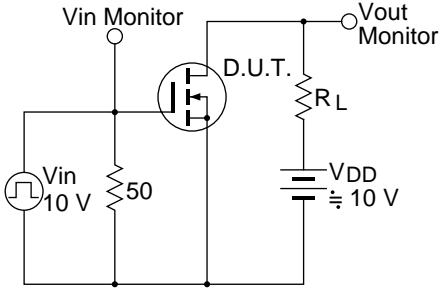
\*Value on the alumina ceramic board.(12.5x20x0.7mm)



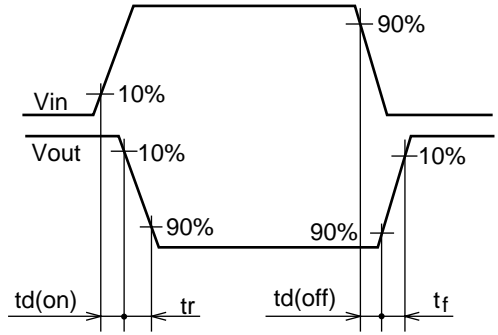




Switching Time Test Circuit

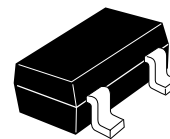
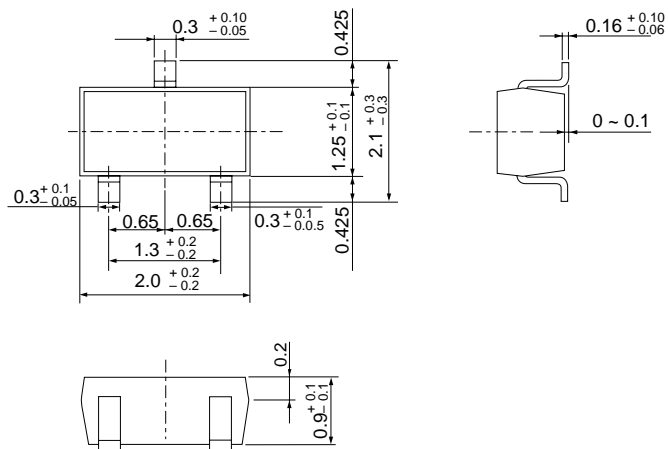


Waveforms



## Package Dimensions

Unit: mm



Hitachi Code	CMPAK
EIAJ	SC-70
JEDEC	-

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