

# HAT1024R

Silicon P Channel Power MOS FET  
High Speed Power Switching

# HITACHI

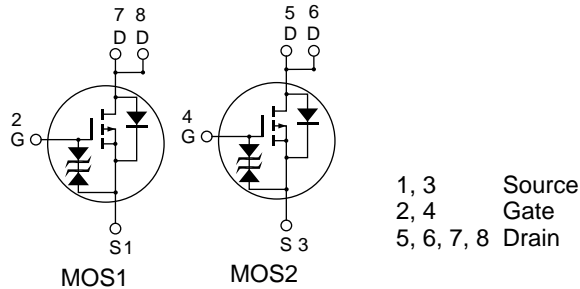
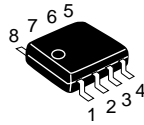
ADE-208-476 G (Z)  
8th. Edition  
June 1997

## Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

## Outline

SOP-8



# HAT1024R

## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-3.5	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-28	A
Body-drain diode reverse drain current	$I_{DR}$	-3.5	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	2	W
Channel dissipation	$P_{ch}$ <sup>Note3</sup>	3	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$

2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

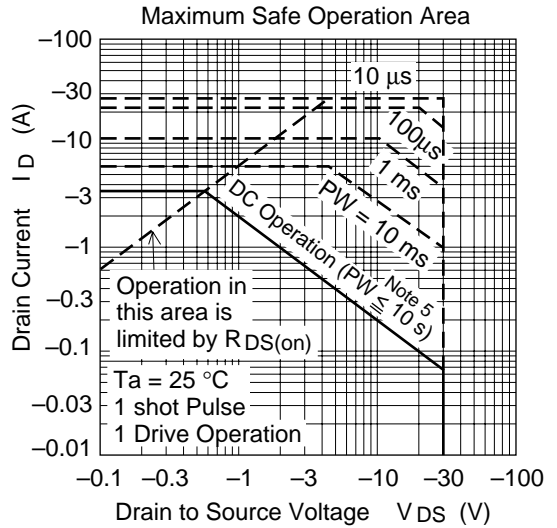
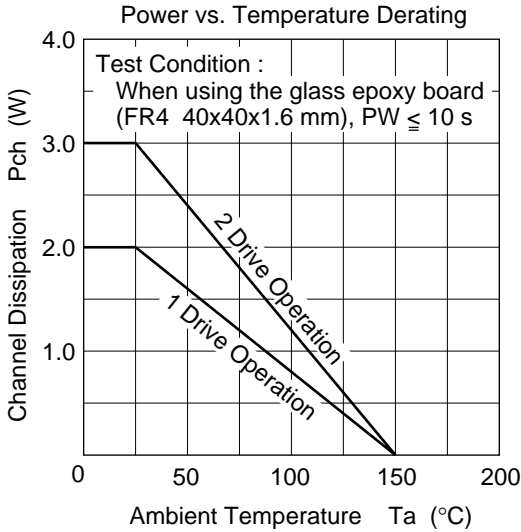
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

**Electrical Characteristics** (Ta = 25°C)

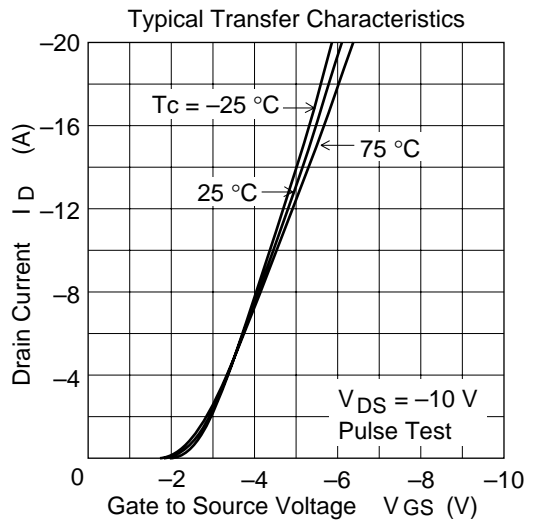
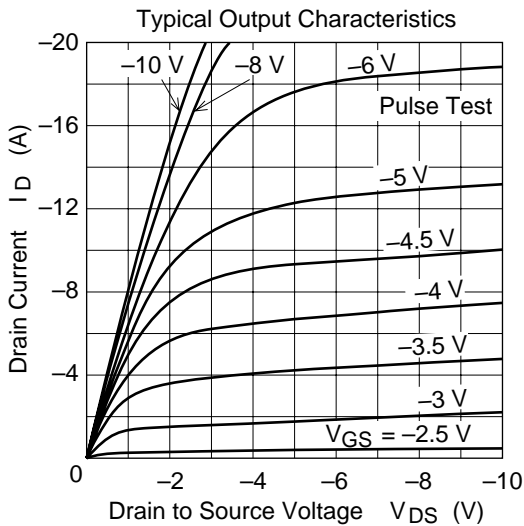
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	μA	$V_{DS} = -30\text{V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10\text{V}$ , $I_D = -1\text{mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	$I_D = -2\text{A}$ , $V_{GS} = -10\text{V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.2	0.34	Ω	$I_D = -2\text{A}$ , $V_{GS} = -4\text{V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	2.5	3.5	—	S	$I_D = -2\text{A}$ , $V_{DS} = -10\text{V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	350	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	$C_{oss}$	—	230	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	75	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	$V_{GS} = -4\text{V}$ , $I_D = -2\text{A}$
Rise time	$t_r$	—	110	—	ns	$V_{DD} \cong -10\text{V}$
Turn-off delay time	$t_{d(off)}$	—	20	—	ns	
Fall time	$t_f$	—	30	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-1.0	-1.5	V	$I_F = -3.5\text{A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = -3.5\text{A}$ , $V_{GS} = 0$ $di_F/dt = 20\text{A}/\mu\text{s}$

Note: 4. Pulse test

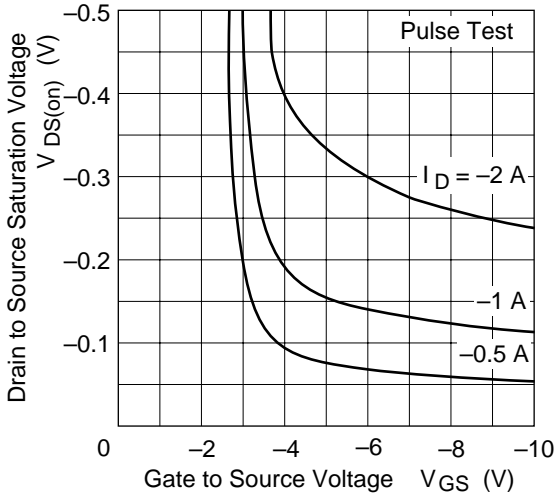
## Main Characteristics



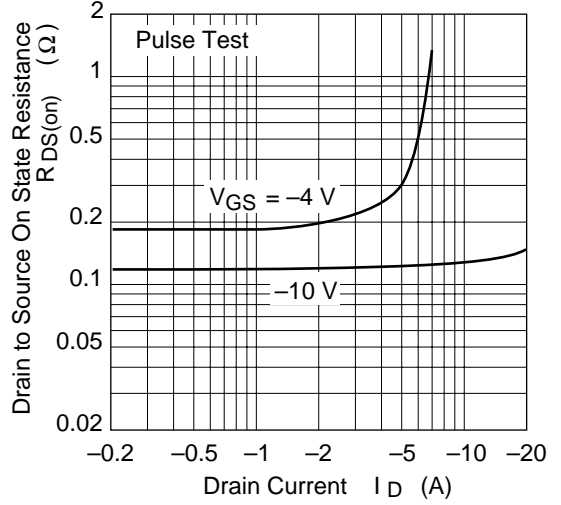
Note 5 :  
When using the glass epoxy board (FR4 40x40x1.6 mm)



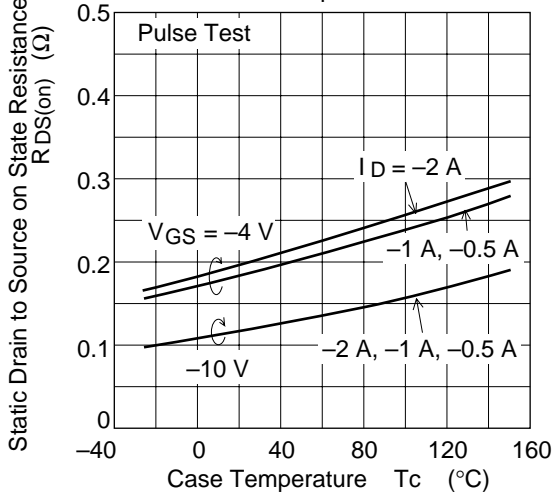
Drain to Source Saturation Voltage vs. Gate to Source Voltage



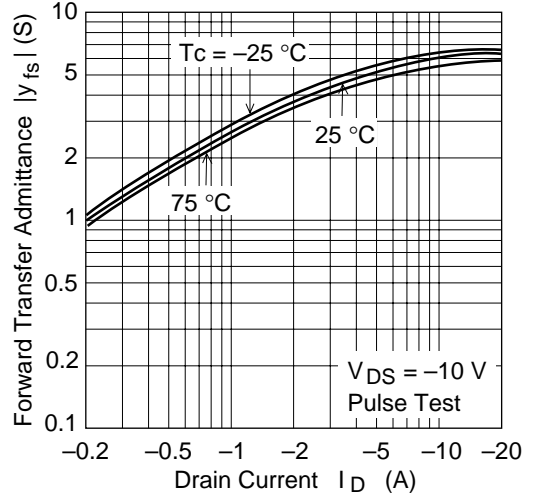
Static Drain to Source on State Resistance vs. Drain Current



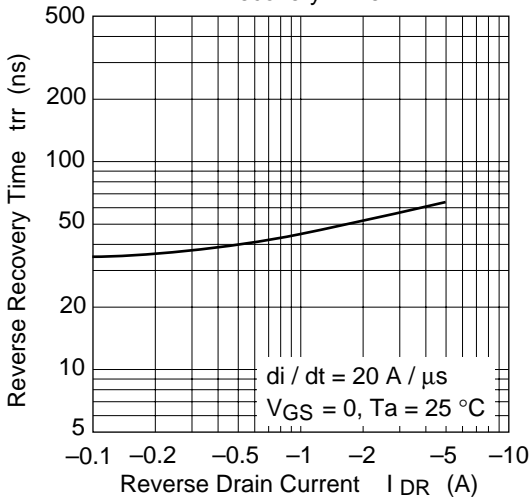
Static Drain to Source on State Resistance vs. Temperature



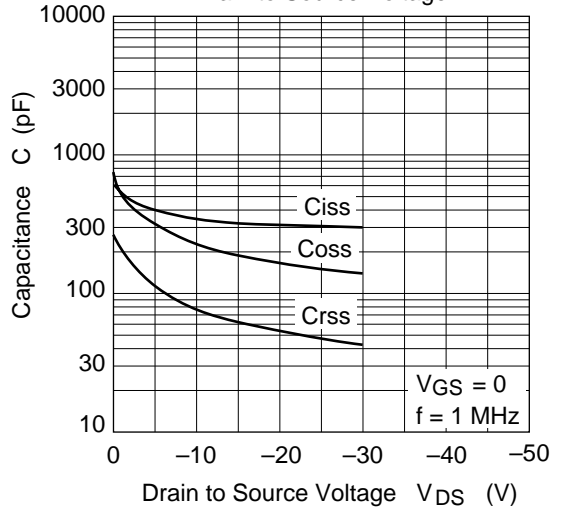
Forward Transfer Admittance vs. Drain Current



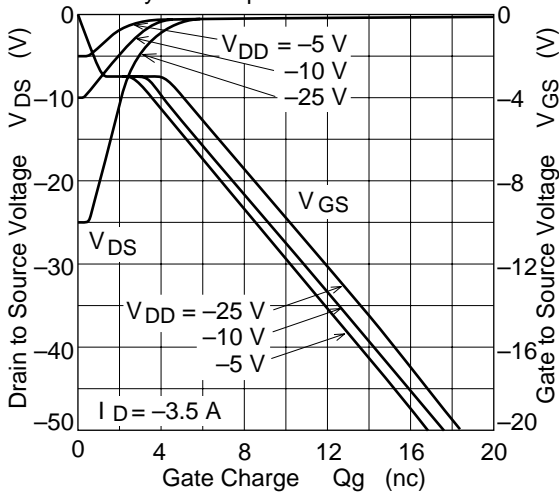
Body-Drain Diode Reverse Recovery Time



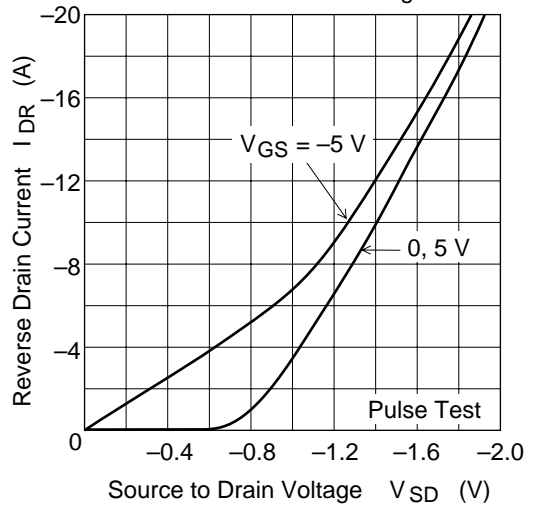
Typical Capacitance vs. Drain to Source Voltage

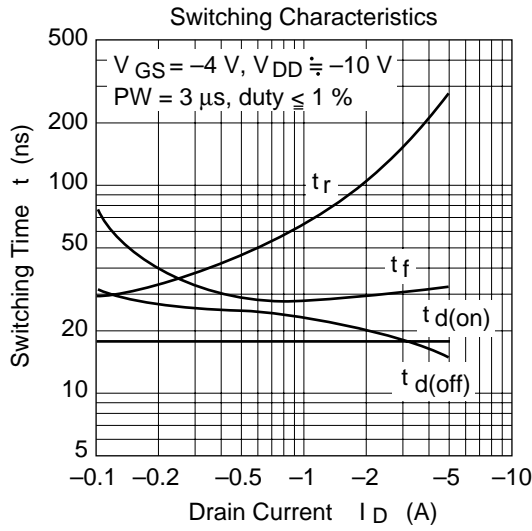


Dynamic Input Characteristics

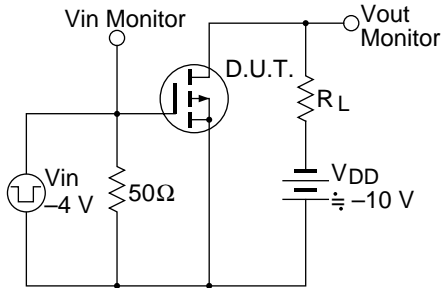


Reverse Drain Current vs. Source to Drain Voltage

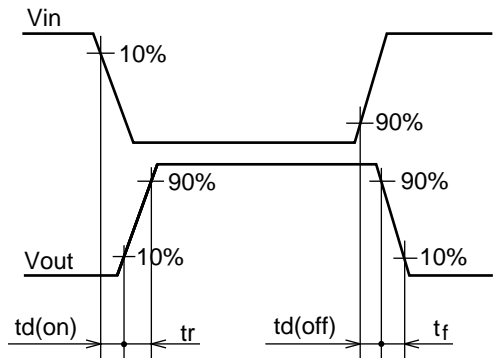


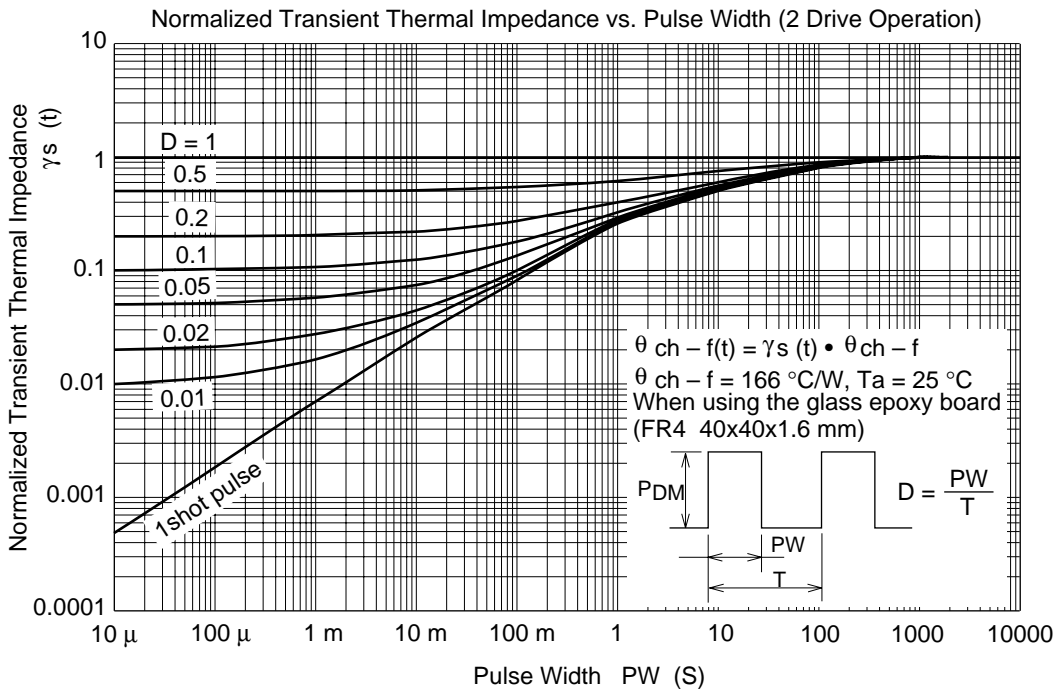
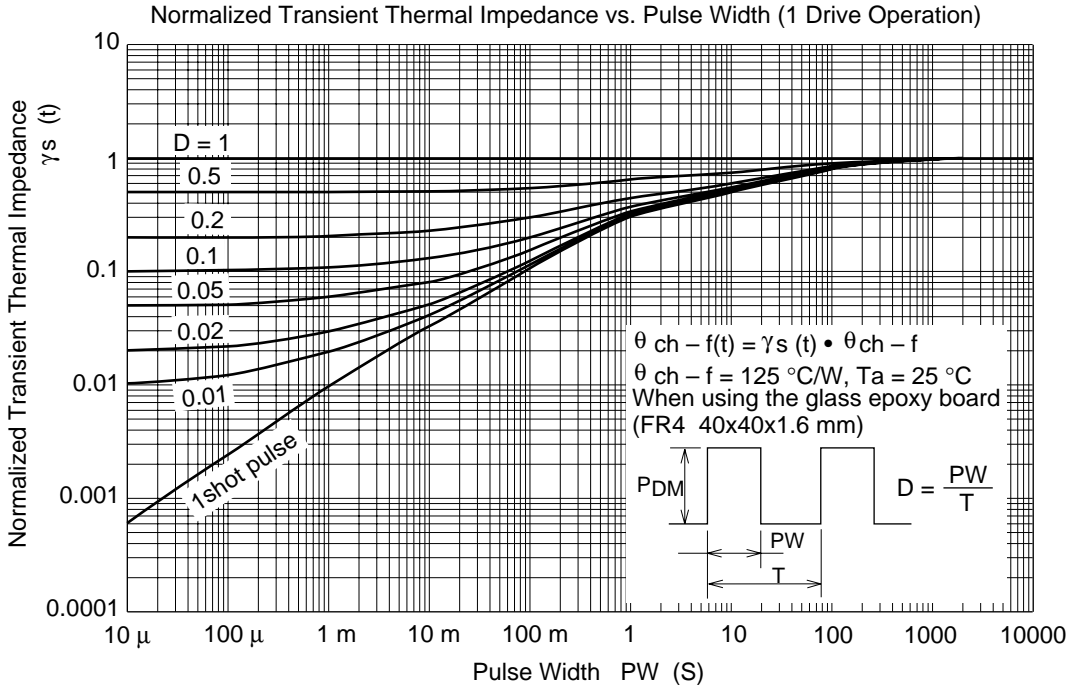


Switching Time Test Circuit



Switching Time Waveform

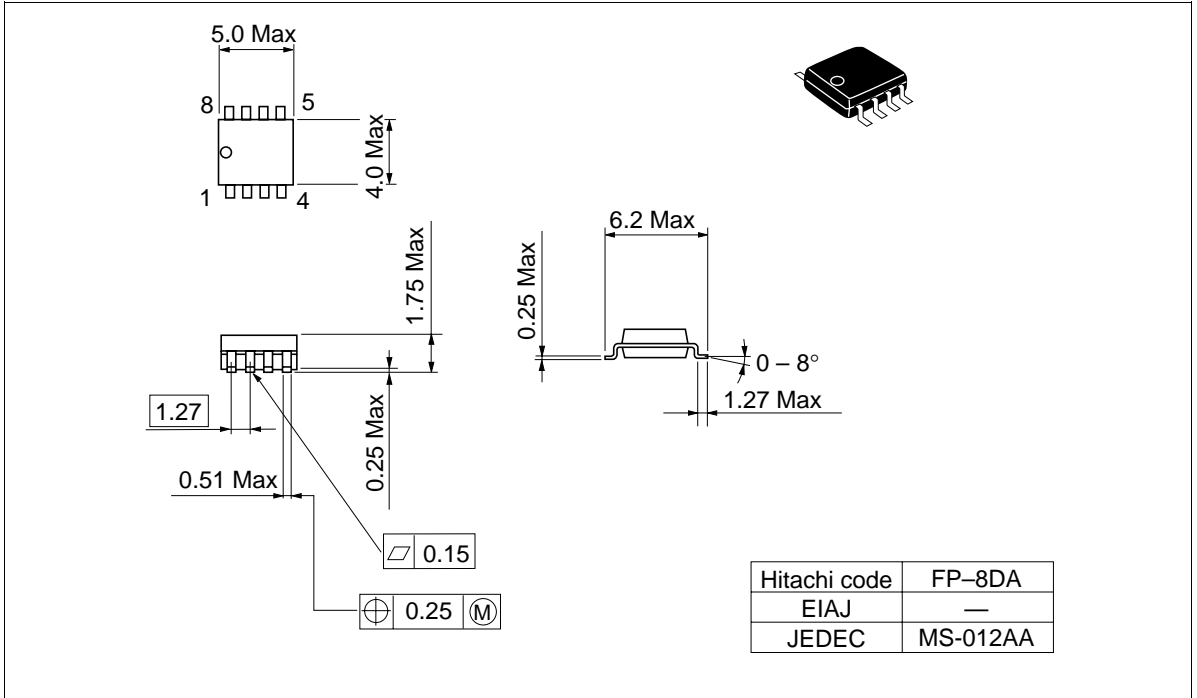






Package Dimentions

Unit: mm



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