

HAT1025R

Silicon P Channel Power MOS FET
High Speed Power Switching

HITACHI

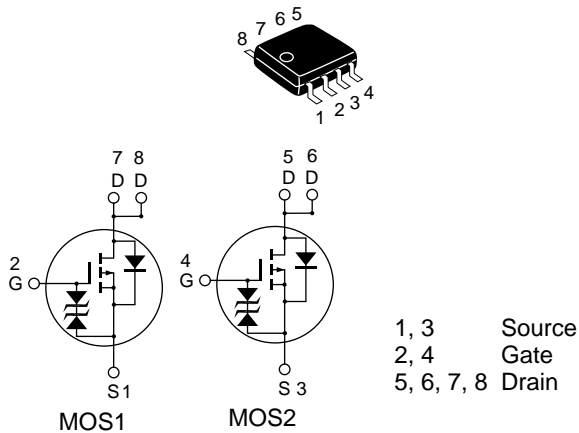
ADE-208-437 H (Z)
9th. Edition
February 1999

Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|--|---------------------------------|---------------|------|
| Drain to source voltage | V_{DSS} | - 20 | V |
| Gate to source voltage | V_{GSS} | ± 10 | V |
| Drain current | I_D | - 4.5 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note1} | - 36 | A |
| Body-drain diode reverse drain current | I_{DR} | - 4.5 | A |
| Channel dissipation | Pch ^{Note2} | 2 | W |
| Channel dissipation | Pch ^{Note3} | 3 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | - 55 to + 150 | °C |

Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

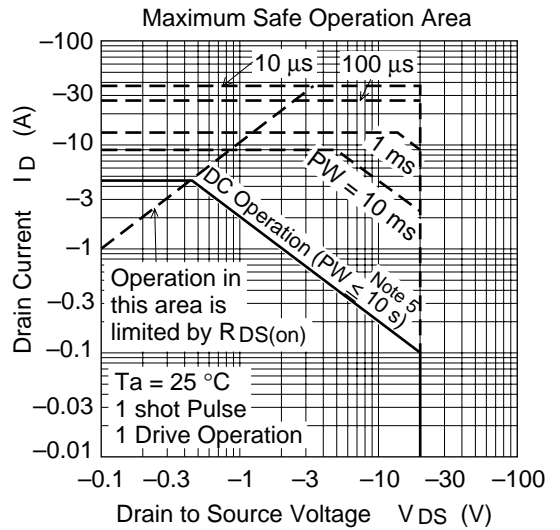
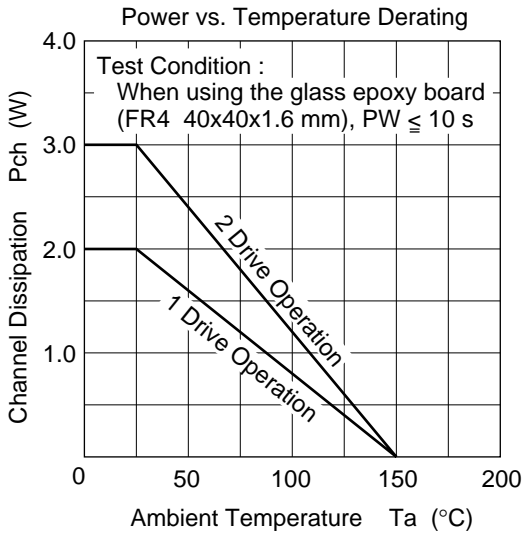
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics (Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|---------------|----------|-------|----------|----------|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | - 20 | — | — | V | $I_D = - 10\text{ mA}$, $V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ± 10 | — | — | V | $I_G = \pm 100\mu A$, $V_{DS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 10 | μA | $V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | - 10 | μA | $V_{DS} = - 20\text{ V}$, $V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | - 0.5 | — | - 1.5 | V | $V_{DS} = - 10\text{ V}$, $I_D = - 1\text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.065 | 0.095 | Ω | $I_D = - 3\text{ A}$, $V_{GS} = - 4\text{ V}$ ^{Note4} |
| | $R_{DS(on)}$ | — | 0.09 | 0.15 | Ω | $I_D = - 3\text{ A}$, $V_{GS} = - 2.5\text{ V}$ ^{Note4} |
| Forward transfer admittance | $ y_{fs} $ | 4.5 | 7 | — | S | $I_D = - 3\text{ A}$, $V_{DS} = - 10\text{ V}$ ^{Note4} |
| Input capacitance | Ciss | — | 860 | — | pF | $V_{DS} = - 10\text{ V}$ |
| Output capacitance | Coss | — | 450 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | Crss | — | 150 | — | pF | $f = 1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 20 | — | ns | $V_{GS} = - 4\text{ V}$, $I_D = - 3\text{ A}$ |
| Rise time | t_r | — | 120 | — | ns | $V_{DD} \cong - 10\text{ V}$ |
| Turn-off delay time | $t_{d(off)}$ | — | 120 | — | ns | |
| Fall time | t_f | — | 100 | — | ns | |
| Body-drain diode forward voltage | V_{DF} | — | - 0.9 | - 1.4 | V | $I_F = - 4.5\text{ A}$, $V_{GS} = 0$ ^{Note4} |
| Body-drain diode reverse recovery time | t_{rr} | — | 60 | — | ns | $I_F = - 4.5\text{ A}$, $V_{GS} = 0$ $diF/dt = 20\text{ A}/\mu s$ |

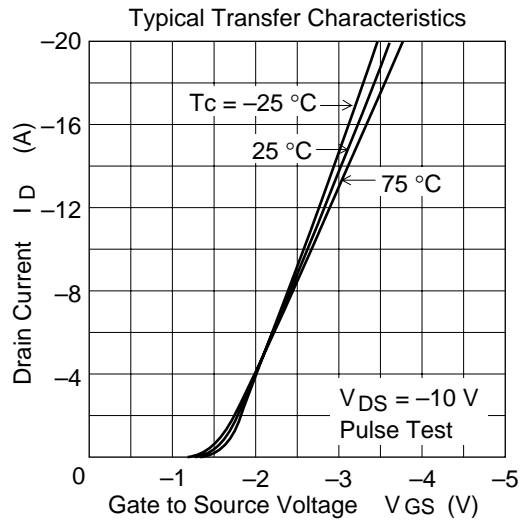
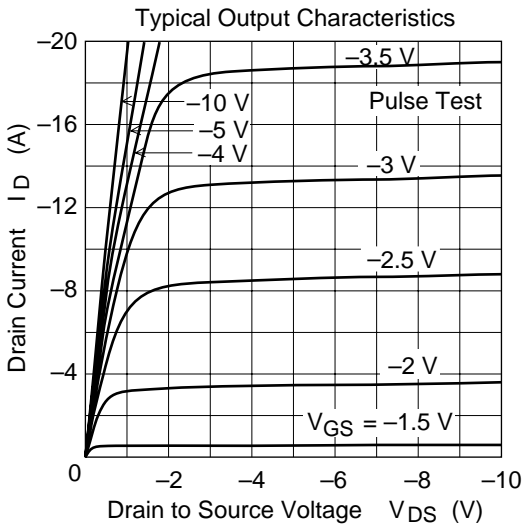
Note: 4. Pulse test

Main Characteristics

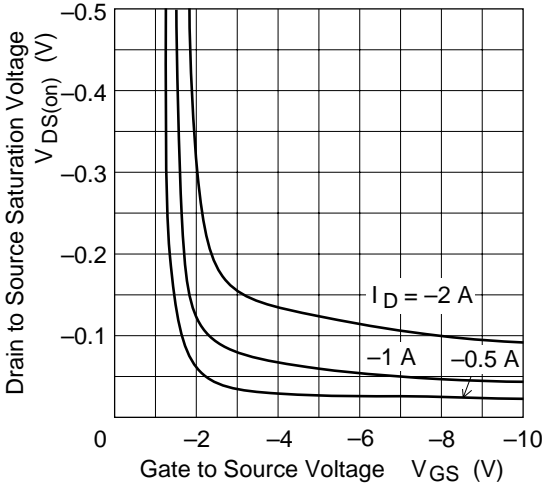


Note 5 :

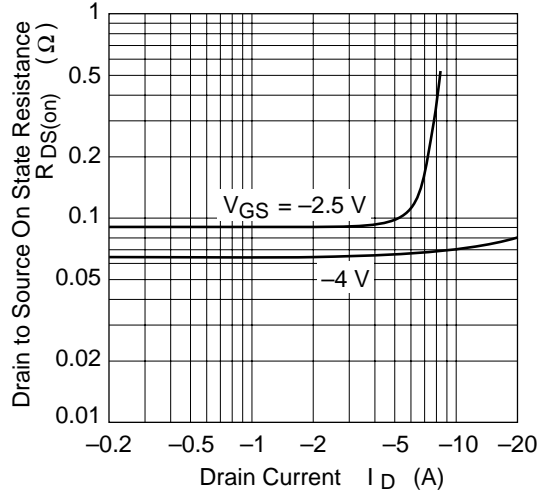
When using the glass epoxy board
(FR4 40x40x1.6 mm)



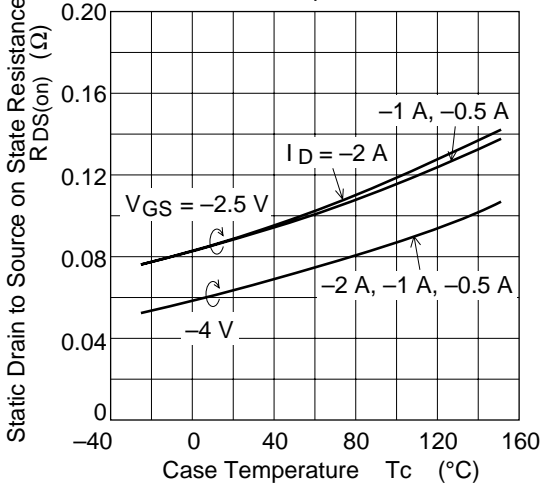
Drain to Source Saturation Voltage vs. Gate to Source Voltage



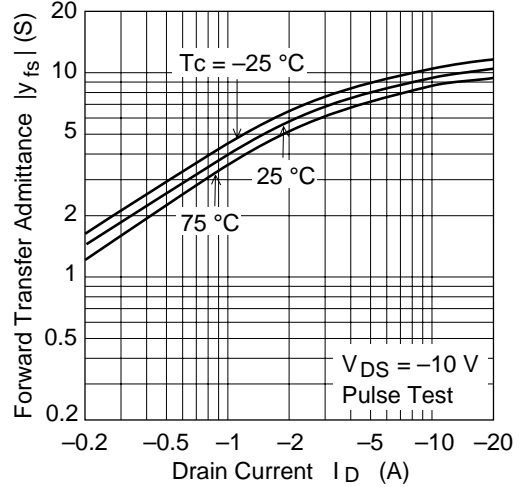
Static Drain to Source on State Resistance vs. Drain Current

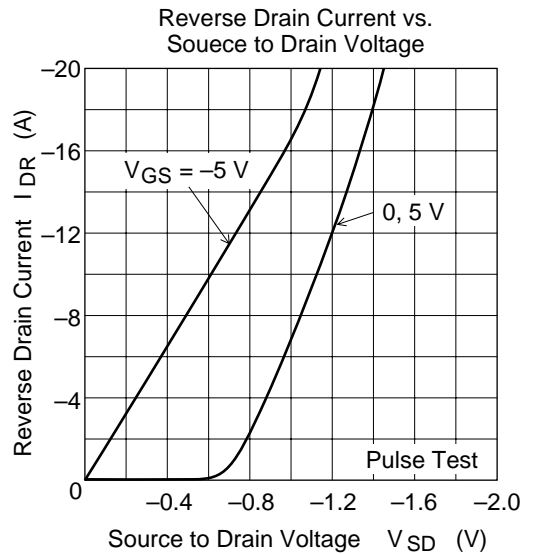
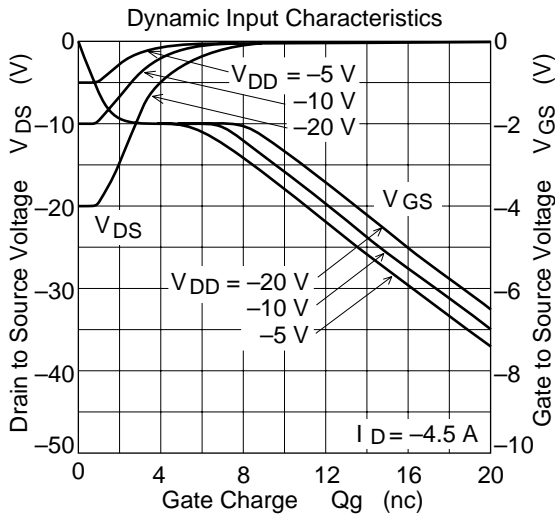
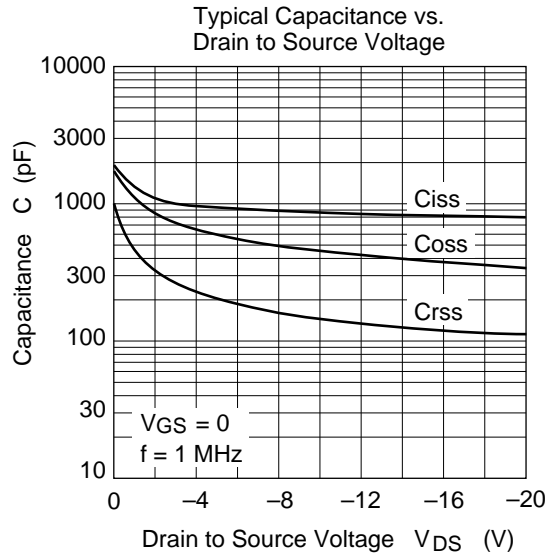
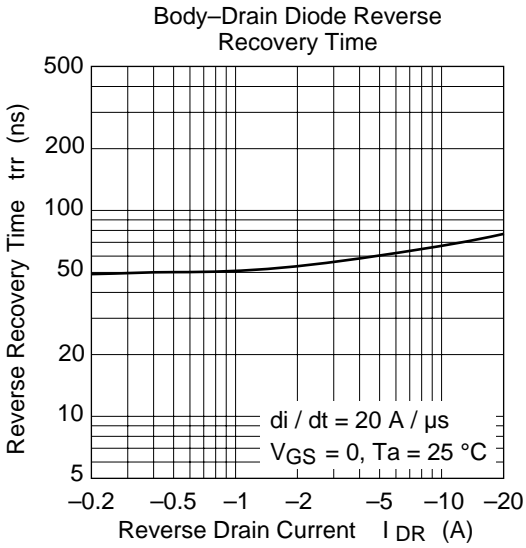


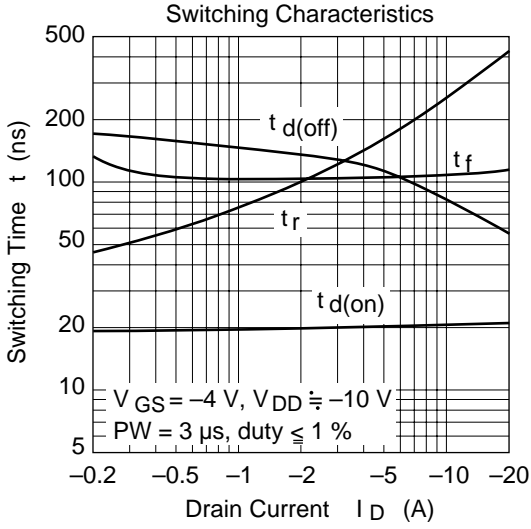
Static Drain to Source on State Resistance vs. Temperature



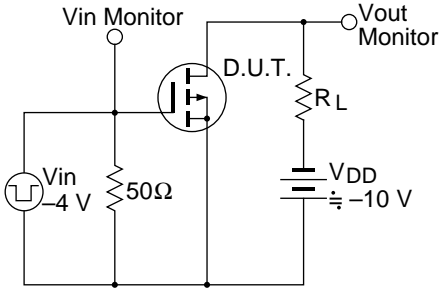
Forward Transfer Admittance vs. Drain Current



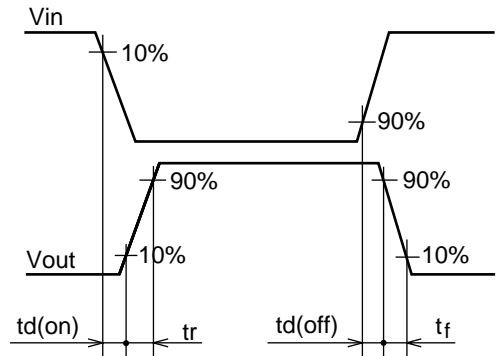




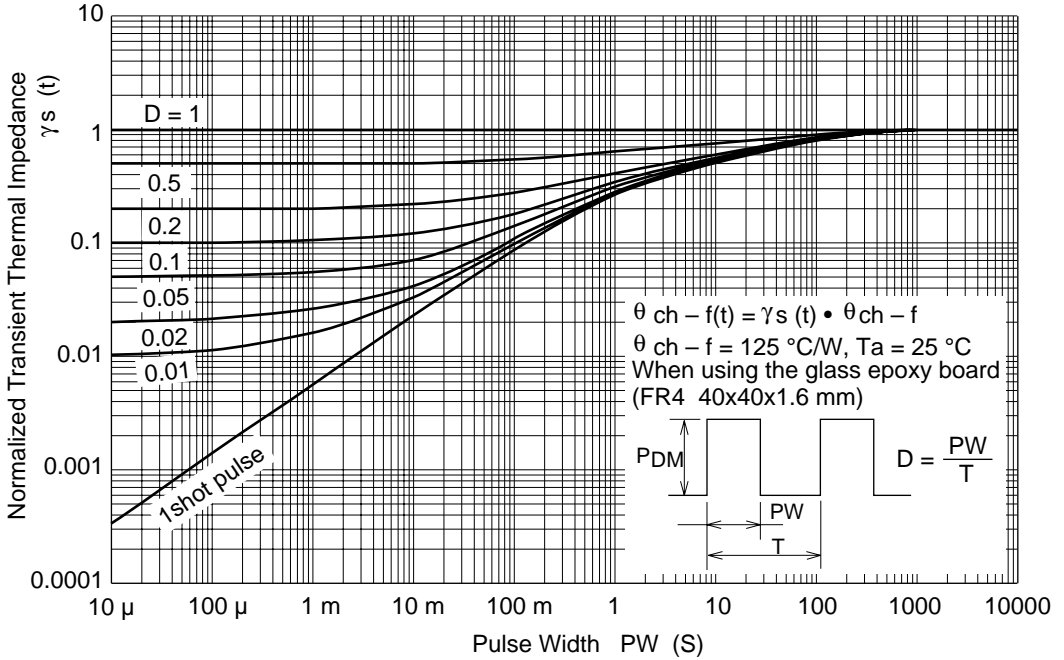
Switching Time Test Circuit



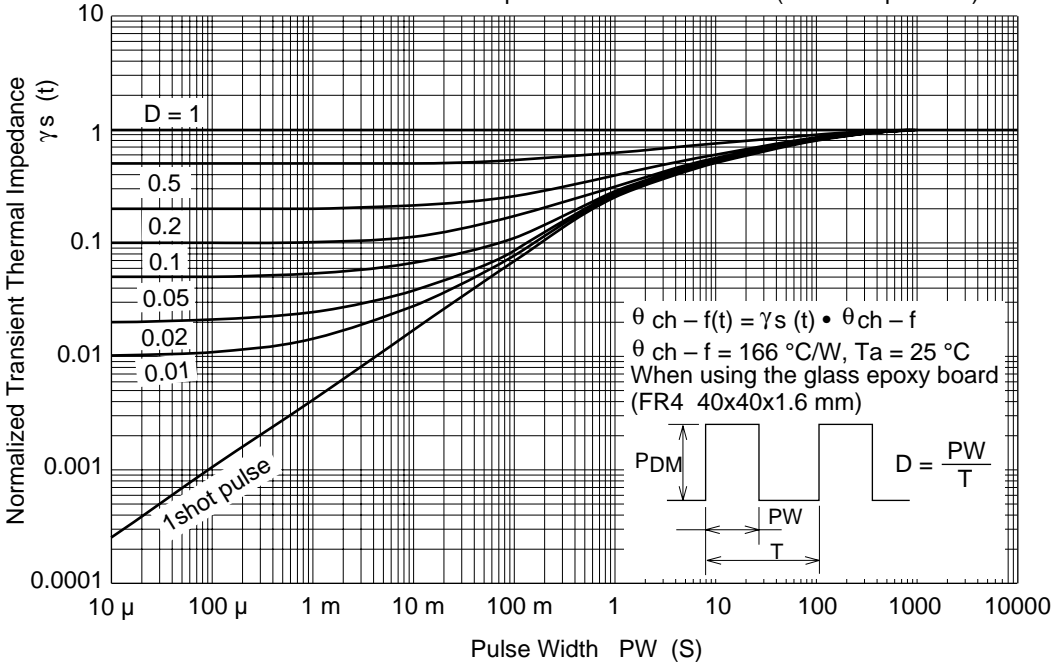
Switching Time Waveform



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

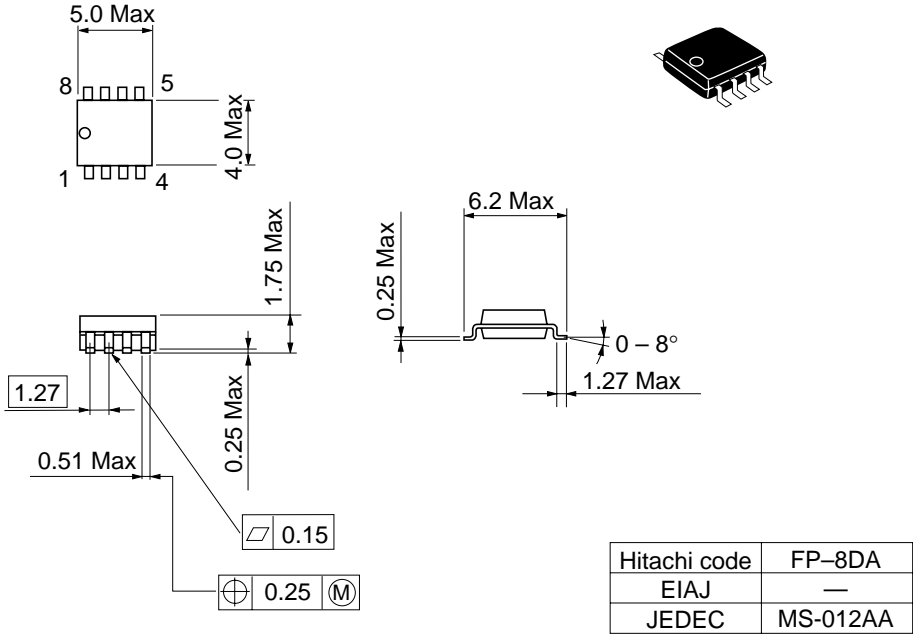


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions

Unit: mm



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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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