

HAT1043M

Silicon P Channel Power MOS FET
Power Switching

HITACHI

ADE-208-754D (Z)

5th Edition

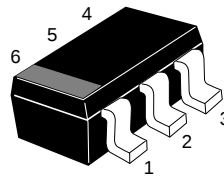
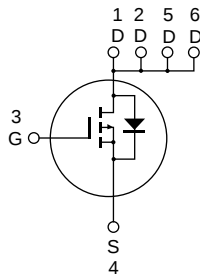
February 1999

Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device can be driven from 3 V source

Outline

TSOP-6



4 Source
3 Gate
1, 2, 5, 6 Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	−20	V
Gate to source voltage	V _{GSS}	±12	V
Drain current	I _D	−4.4	A
Drain peak current	I _{D(pulse)} ^{Note 1}	−17.6	A
Body-drain diode reverse drain current	I _{DR} ^{Note 2}	−4.4	A
Channel dissipation	Pch _(pulse) ^{Note 2}	2.0	W
	Pch _(continuous) ^{Note 3}	1.05	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

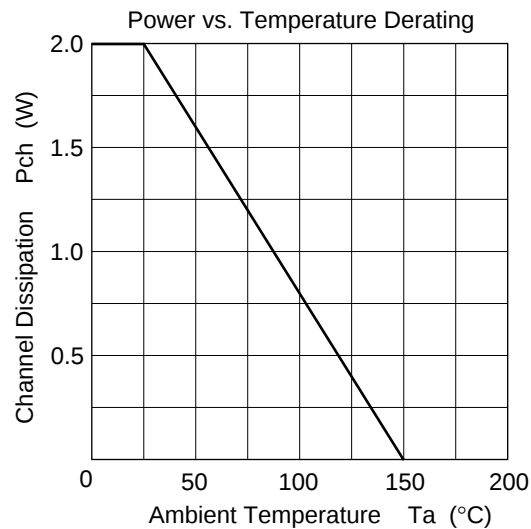
Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. When using the alumina ceramic board (50 x 50 x 0.7 mm), PW ≤ 5 s, Ta = 25°C
3. When using the alumina ceramic board (50 x 50 x 0.7 mm), Ta = 25°C

Electrical Characteristics (Ta = 25°C)

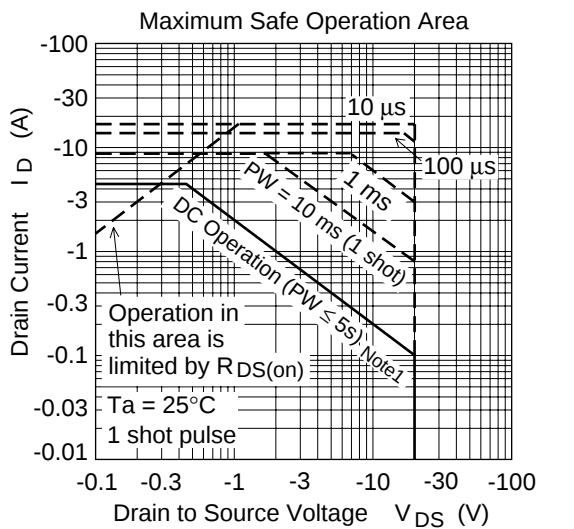
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	−20	—	—	V	I _D = −10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±12 V, V _{DS} = 0
Zero gate voltege drain current	I _{DSS}	—	—	−1	μA	V _{DS} = −20 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	−0.4	—	−1.4	V	I _D = −1 mA, V _{DS} = −10 V
Static drain to source on state resistance	R _{DS(on)}	—	55	65	mΩ	I _D = −3 A, V _{GS} = −4.5 V ^{Note 1}
		—	85	110	mΩ	I _D = −3 A, V _{GS} = −2.5 V ^{Note 1}
Forward transfer admittance	y _{fs}	4	7	—	S	I _D = −3 A, V _{DS} = −10 V ^{Note 1}
Input capacitance	Ciss	—	750	—	pF	V _{DS} = −10 V
Output capacitance	Coss	—	310	—	pF	V _{GS} = 0
Reverse transfer capacitance	Crss	—	220	—	pF	f = 1 MHz
Total Gate charge	Qg	—	11	—	nc	V _{DD} = −10 V
Gate to Source charge	Qgs	—	2	—	nc	V _{GS} = −4.5 V
Gate to Drain charge	Qgd	—	3.5	—	nc	I _D = −4.4 A
Turn-on delay time	t _{d(on)}	—	15	—	ns	V _{GS} = −4.5 V, I _D = −3 A
Rise time	t _r	—	100	—	ns	R _L = 3.3 Ω
Turn-off delay time	t _{d(off)}	—	85	—	ns	
Fall time	t _f	—	100	—	ns	
Body–drain diode forward voltage	V _{DF}	—	−0.95	−1.23	V	I _F = −4.4 A, V _{GS} = 0
Body–drain diode reverse recovery time	t _{rr}	—	50	—	ns	I _F = −4.4 A, V _{GS} = 0 diF/ dt = −20 A/ μs

Note: 1. Pulse test

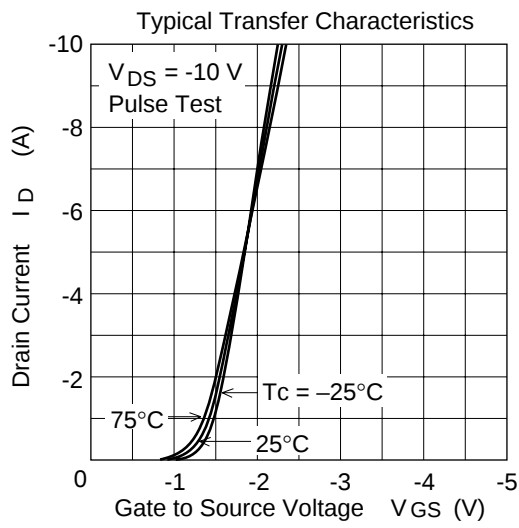
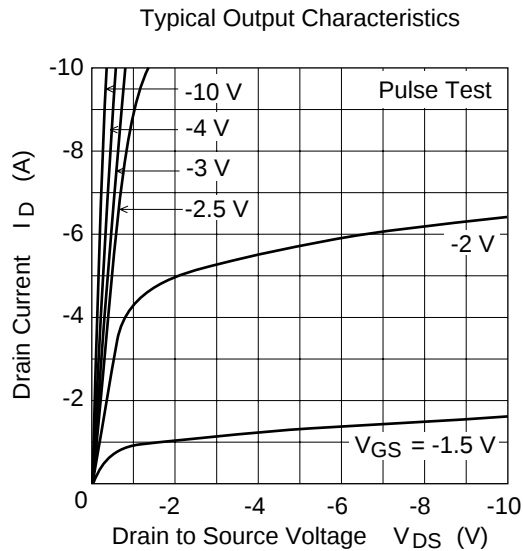
Main Characteristics



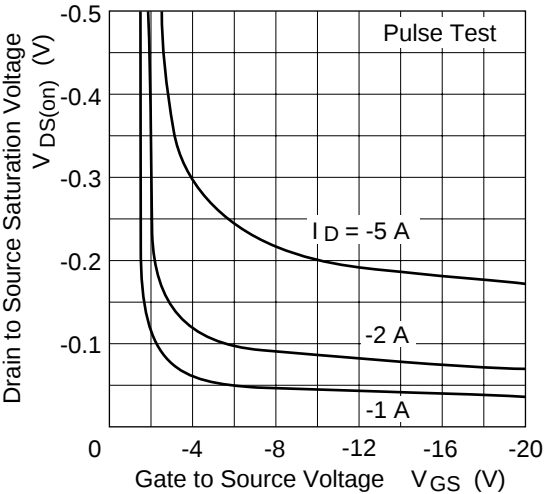
Test Condition
When using the alumina ceramic board
(50x50x0.7mm), ($PW \leq 5s$)



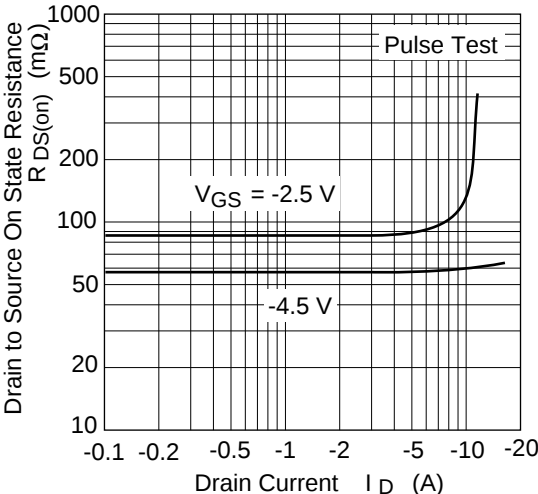
Note 1 When using the alumina ceramic board
(50x50x0.7mm)



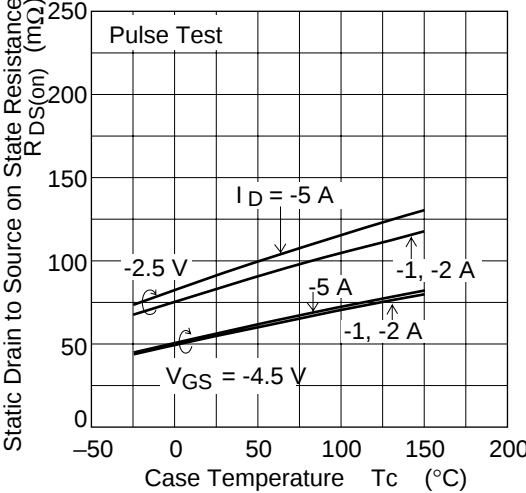
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



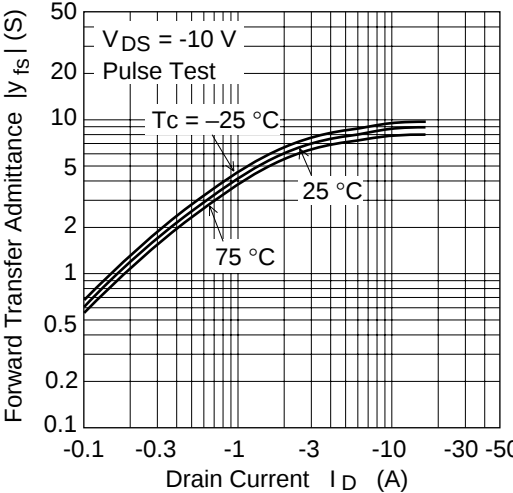
Static Drain to Source on State Resistance
vs. Drain Current

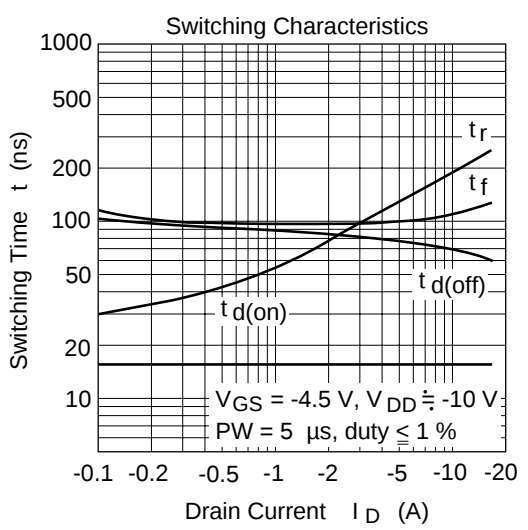
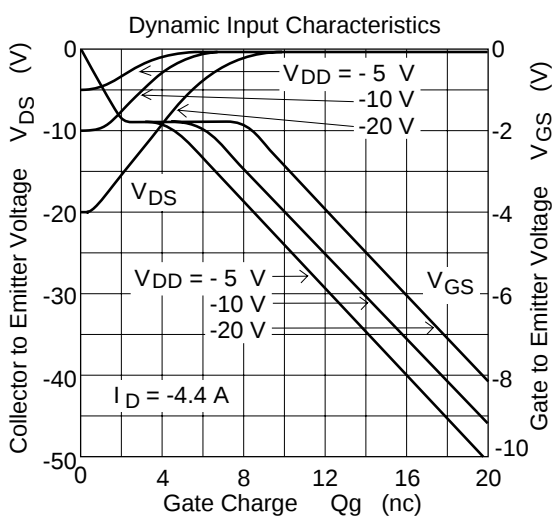
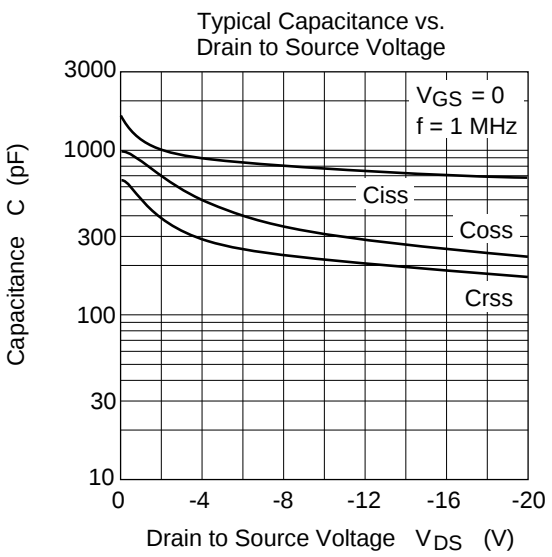
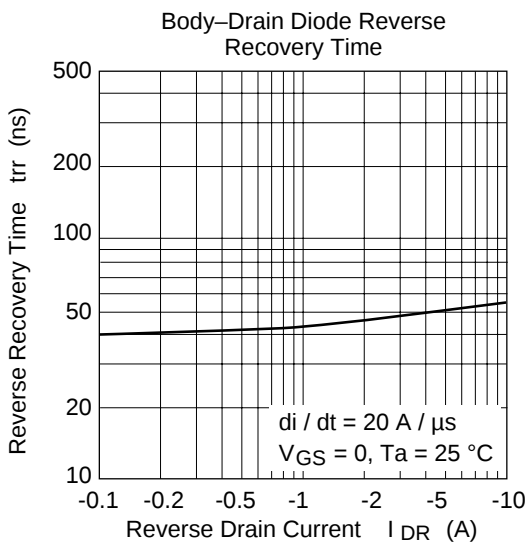


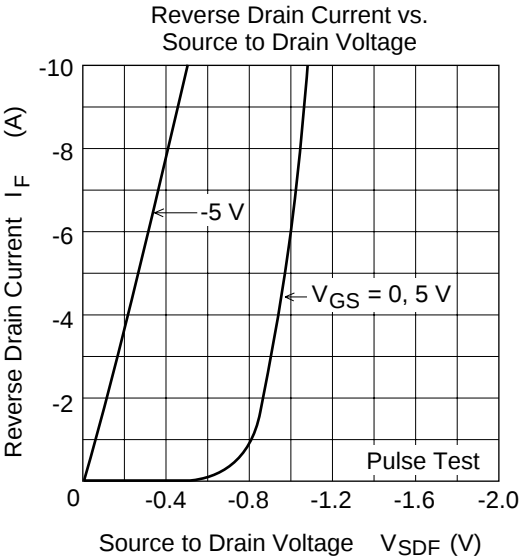
Static Drain to Source on State Resistance
vs. Temperature



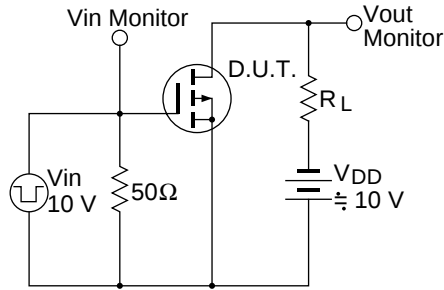
Forward Transfer Admittance vs.
Drain Current



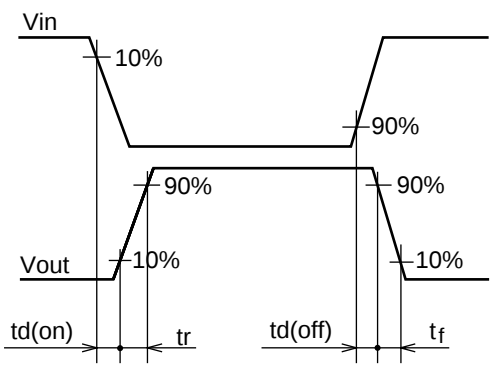




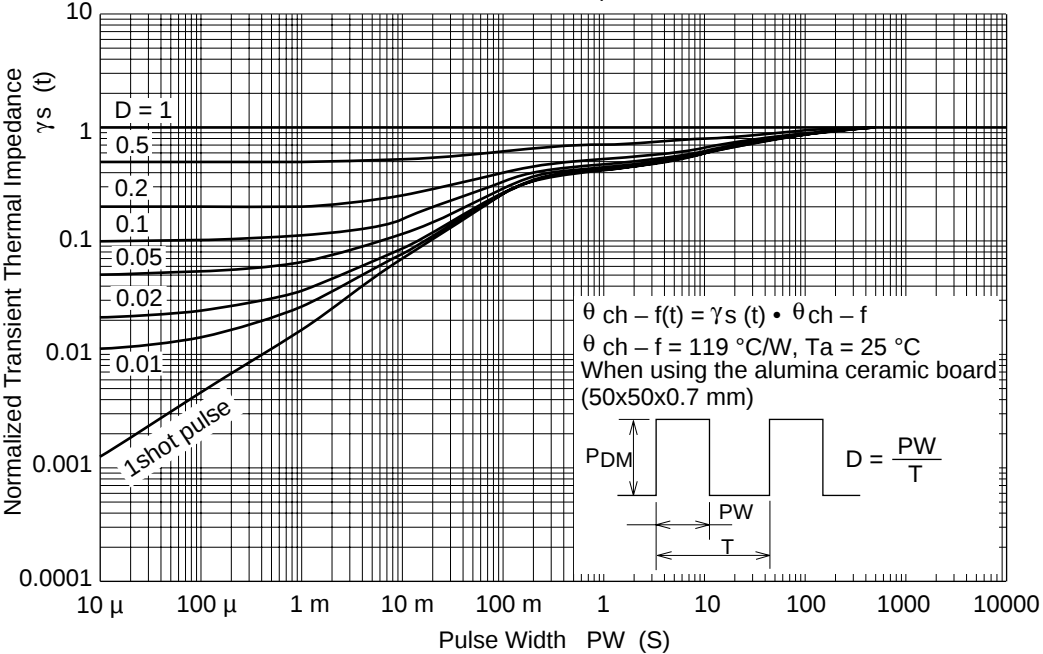
Switching Time Test Circuit



Switching Time Waveform

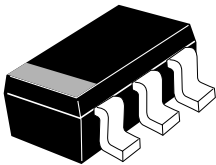
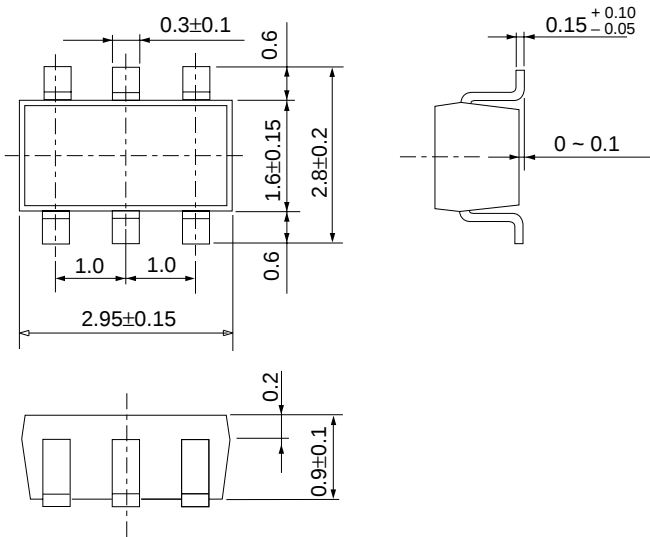


Normalized Transient Thermal Impedance vs. Pulse Width



Package Dimensions

Unit: mm



Hitachi Code	TSOP-6
EIAJ	-
JEDEC	-

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