HAT2038R/HAT2038RJ

Silicon N Channel Power MOS FET
High Speed Power Switching

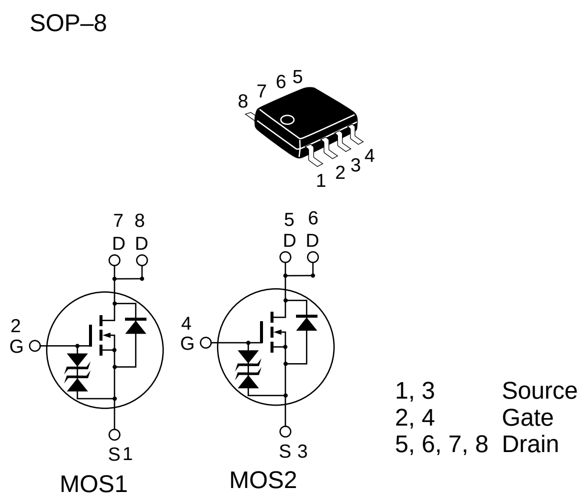
HITACHI

ADE-208-666C (Z)
4th. Edition
February 1999

Features

- For Automotive Application (at Type Code “J “)
- Low on-resistance
- Capable of 4 V gate drive
- High density mounting

Outline



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Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage		V_{DSS}	60	V
Gate to source voltage		V_{GSS}	± 20	V
Drain current		I_D	5	A
Drain peak current		$I_{D(pulse)}$ Note1	40	A
Body-drain diode reverse drain current		I_{DR}	5	A
Avalanche current	HAT2038R	I_{AP} Note4	—	—
	HAT2038RJ		5	A
Avalanche energy	HAT2038R	E_{AR} Note4	—	—
	HAT2038RJ		2.14	mJ
Channel dissipation		Pch Note2	2	W
Channel dissipation		Pch Note3	3	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	– 55 to + 150	°C

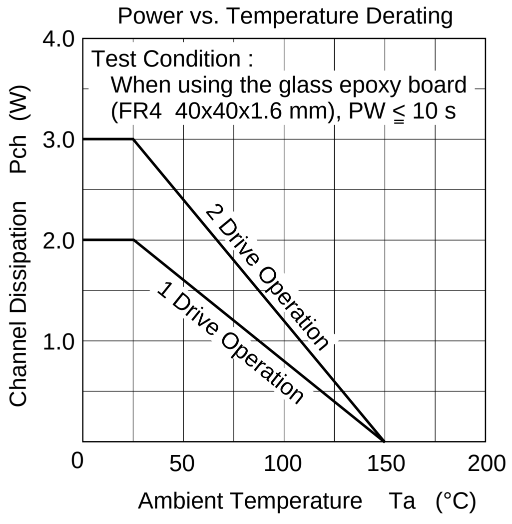
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s
4. Value at Tch=25°C, Rg≥50Ω

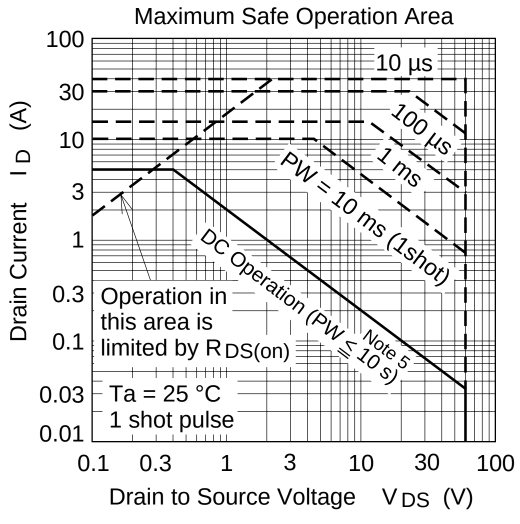
Electrical Characteristics (Ta = 25°C)

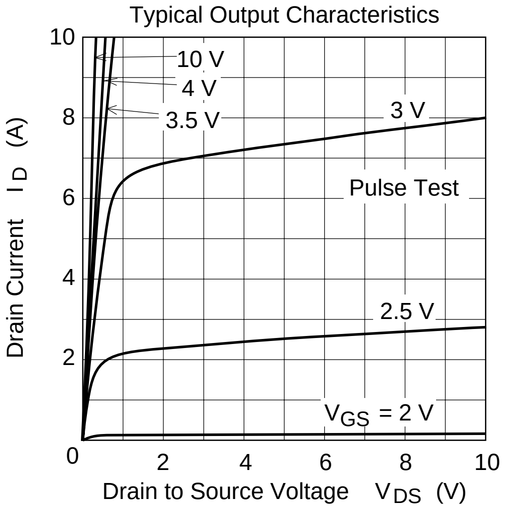
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)GSS}$	± 20	—	—	V	I_G = ± 100 μA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	± 10	μA	V_{GS} = ± 16 V, V_{DS} = 0
Zero gate voltage	HAT2038R	I_{DSS}	—	—	1	μA	V_{DS} = 60 V, V_{GS} = 0
drain current	HAT2038RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage	HAT2038R	I_{DSS}	—	—	—	μA	V_{DS} = 48 V, V_{GS} = 0
drain current	HAT2038RJ	I_{DSS}	—	—	10	μA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS(off)}$	1.2	—	2.2	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state		$R_{DS(on)}$	—	0.043	0.058	Ω	I_D = 3 A, V_{GS} = 10 V Note5
resistance		$R_{DS(on)}$	—	0.056	0.084	Ω	I_D = 3 A, V_{GS} = 4 V Note5
Forward transfer admittance		$\|y_{fs}\|$	6	9	—	S	I_D = 3 A, V_{DS} = 10 V Note5
Input capacitance		Ciss	—	520	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	270	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	100	—	pF	f = 1MHz
Turn-on delay time		$t_{d(on)}$	—	11	—	ns	V_{GS} =10 V, I_D = 3 A
Rise time		t_r	—	40	—	ns	V_{DD} ≅ 30 V
Turn-off delay time		$t_{d(off)}$	—	110	—	ns	
Fall time		t_f	—	80	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.84	1.1	V	IF = 5 A, V_{GS} = 0 Note5
Body–drain diode reverse recovery time		t_{rr}	—	40	—	ns	IF = 5 A, V_{GS} = 0 diF/ dt = 50 A/μs

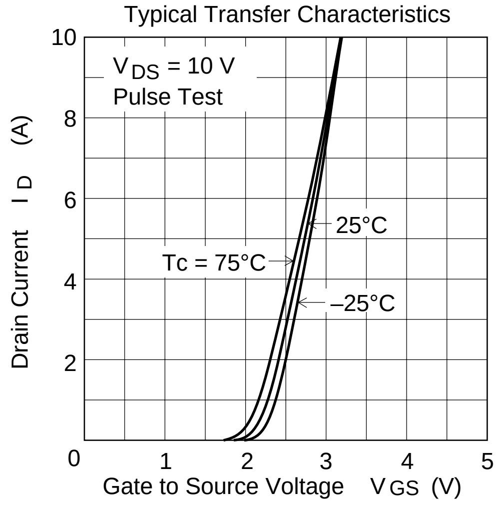
Note: 5. Pulse test

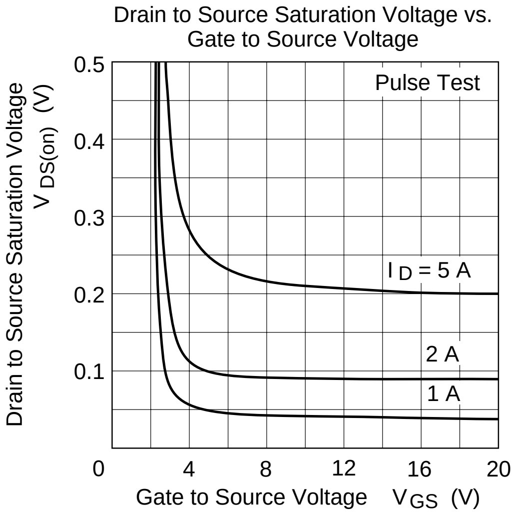
Main Characteristics

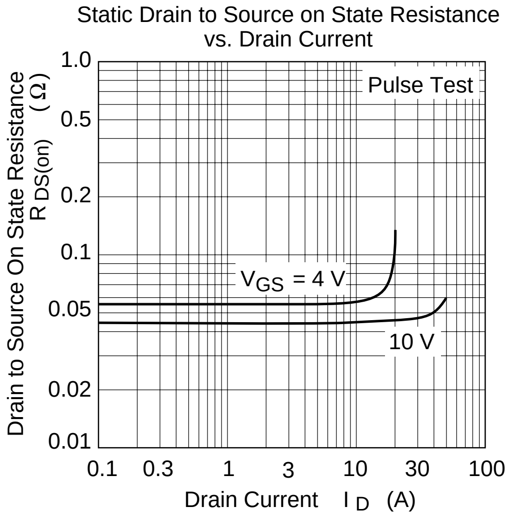


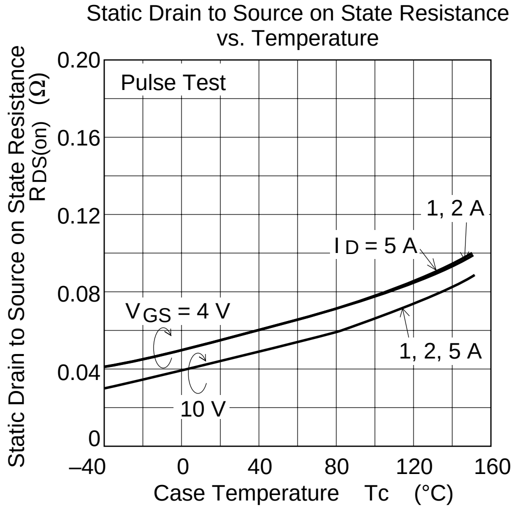


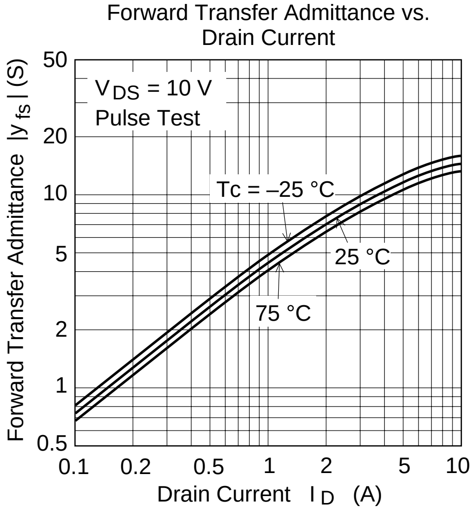


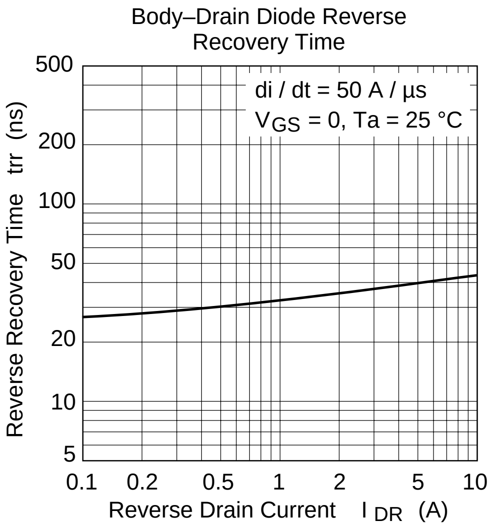


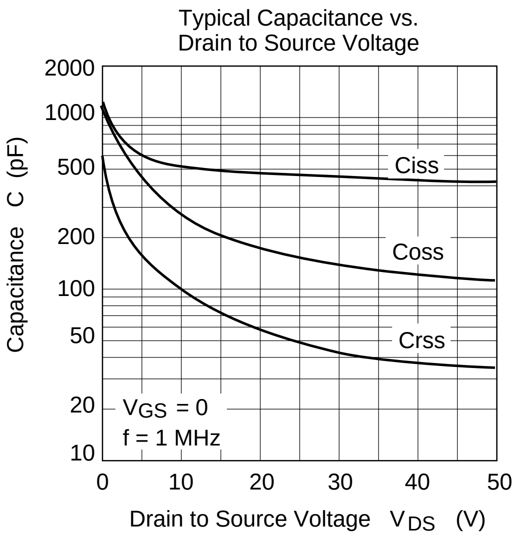

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 5 A
2 A
1 A
Drain to Source Saturation Voltage V DS(on) (V)
0.5
0.4
0.3
0.2
0.1
0
4
8
12
16
20
Gate to Source Voltage V GS (V)

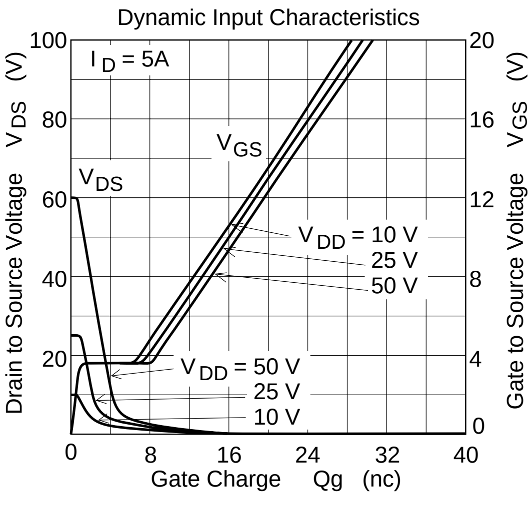

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = 4 V
10 V
Drain to Source On State Resistance R DS(on) (Ω)
1.0
0.5
0.2
0.1
0.05
0.02
0.01
0.1
0.3
1
3
10
30
100
Drain Current I D (A)

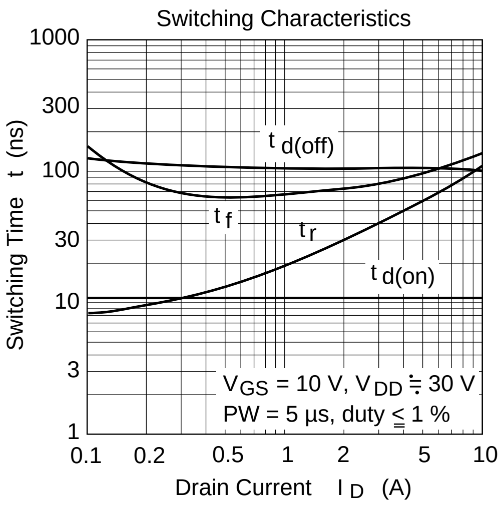

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
1, 2 A
I D = 5 A
V GS = 4 V
1, 2, 5 A
10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
V DS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
Forward Transfer Admittance |y fs | (S)
50
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

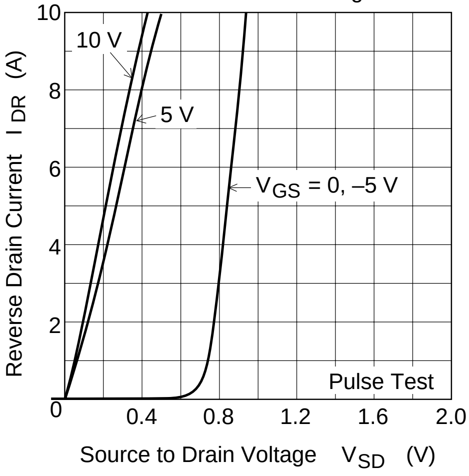

Body–Drain Diode Reverse Recovery Time
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
2000
1000
500
200
100
50
20
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

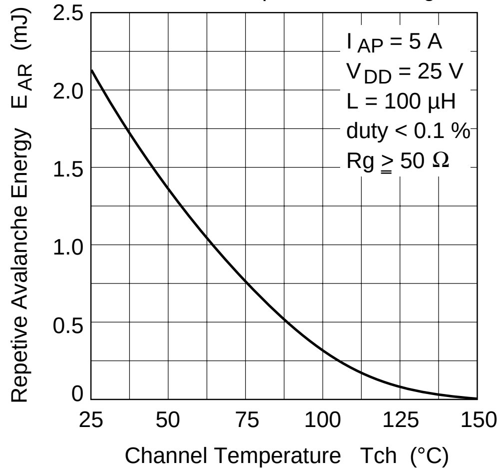

Dynamic Input Characteristics
I D = 5A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
20
16
12
8
4
0
VGS
VDS
VDD = 10 V
25 V
50 V
VDD = 50 V
25 V
10 V
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
1
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

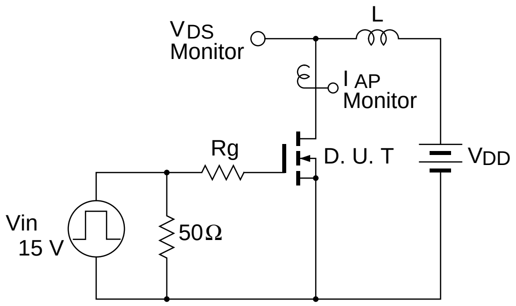
Reverse Drain Current vs.
Source to Drain Voltage



Maximun Avalanche Energy vs.
Channel Temperature Derating

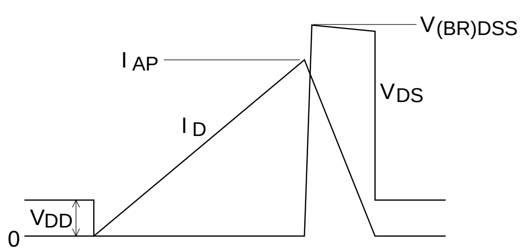


Avalanche Test Circuit

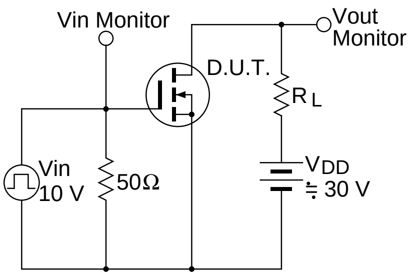


Avalanche Waveform

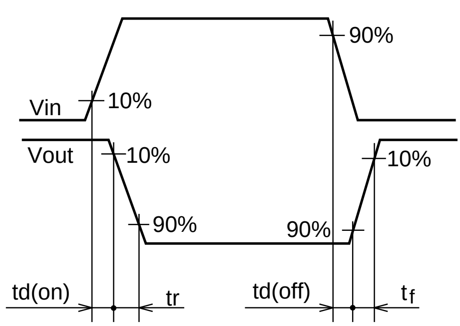
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

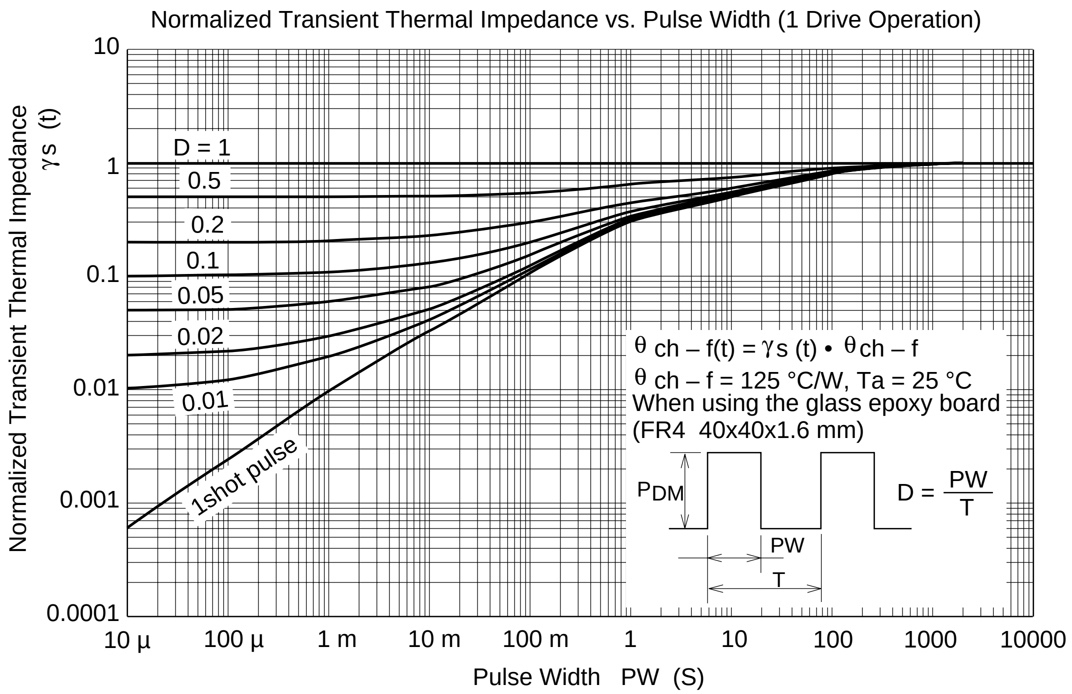


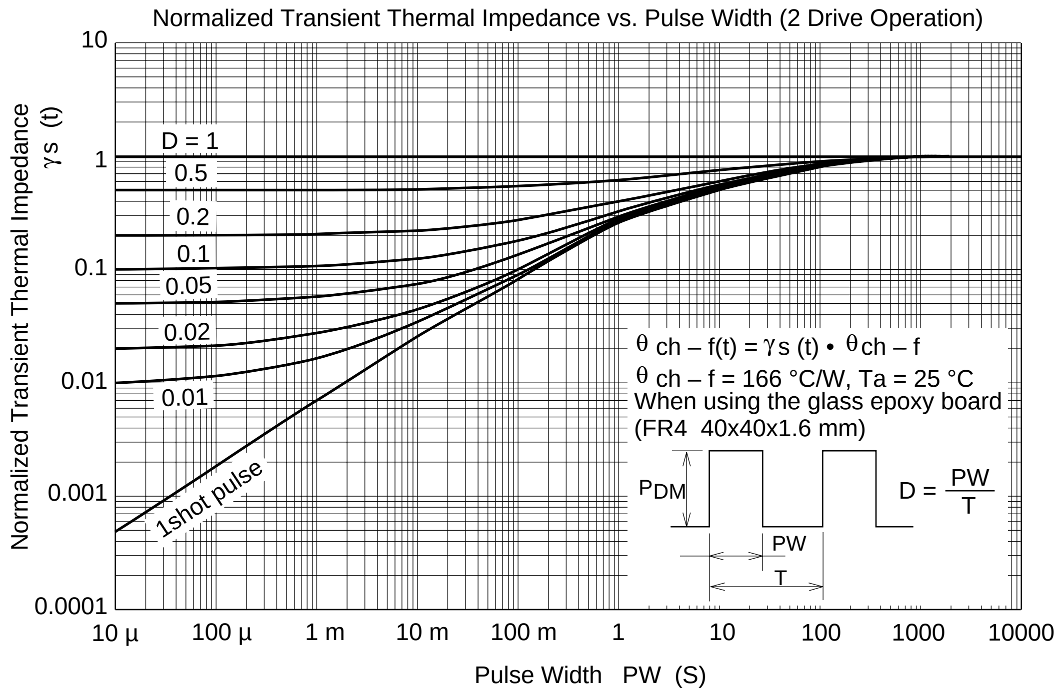
Switching Time Test Circuit



Switching Time Waveform

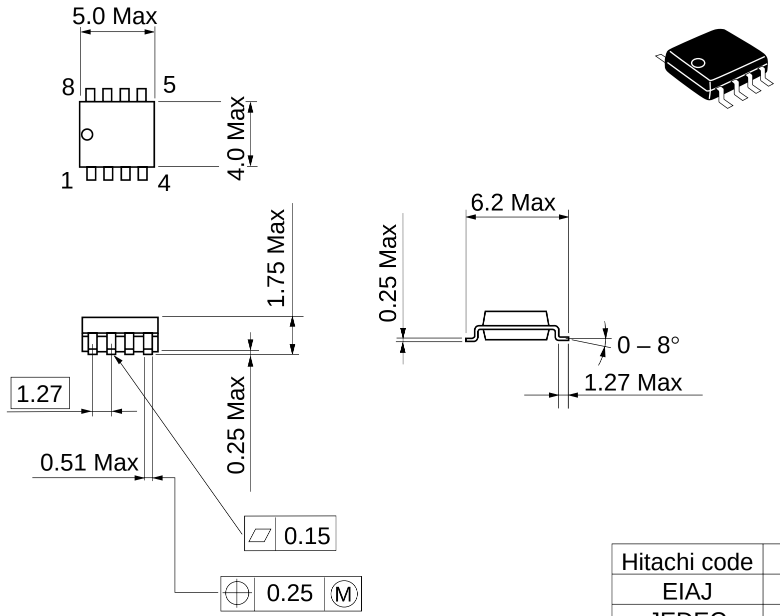



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θ ch – f(t) = γs (t) • θ ch – f
θ ch – f = 125 °C/W, Ta = 25 °C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
PW
T
D = PW / T
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θ ch – f(t) = γs (t) • θ ch – f
θ ch – f = 166 °C/W, Ta = 25 °C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
PW
T
D = PW / T
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

Package Dimensions

Unit: mm



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