HAT3008R/HAT3008RJ

Silicon N/P Channel Power MOS FET
High Speed Power Switching

HITACHI

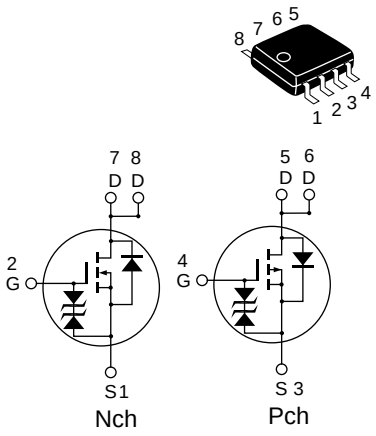
ADE-208-536B (Z)
3rd. Edition
February 1999

Features

- For Automotive Application (at Type Code “J “)
- Low on-resistance
- Capable of 4 V gate drive
- High density mounting

Outline

SOP–8



1, 3	Source
2, 4	Gate
5, 6, 7, 8	Drain

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings		Unit
			Nch	Pch	
Drain to source voltage		V_{DSS}	60	– 60	V
Gate to source voltage		V_{GSS}	±20	± 20	V
Drain current		I_D	5	– 3.5	A
Drain peak current		$I_{D(pulse)}$ Note1	40	– 28	A
Body-drain diode		I_{DR}	5	– 3.5	A
reverse drain current					
Avalanche current	HAT3008R	I_{AP} Note4	—	—	—
	HAT3008RJ		5	– 3.5	A
Avalanche energy	HAT3008R	E_{AR} Note4	—	—	—
	HAT3008RJ		2.14	1.05	mJ
Channel dissipation		Pch Note2	2	2	W
Channel dissipation		Pch Note3	3	3	W
Channel temperature		Tch	150	150	°C
Storage temperature		Tstg	– 55 to + 150	–55 to + 150	°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s
4. Value at Tch=25°C, Rg≥50Ω

Electrical Characteristics (Ta = 25°C)

(N Channel)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)GSS}$	± 20	—	—	V	I_G = ± 100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	± 10	µA	V_{GS} = ± 16 V, V_{DS} = 0
Zero gate voltage	HAT3008R	I_{DSS}	—	—	1	µA	V_{DS} = 60 V, V_{GS} = 0
drain current	HAT3008RJ	I_{DSS}	—	—	0.1	µA	
Zero gate voltage	HAT3008R	I_{DSS}	—	—	—	µA	V_{DS} = 48 V, V_{GS} = 0
drain current	HAT3008RJ	I_{DSS}	—	—	10	µA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS(off)}$	1.2	—	2.2	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance		$R_{DS(on)}$	—	0.043	0.058	Ω	I_D = 3 A, V_{GS} = 10 V [Note4]
		$R_{DS(on)}$	—	0.056	0.084	Ω	I_D = 3 A, V_{GS} = 4 V [Note4]
Forward transfer admittance		$\|y_{fs}\|$	6	9	—	S	I_D = 3 A, V_{DS} = 10 V [Note4]
Input capacitance		Ciss	—	520	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	270	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	100	—	pF	f = 1MHz
Turn-on delay time		$t_{d(on)}$	—	11	—	ns	V_{GS} =10 V, I_D = 3 A
Rise time		t_r	—	40	—	ns	V_{DD} ≅ 30 V
Turn-off delay time		$t_{d(off)}$	—	110	—	ns	
Fall time		t_f	—	80	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.84	1.1	V	IF = 5 A, V_{GS} = 0 [Note4]
Body–drain diode reverse recovery time		t_{rr}	—	40	—	ns	IF =5 A, V_{GS} = 0 diF/ dt = 50 A/µs

Note: 5. Pulse test

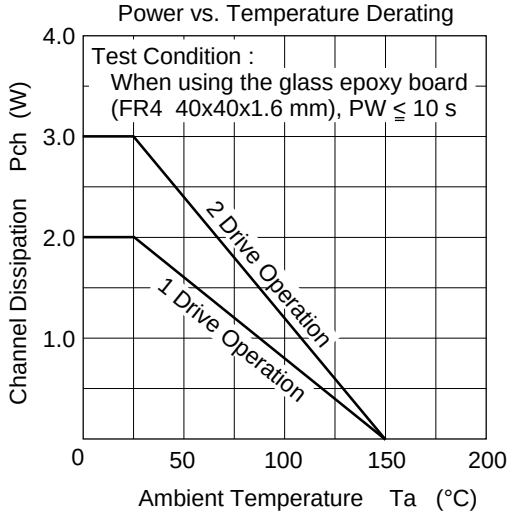
(P Channel)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	– 60	—	—	V	I_D = – 10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)GSS}$	± 20	—	—	V	I_G = ± 100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ± 16 V, V_{DS} = 0
Zero gate voltage	HAT3008R	I_{DSS}	—	—	–1	µA	V_{DS} = – 60 V, V_{GS} = 0
drain current	HAT3008RJ	I_{DSS}	—	—	–0.1	µA	
Zero gate voltage	HAT3008R	I_{DSS}	—	—	—	µA	V_{DS} = – 48 V, V_{GS} = 0
drain current	HAT3008RJ	I_{DSS}	—	—	–10	µA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS(off)}$	–1.2	—	–2.2	V	V_{DS} = – 10 V, I_D = – 1mA
Static drain to source on state		$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = – 2 A, V_{GS} = – 10 V [Note4]
resistance		$R_{DS(on)}$	—	0.16	0.23	Ω	I_D = – 2 A, V_{GS} = – 4 V [Note4]
Forward transfer admittance		$\|y_{fs}\|$	3	4.5	—	S	I_D = – 2 A, V_{DS} = –10 V [Note4]
Input capacitance		Ciss	—	600	—	pF	V_{DS} = –10 V
Output capacitance		Coss	—	290	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	75	—	pF	f = 1MHz
Turn-on delay time		$t_{d(on)}$	—	11	—	ns	V_{GS} = –10 V, I_D = – 2 A
Rise time		t_r	—	30	—	ns	V_{DD} ≅ – 30 V
Turn-off delay time		$t_{d(off)}$	—	100	—	ns	
Fall time		t_f	—	55	—	ns	
Body–drain diode forward voltage		V_{DF}	—	– 0.98	– 1.28	V	IF = – 3.5 A, V_{GS} = 0 [Note4]
Body–drain diode reverse recovery time		t_{rr}	—	70	—	ns	IF = – 3.5 A, V_{GS} = 0 diF/ dt = 50 A/µs

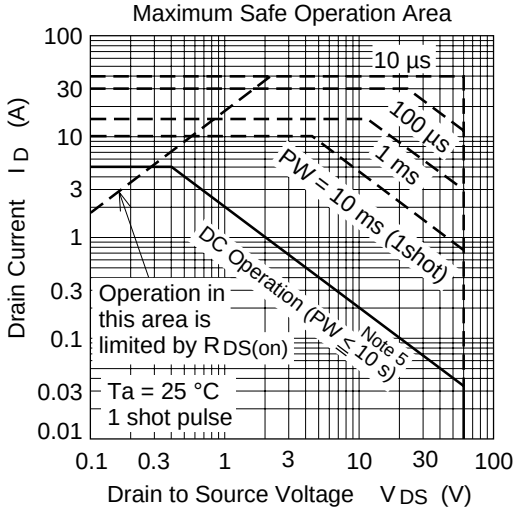
Note: 5. Pulse test

Main Characteristics (N Channel)

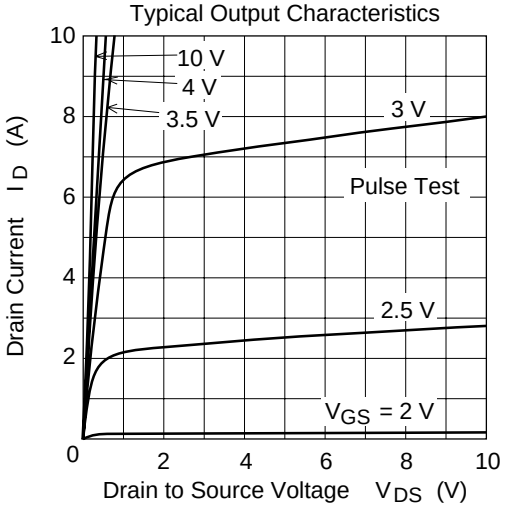
Power vs. Temperature Derating



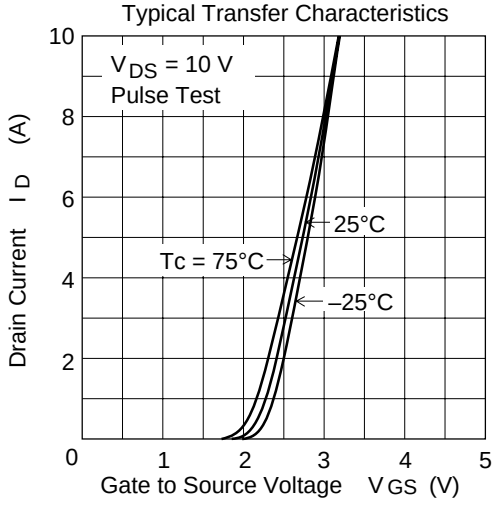
Maximum Safe Operation Area



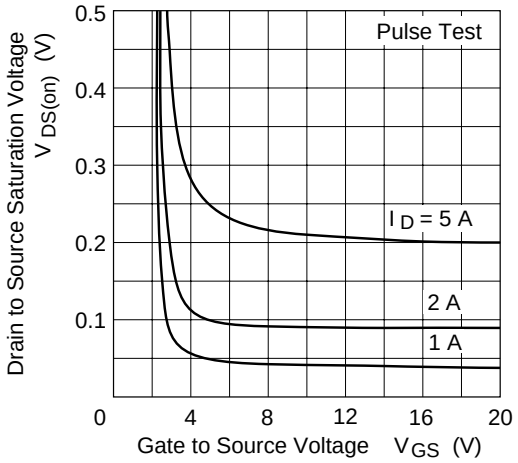
Typical Output Characteristics



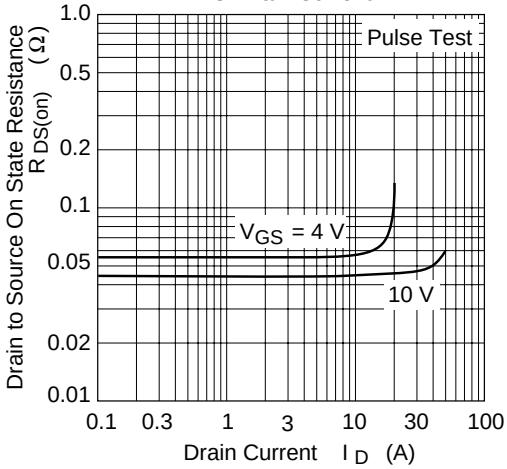
Typical Transfer Characteristics



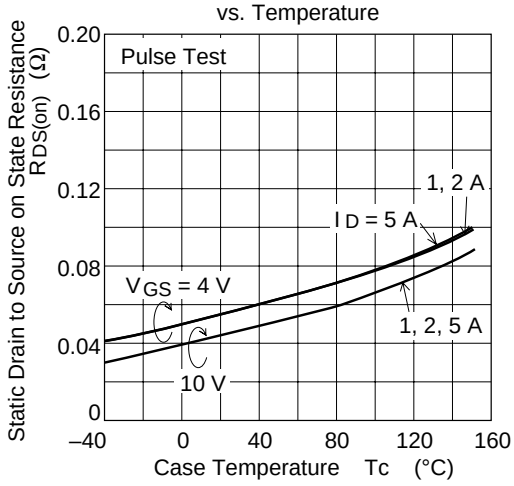
Drain to Source Saturation Voltage vs. Gate to Source Voltage



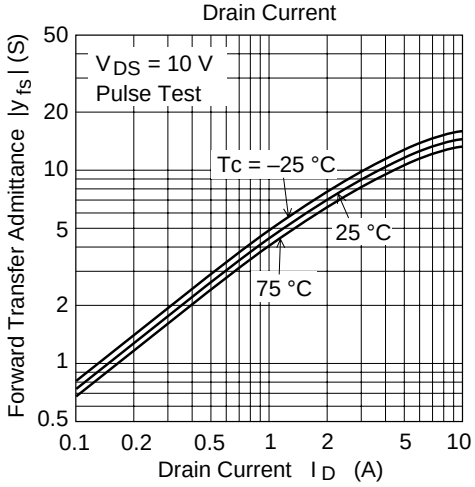
Static Drain to Source on State Resistance vs. Drain Current



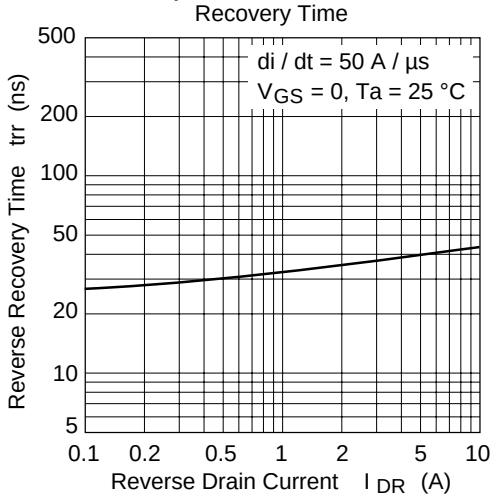
Static Drain to Source on State Resistance vs. Temperature



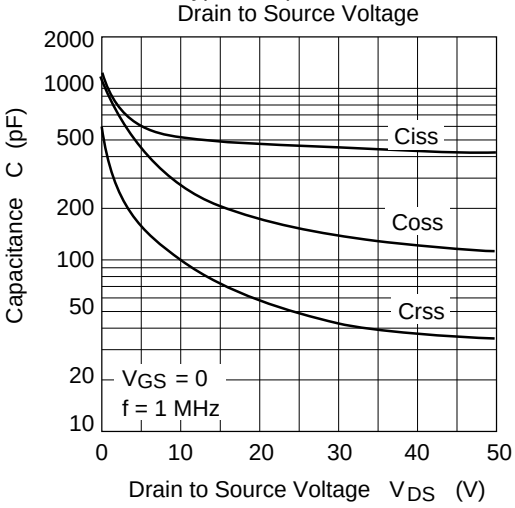
Forward Transfer Admittance vs. Drain Current



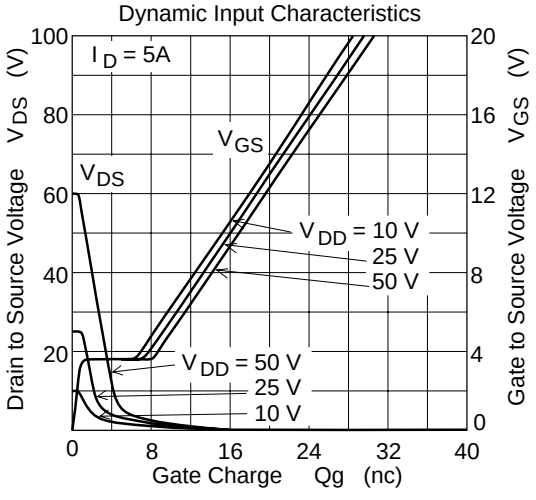
Body–Drain Diode Reverse Recovery Time



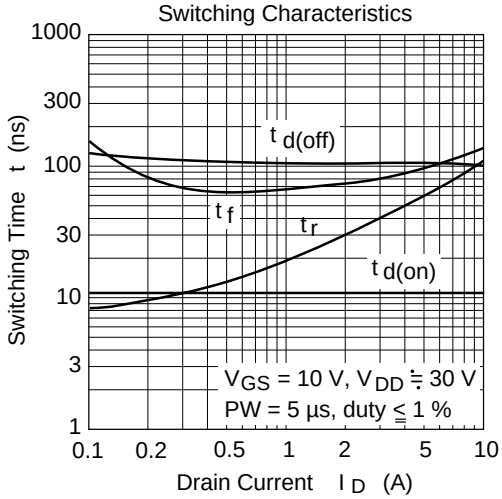
Typical Capacitance vs. Drain to Source Voltage



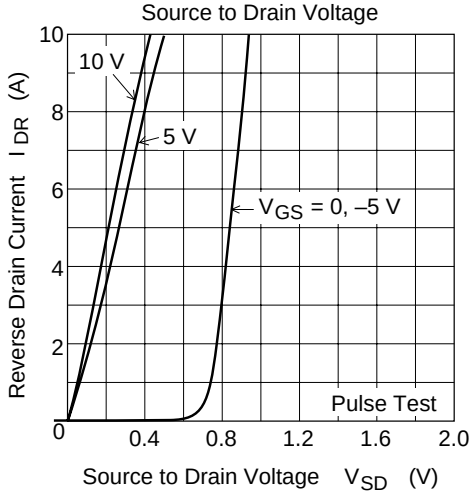
Dynamic Input Characteristics



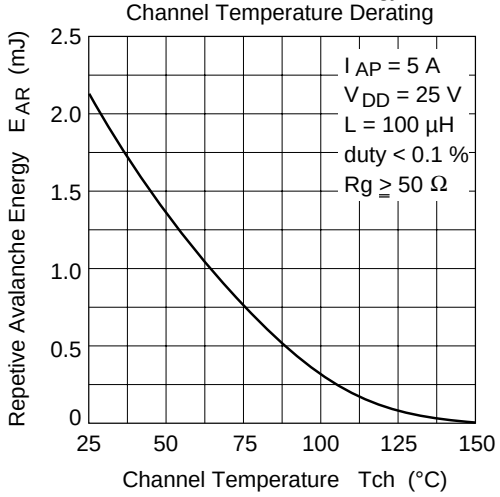
Switching Characteristics



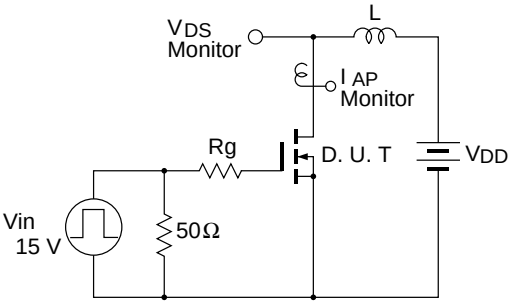
Reverse Drain Current vs.
Source to Drain Voltage



Maximun Avalanche Energy vs.
Channel Temperature Derating

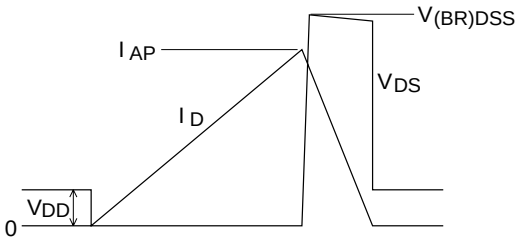


Avalanche Test Circuit

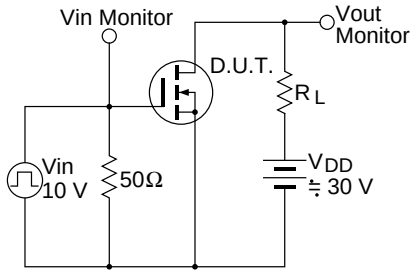


Avalanche Waveform

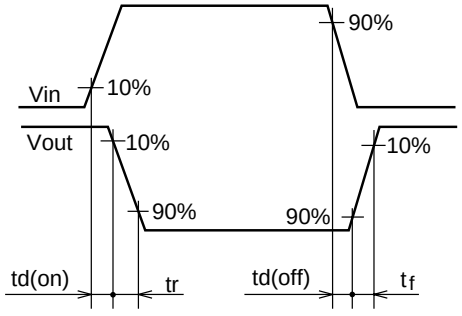
$$E_{AR} = \frac{1}{2} \bullet L \bullet {I_{AP}}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

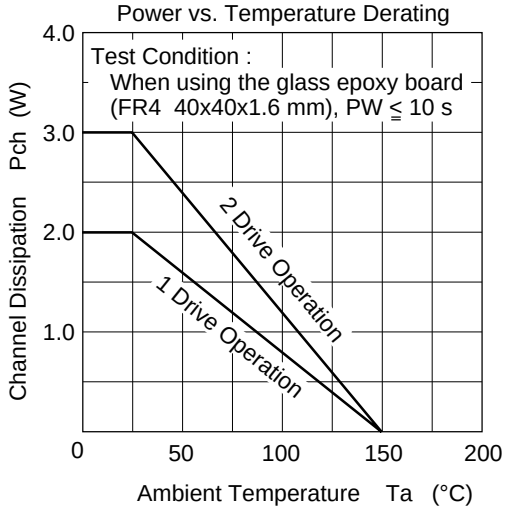


Switching Time Waveform

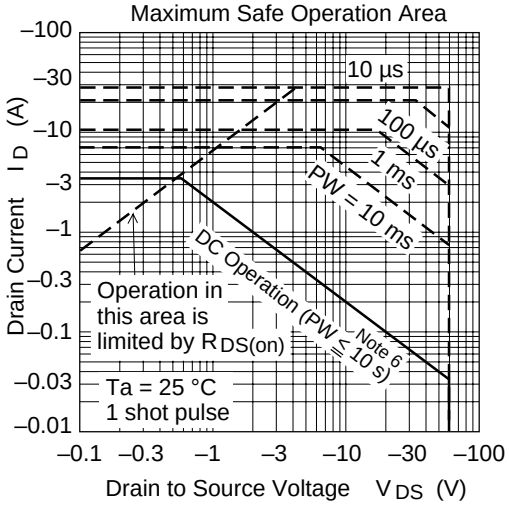


(P Channel)

Power vs. Temperature Derating

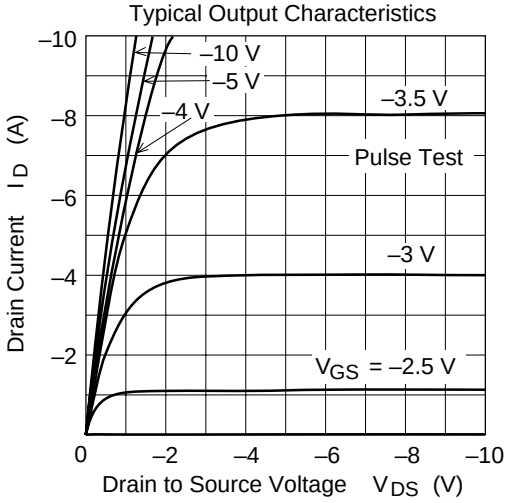


Maximum Safe Operation Area

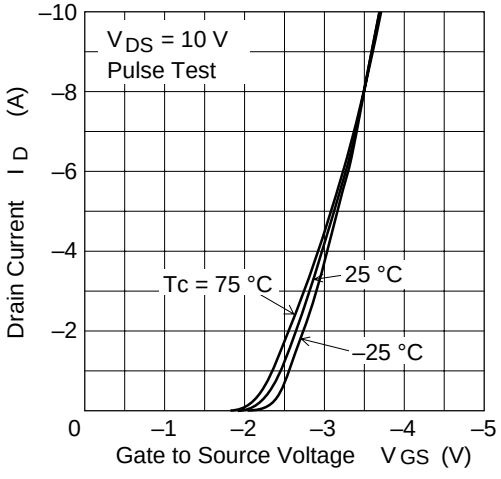


Note 6 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

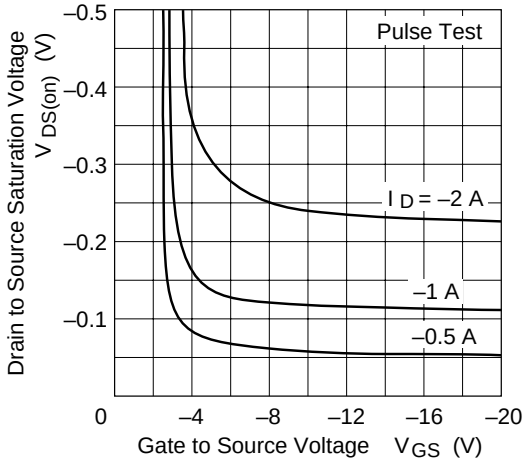
Typical Output Characteristics



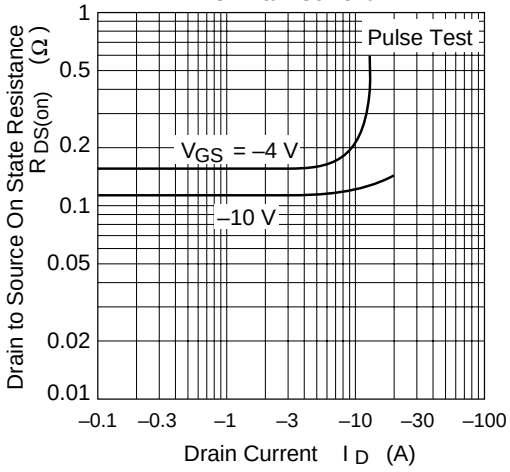
Typical Transfer Characteristics



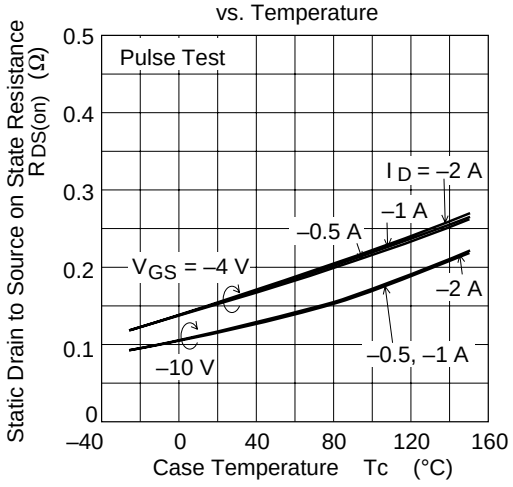
Drain to Source Saturation Voltage vs. Gate to Source Voltage



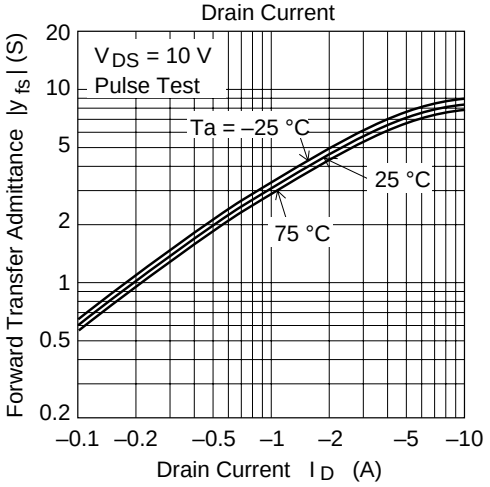
Static Drain to Source on State Resistance vs. Drain Current



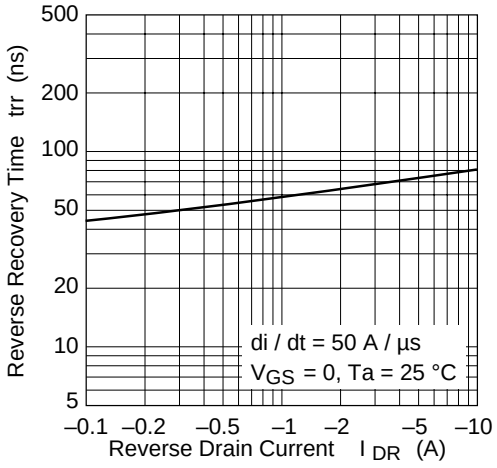
Static Drain to Source on State Resistance vs. Temperature



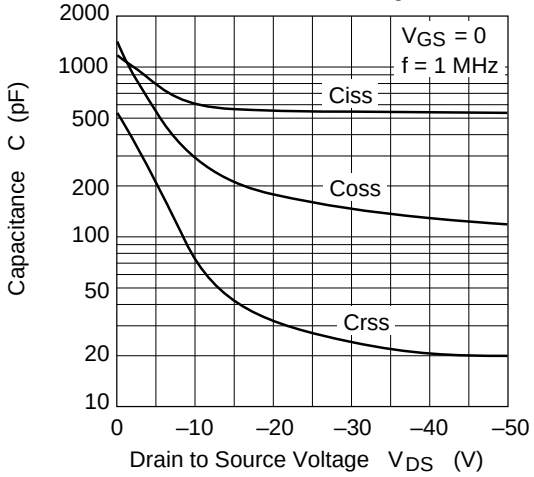
Forward Transfer Admittance vs. Drain Current



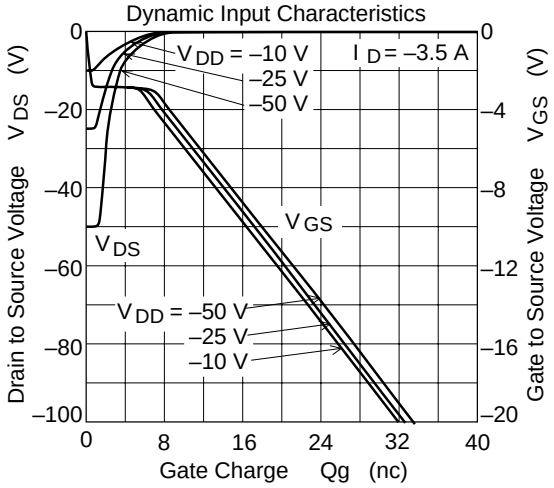
Body–Drain Diode Reverse Recovery Time



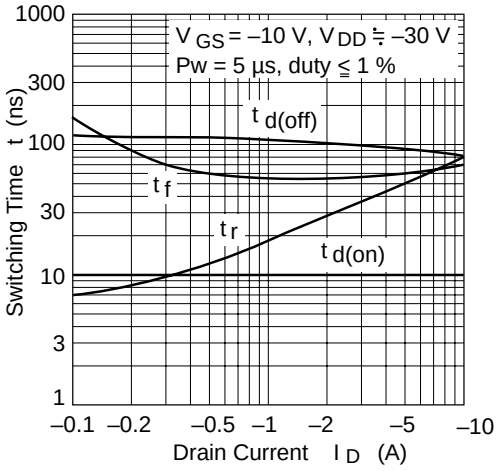
Typical Capacitance vs. Drain to Source Voltage



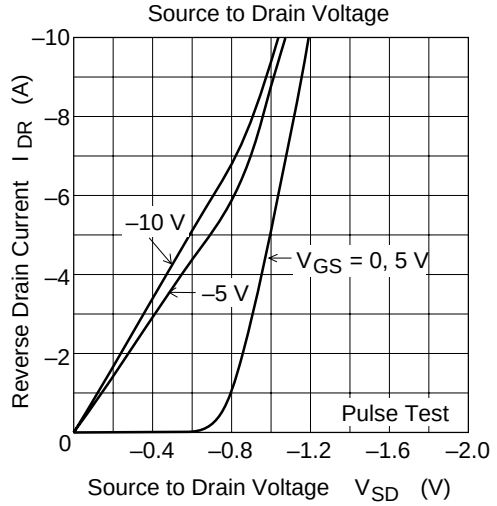
Dynamic Input Characteristics



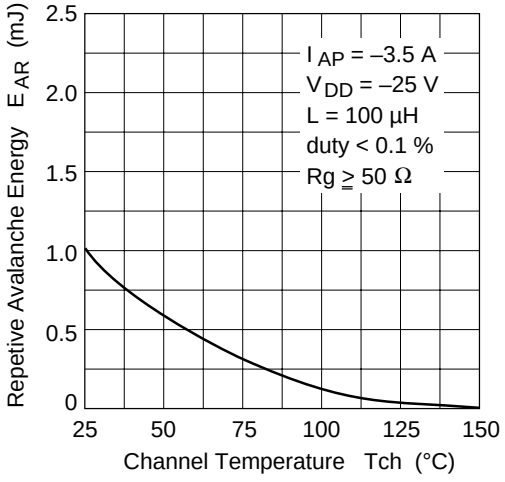
Switching Characteristics



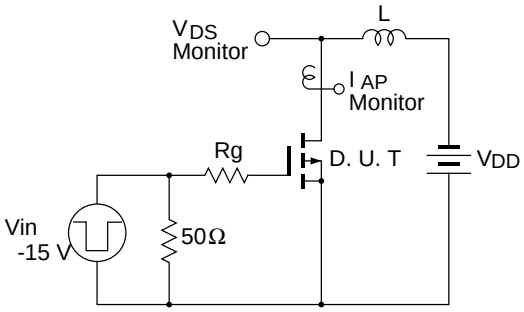
Reverse Drain Current vs.
Source to Drain Voltage



Maximun Avalanche Energy vs.
Channel Temperature Derating

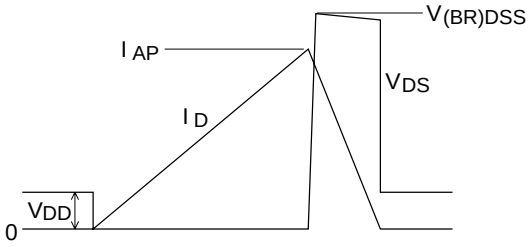


Avalanche Test Circuit

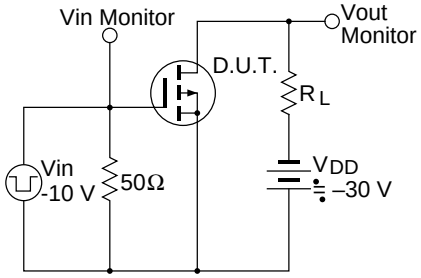


Avalanche Waveform

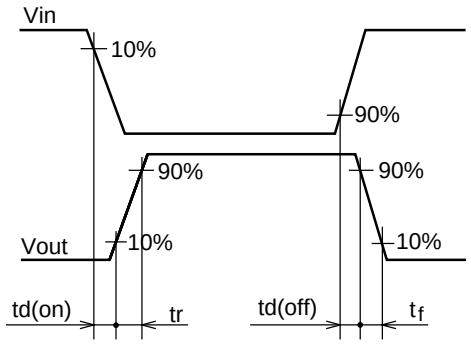
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



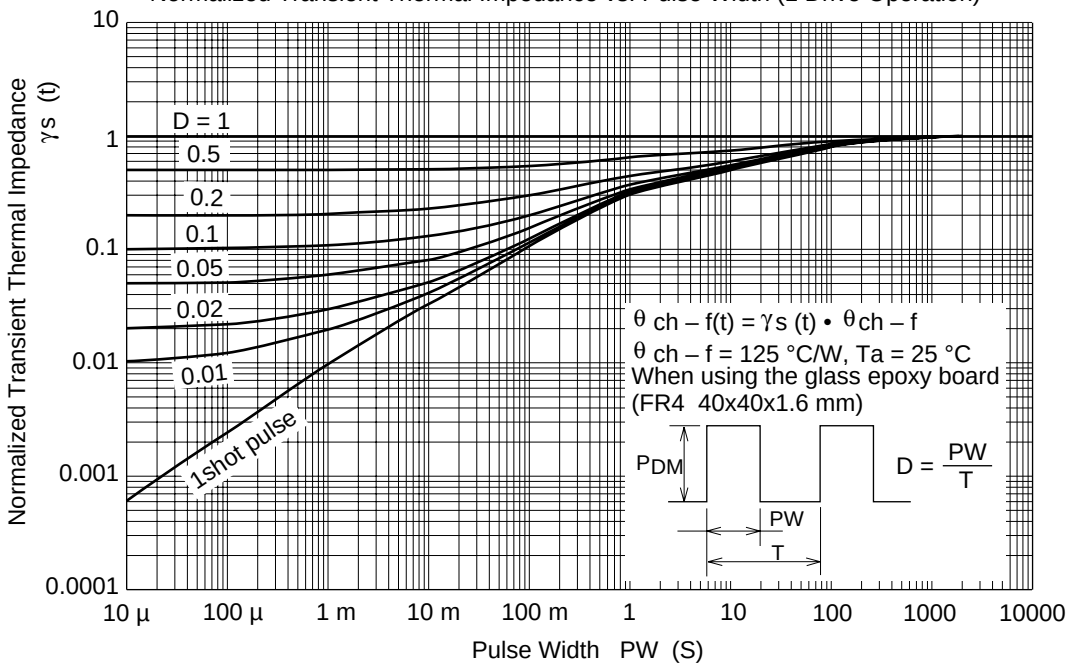
Switching Time Test Circuit



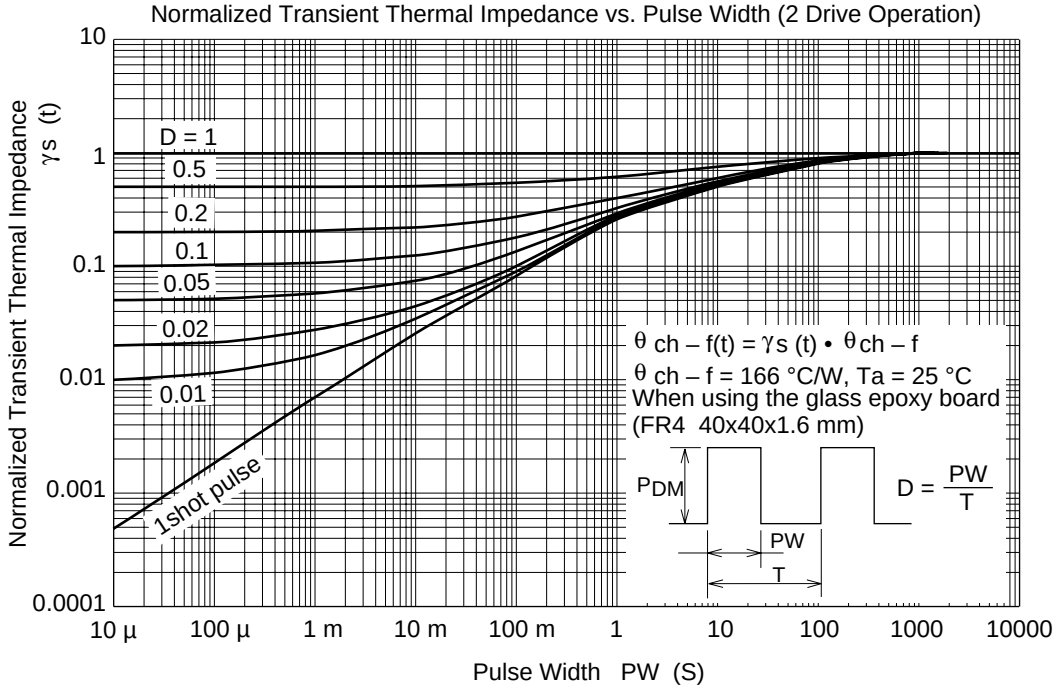
Switching Time Waveform



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

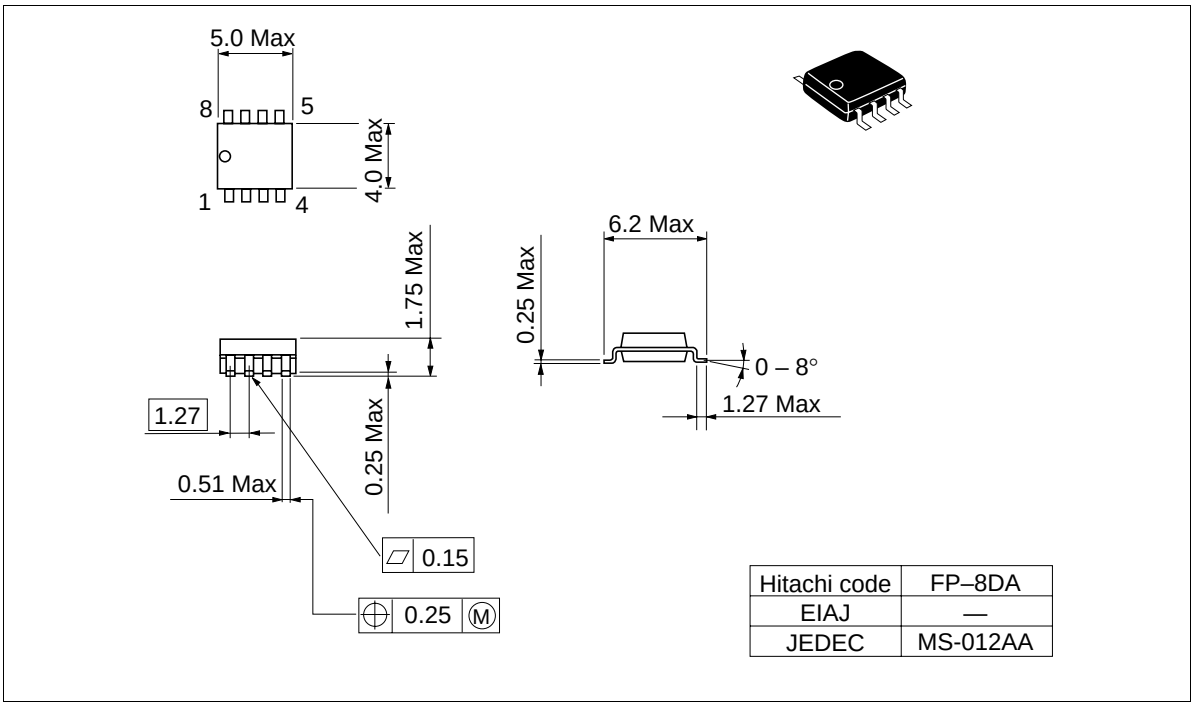


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions

Unit: mm



Hitachi code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

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