
HD74ALVCH16260

12-bit to 24-bit Multiplexed D-type Latches with 3-state Outputs

HITACHI

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Description

The HD74ALVCH16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and / or demultiplexing of address and data information in microprocessor or bus interface applications. This device is also useful in memory interleaving applications. Three 12-bit I / O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and / or data transfer. The output enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction. Address and / or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Features

- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ (@ $V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ (@ $V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 24 \text{ mA}$ (@ $V_{CC} = 3.0 \text{ V}$)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors

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Function Table

Inputs						Output A
1B	2B	SEL	LE1B	LE2B	$\overline{OE\bar{A}}$	
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0^{*1}
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0^{*1}
X	X	X	X	X	H	Z

B-to-A ($\overline{OE\bar{B}} = H$)

Inputs					Outputs	
A	LEA1B	LEA2B	$\overline{OE1\bar{B}}$	$\overline{OE2\bar{B}}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0^{*1}$
L	H	L	L	L	L	$2B_0^{*1}$
H	L	H	L	L	$1B_0^{*1}$	H
L	L	H	L	L	$1B_0^{*1}$	L
X	L	L	L	L	$1B_0^{*1}$	$2B_0^{*1}$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

A-to-B ($\overline{OE\bar{A}} = H$)

H : High level

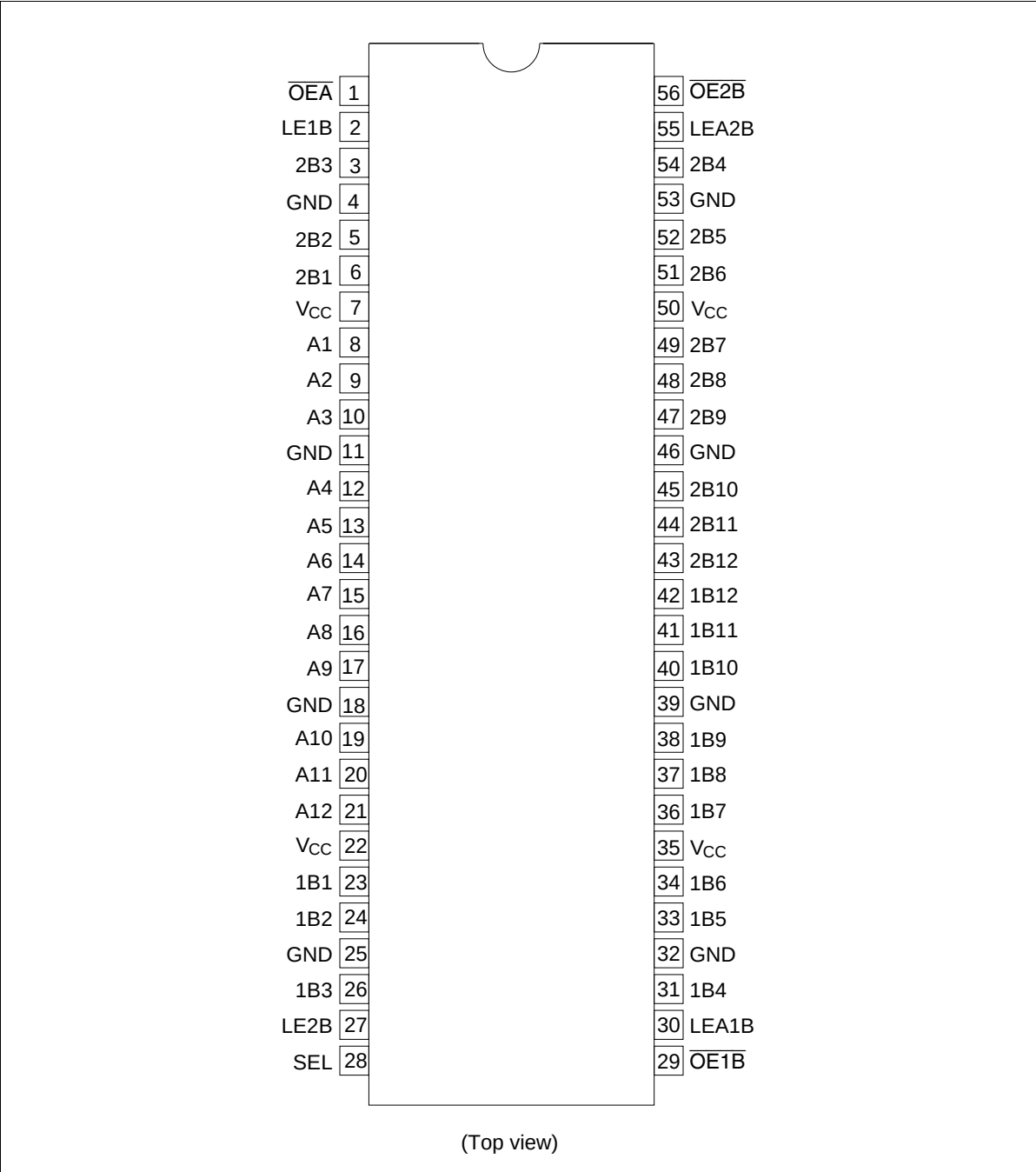
L : Low level

X : Immaterial

Z : High impedance

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	−0.5 to 4.6	V	
Input voltage ^{*1, 2}	V_I	−0.5 to 4.6	V	Except I/O ports
		−0.5 to $V_{CC} + 0.5$		I/O ports
Output voltage ^{*1, 2}	V_O	−0.5 to $V_{CC} + 0.5$	V	
Input clamp current	I_{IK}	−50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
V_{CC} , GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ^{*3}	P_T	1	W	TSSOP
Storage temperature	T_{stg}	−65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

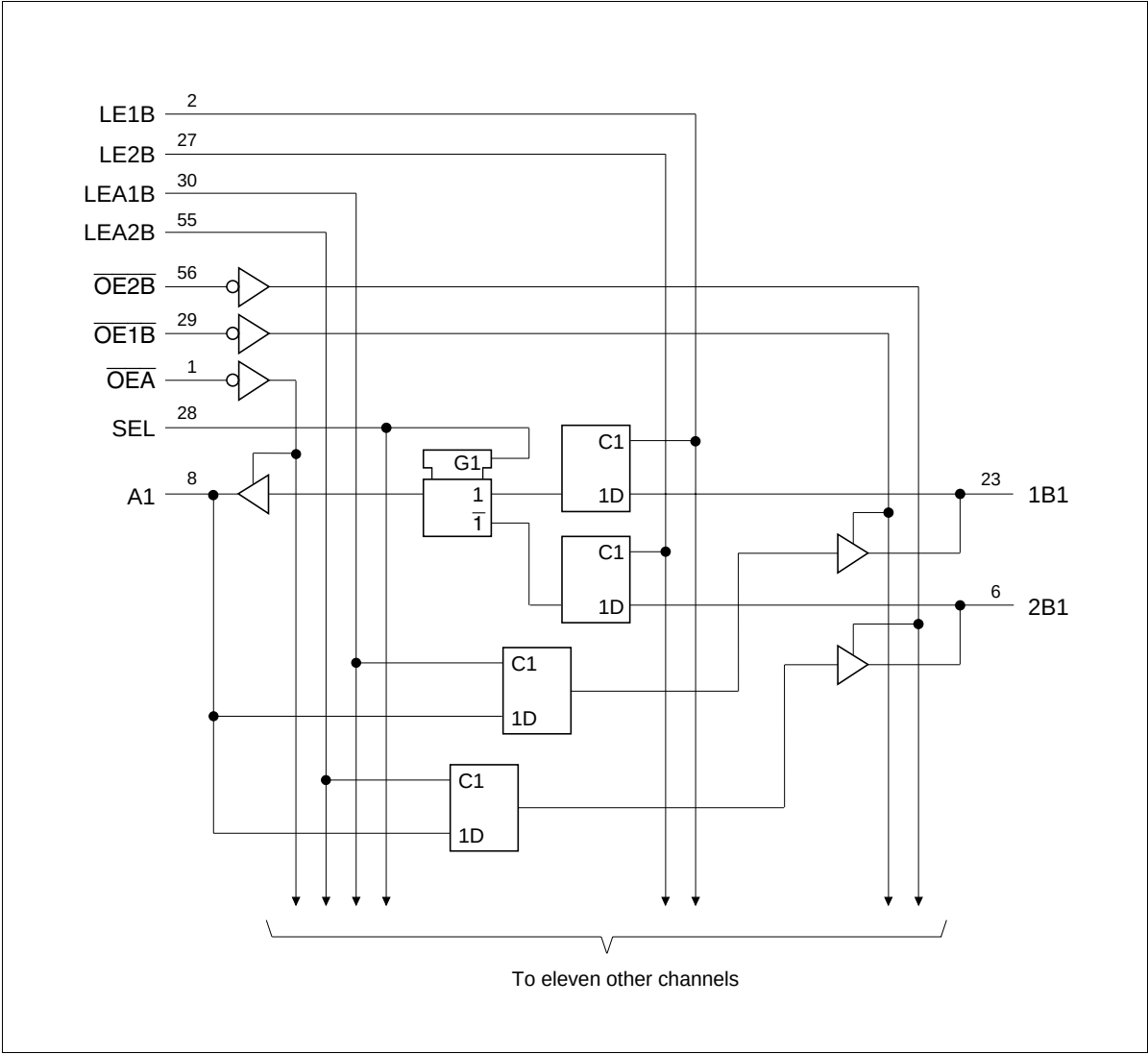
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	−12	mA	$V_{CC} = 2.3\text{ V}$
		—	−12		$V_{CC} = 2.7\text{ V}$
		—	−24		$V_{CC} = 3.0\text{ V}$
Low level output current	I_{OL}	—	12	mA	$V_{CC} = 2.3\text{ V}$
		—	12		$V_{CC} = 2.7\text{ V}$
		—	24		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	T_a	−40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



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Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V) ^{*1}	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V _{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V _{OH}	Min to Max	V _{CC} -0.2	—	V	I _{OH} = -100 μA
		2.3	2.0	—		I _{OH} = -6 mA, V _{IH} = 1.7 V
		2.3	1.7	—		I _{OH} = -12 mA, V _{IH} = 1.7 V
		2.7	2.2	—		I _{OH} = -12 mA, V _{IH} = 2.0 V
		3.0	2.4	—		I _{OH} = -12 mA, V _{IH} = 2.0 V
		3.0	2.0	—		I _{OH} = -24 mA, V _{IH} = 2.0 V
	V _{OL}	Min to Max	—	0.2		I _{OL} = 100 μA
		2.3	—	0.4		I _{OL} = 6 mA, V _{IL} = 0.7 V
		2.3	—	0.7		I _{OL} = 12 mA, V _{IL} = 0.7 V
		2.7	—	0.4		I _{OL} = 12 mA, V _{IL} = 0.8 V
		3.0	—	0.55		I _{OL} = 24 mA, V _{IL} = 0.8 V
Input current	I _{IN}	3.6	—	±5	μA	V _{IN} = V _{CC} or GND
	I _{IN (hold)}	2.3	45	—		V _{IN} = 0.7 V
		2.3	-45	—		V _{IN} = 1.7 V
		3.0	75	—		V _{IN} = 0.8 V
		3.0	-75	—		V _{IN} = 2.0 V
		3.6	—	±500		V _{IN} = 0 to 3.6 V
Off state output current ^{*2} I _{OZ}		3.6	—	±10	μA	V _{OUT} = V _{CC} or GND
Quiescent supply current	I _{CC}	3.6	—	40	μA	V _{IN} = V _{CC} or GND
	ΔI _{CC}	3.0 to 3.6	—	750	μA	V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

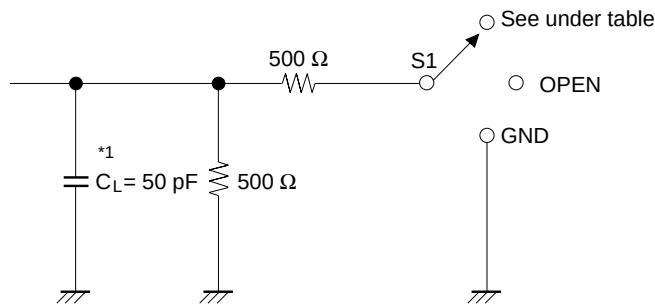
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics (Ta = −40 to 85°C)

Item	Symbol	V _{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t _{PLH}	2.5±0.2	1.2	—	5.6	ns	A or B	B or A
		2.7	—	—	5.1			
		3.3±0.3	1.2	—	4.3			
	t _{PHL}	2.5±0.2	1.0	—	6.2		$\overline{LE}$	A or B
		2.7	—	—	5.2			
		3.3±0.3	1.0	—	4.4			
		2.5±0.2	1.2	—	6.9		SEL	A
		2.7	—	—	6.6			
		3.3±0.3	1.1	—	5.6			
Output enable time	t _{ZH}	2.5±0.2	1.0	—	6.7	ns	$\overline{OE}$	A or B
		2.7	—	—	6.4			
		3.3±0.3	1.0	—	5.4			
Output disable time	t _{HZ}	2.5±0.2	1.7	—	5.7	ns	$\overline{OE}$	A or B
		2.7	—	—	5.0			
		3.3±0.3	1.3	—	4.6			
Setup time	t _{su}	2.5±0.2	1.4	—	—	ns		
		2.7	1.1	—	—			
		3.3±0.3	1.1	—	—			
Hold time	t _h	2.5±0.2	1.6	—	—	ns		
		2.7	1.9	—	—			
		3.3±0.3	1.5	—	—			
Pulse width	t _w	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C _{IN}	3.3	—	3.5	—	pF	Control inputs	
Output capacitance	C _{IN / O}	3.3	—	9.0	—	pF	A or B ports	

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• Test Circuit

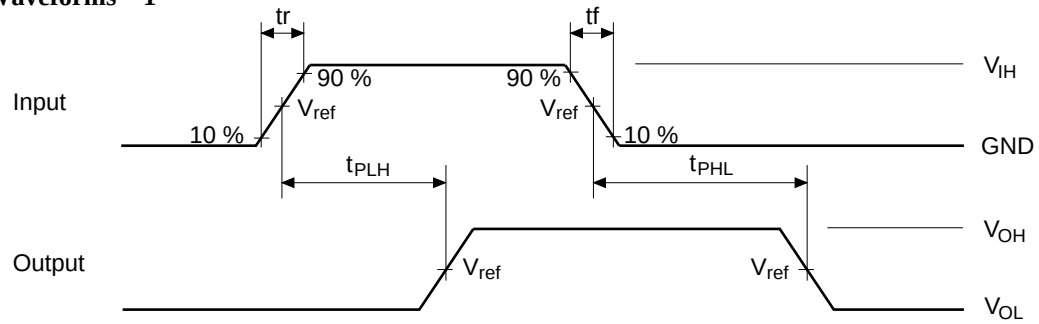


Load Circuit for Outputs

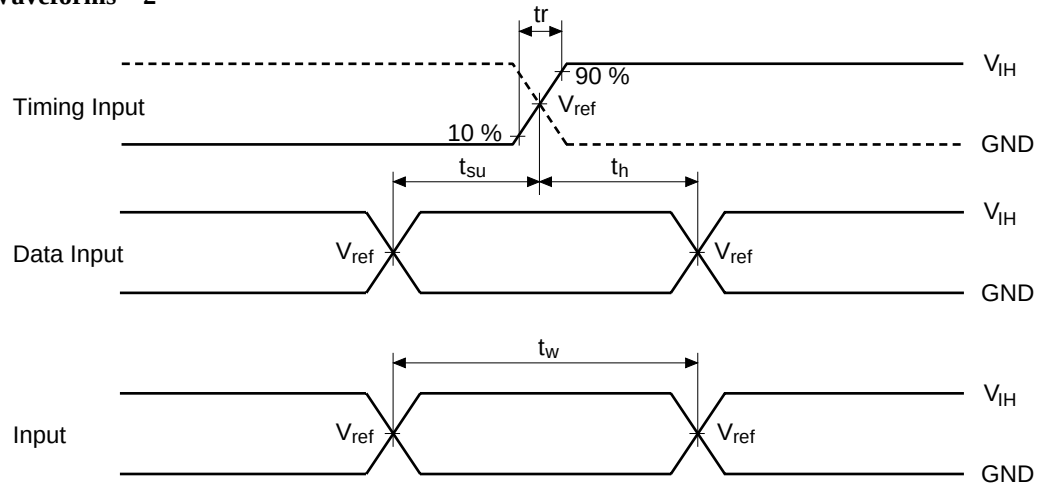
Symbol	$V_{CC}=2.5\pm0.2\text{V}$	$V_{CC}=2.7\text{V}, 3.3\pm0.3\text{V}$
t_{PLH}/t_{PHL}	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

• Waveforms – 1

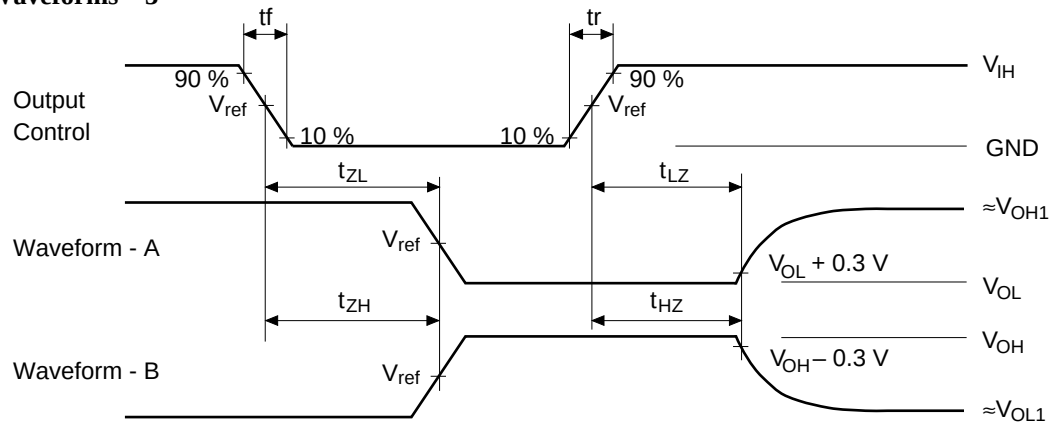


• Waveforms – 2



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• Waveforms – 3

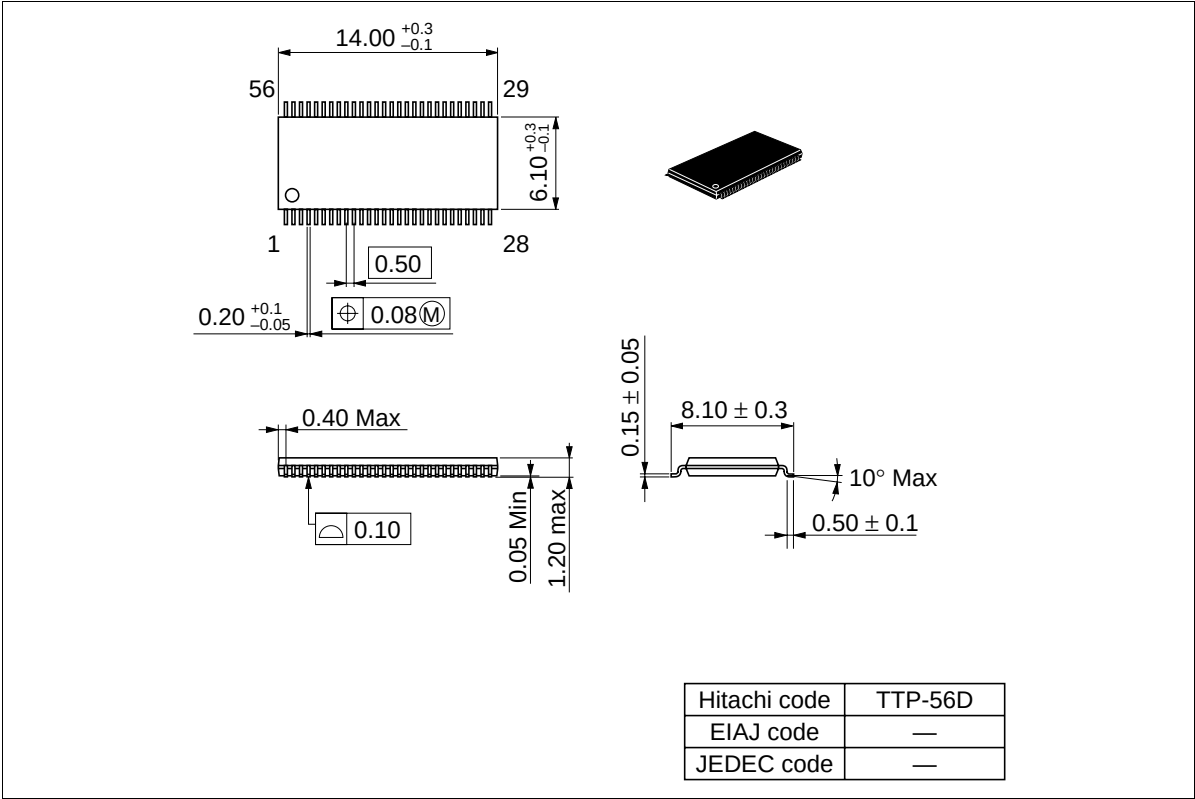


TEST	$V_{CC}=2.5\pm0.2V$	$V_{CC}=2.7V, 3.3\pm0.3V$
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



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