
HM628512B Series

4 M SRAM (512-kword $\times$ 8-bit)

HITACHI

ADE-203-903D (Z)

Rev. 3.0

Aug. 24, 1999

Description

The Hitachi HM628512B is a 4-Mbit static RAM organized 512-kword $\times$ 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 μ m Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512B is suitable for battery backup system.

Features

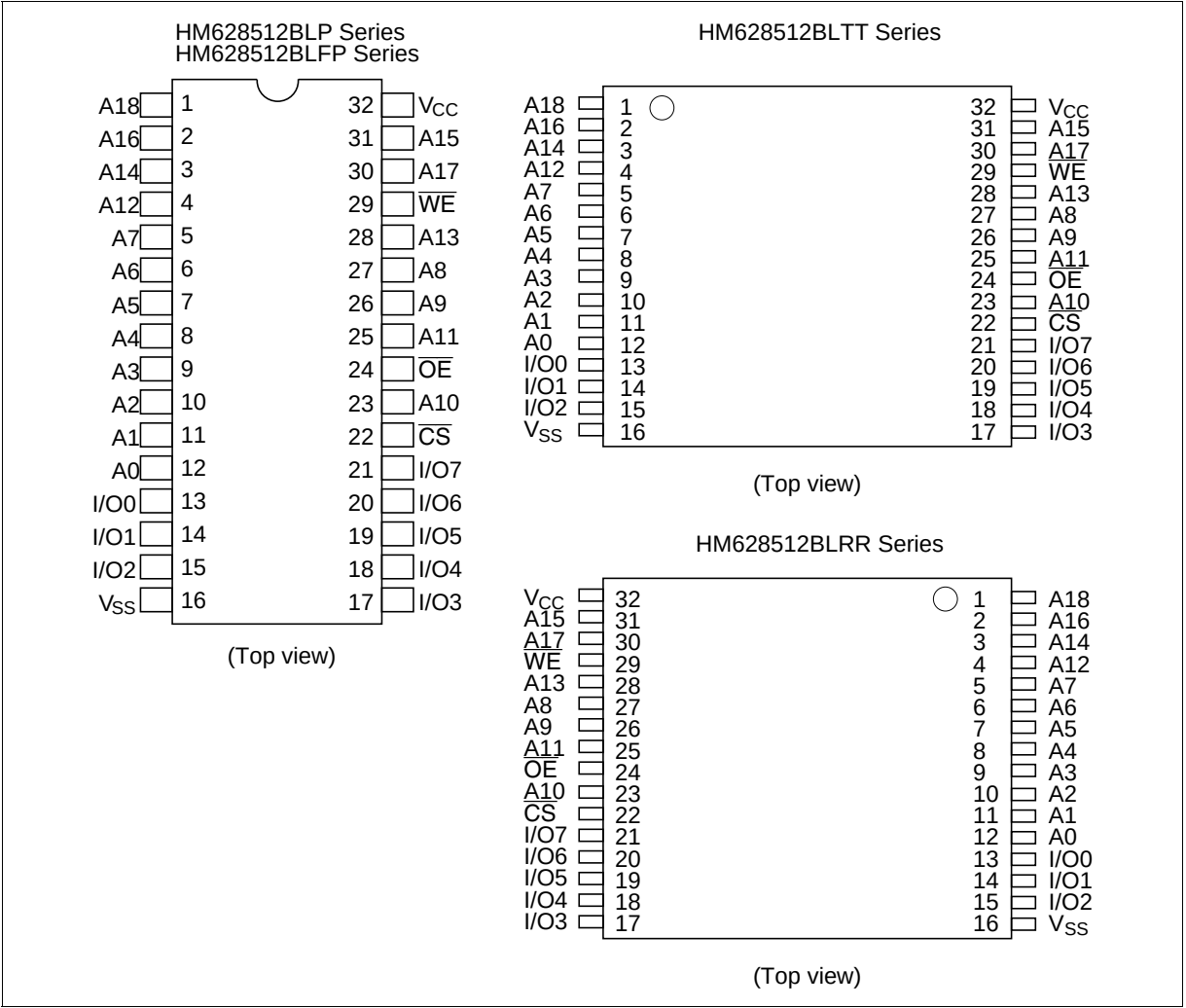
- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 50 mW/MHz (typ)
 - Standby: 10 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

HM628512B Series

Ordering Information

Type No.	Access time	Package
HM628512BLP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512BLP-7	70 ns	
HM628512BLP-5SL	55 ns	
HM628512BLP-7SL	70 ns	
HM628512BLP-5UL	55 ns	
HM628512BLP-7UL	70 ns	
HM628512BLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512BLFP-7	70 ns	
HM628512BLFP-5SL	55 ns	
HM628512BLFP-7SL	70 ns	
HM628512BLFP-5UL	55 ns	
HM628512BLFP-7UL	70 ns	
HM628512BLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512BLTT-7	70 ns	
HM628512BLTT-5SL	55 ns	
HM628512BLTT-7SL	70 ns	
HM628512BLTT-5UL	55 ns	
HM628512BLTT-7UL	70 ns	
HM628512BLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512BLRR-7	70 ns	
HM628512BLRR-5SL	55 ns	
HM628512BLRR-7SL	70 ns	
HM628512BLRR-5UL	55 ns	
HM628512BLRR-7UL	70 ns	

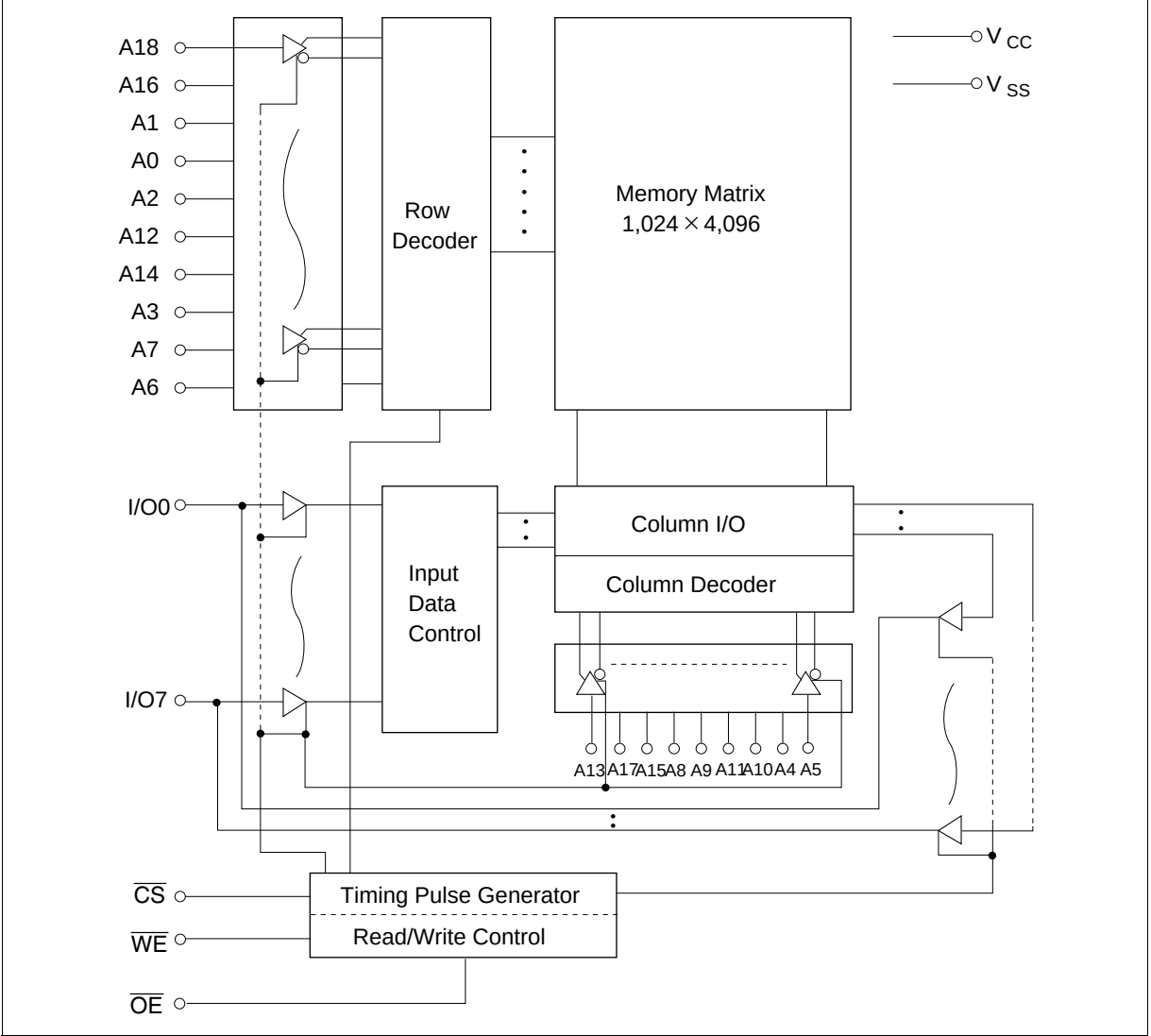
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	Mode	V_{CC} current	Dout pin	Ref. cycle
×	H	×	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_{T}	−0.5 ^{*1} to $V_{\text{CC}} + 0.3$ ^{*2}	V
Power dissipation	P_{T}	1.0	W
Operating temperature	T_{opr}	−20 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−20 to +85	°C

Notes: 1. −3.0 V for pulse half-width ≤ 30 ns

2. Maximum voltage is 7.0 V

Recommended DC Operating Conditions ($T_{\text{a}} = -20$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	$V_{\text{CC}} + 0.3$	V
Input low voltage	V_{IL}	−0.3 ^{*1}	—	0.8	V

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = -20 to +70°C, V_{CC} = 5 V ±10% , V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	—	8	15	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Operating power supply current	I _{CC1}	—	40	60	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{I/O} = 0 mA
Operating power supply current	I _{CC2}	—	10	20	mA	Cycle time = 1 μs, duty = 100% I _{I/O} = 0 mA, $\overline{CS} \leq 0.2$ V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I _{SB1}	—	2* ²	100* ²	μA	V _{in} ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	2* ³	50* ³	μA	
		—	2* ⁴	20* ⁴	μA	
		—	—	—	—	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

- Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L version.
3. This characteristics is guaranteed only for L-SL version.
4. This characteristics is guaranteed only for L-UL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	10	pF	V _{I/O} = 0 V

- Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -20$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (HM628512B-7)
1 TTL Gate + C_L (50 pF) (HM628512B-5)
(Including scope & jig)

Read Cycle

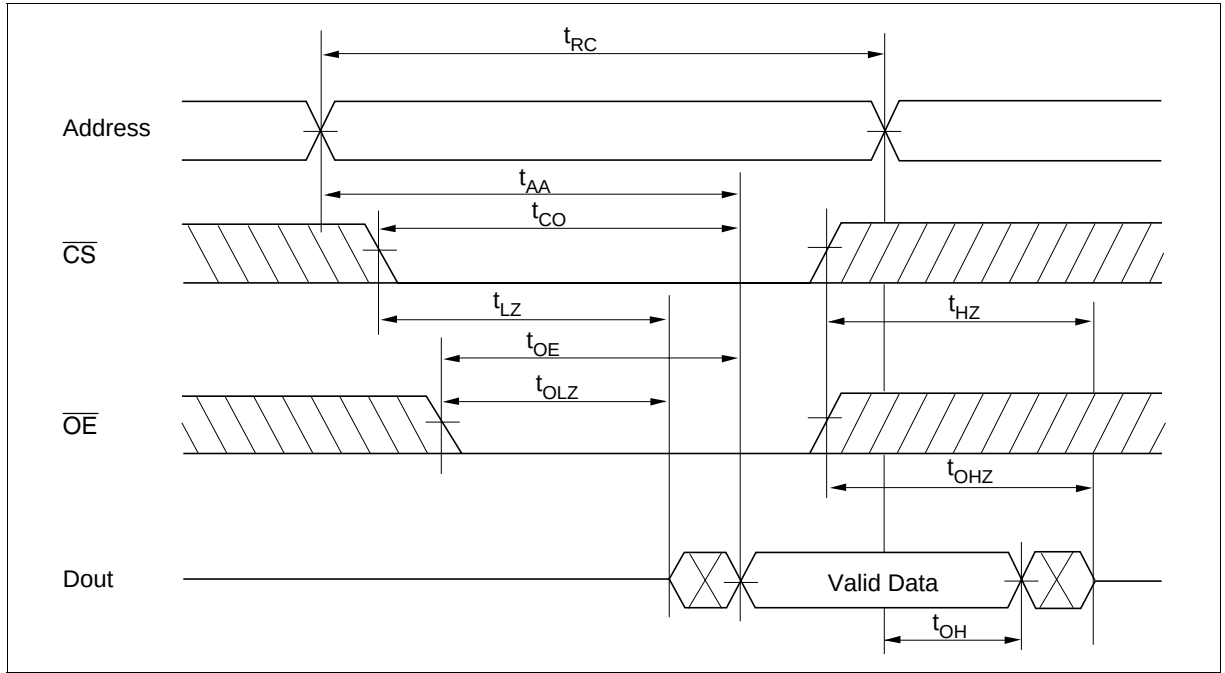
		HM628512B					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{CO}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	25	—	35	ns	
Chip selection to output in low-Z	t _{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	ns	

Write Cycle

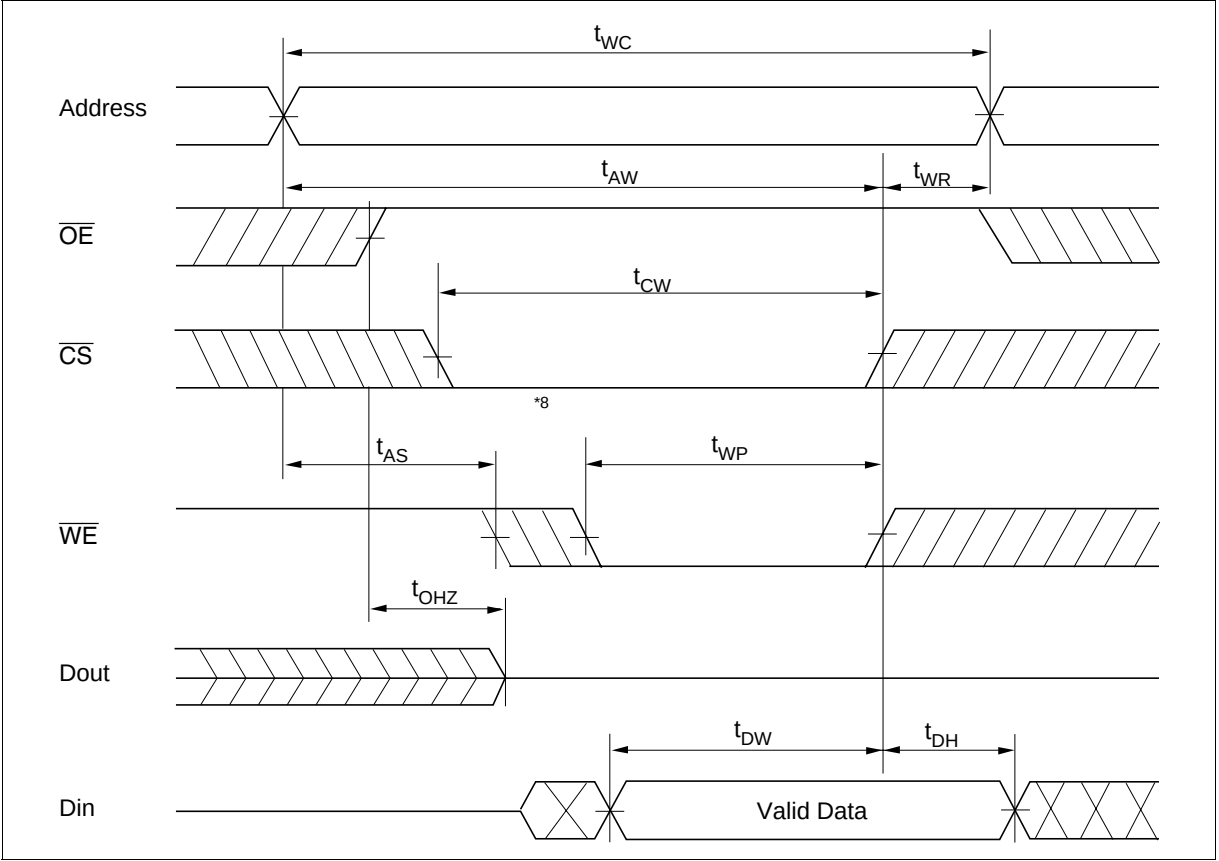
		HM628512B					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	70	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	ns	4
Address setup time	t _{AS}	0	—	0	—	ns	5
Address valid to end of write	t _{AW}	50	—	60	—	ns	
Write pulse width	t _{WP}	40	—	50	—	ns	3, 12
Write recovery time	t _{WR}	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	t _{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t _{DW}	25	—	30	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from output in high-Z	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 7

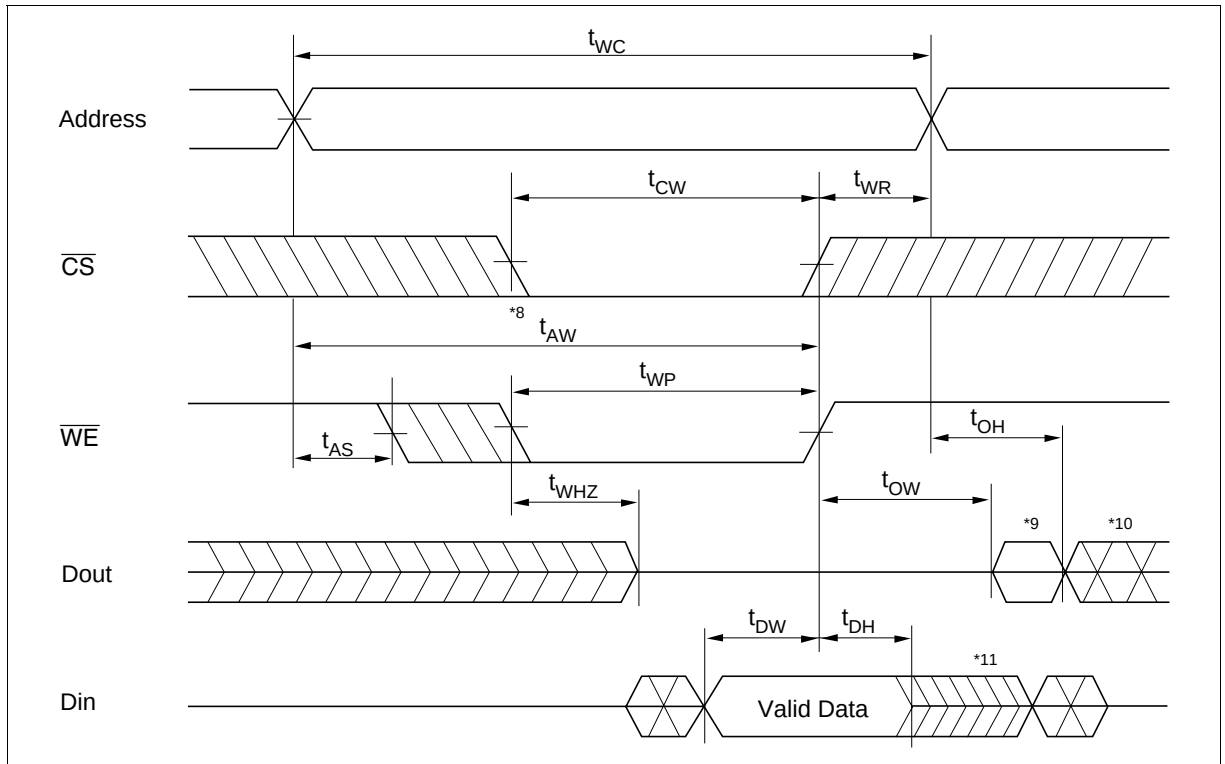
- Notes:
1. t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 4. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
 5. t_{AS} is measured from the address valid to the beginning of write.
 6. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
 7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 8. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
 9. Dout is the same phase of the write data of this write cycle.
 10. Dout is the read data of next address.
 11. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

Timing Waveforms

Read Timing Waveform ($\overline{WE} = V_{IH}$)

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



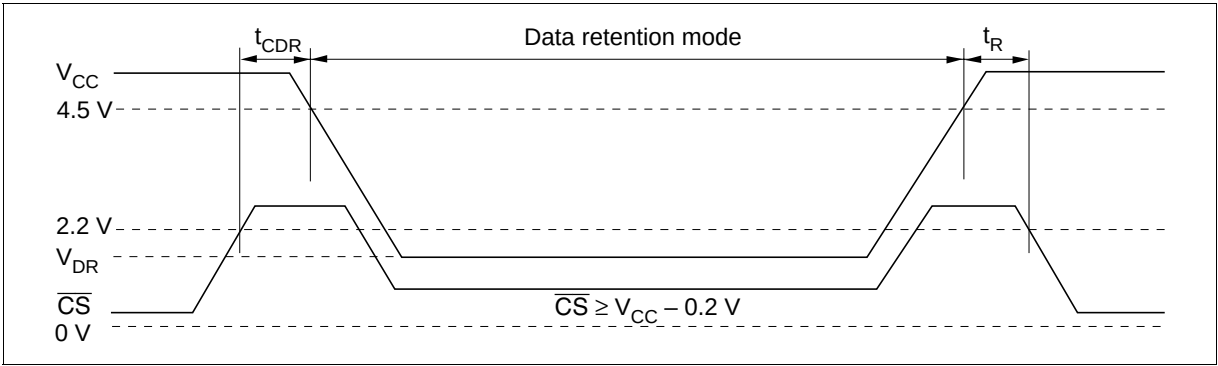
Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

Low V_{CC} Data Retention Characteristics (T_a = -20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions**
V _{CC} for data retention	V _{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, Vin ≥ 0 V
Data retention current	I _{CCDR}	—	1* ⁵	50* ¹	μA	$V_{CC} = 3.0\text{ V}$, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
		—	1* ⁵	15* ²	μA	
		—	1* ⁵	10* ³	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	t _{RC} * ⁶	—	—	ns	

- Notes:
- 1. For L-version and 20 μA (max.) at T_a = -20 to +40°C.
 - 2. For L-SL-version and 3 μA (max.) at T_a = -20 to +40°C.
 - 3. For L-UL-version and 3 μA (max.) at T_a = -20 to +40°C.
 - 4. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. In data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
 - 5. Typical values are at V_{CC} = 3.0 V, T_a = +25°C and specified loading, and not guaranteed.
 - 6. t_{RC} = read cycle time.

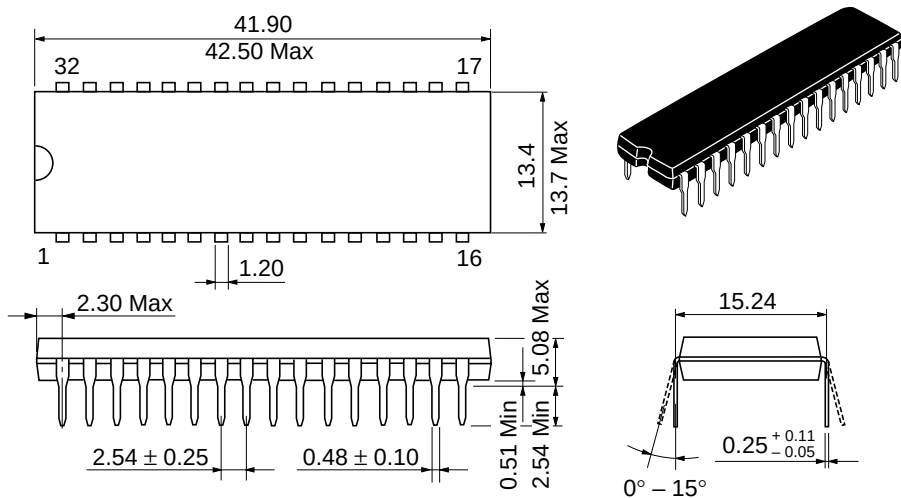
Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



Package Dimensions

HM628512BLP Series (DP-32)

Unit: mm

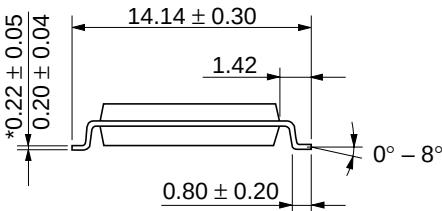
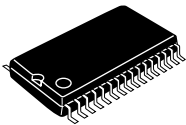
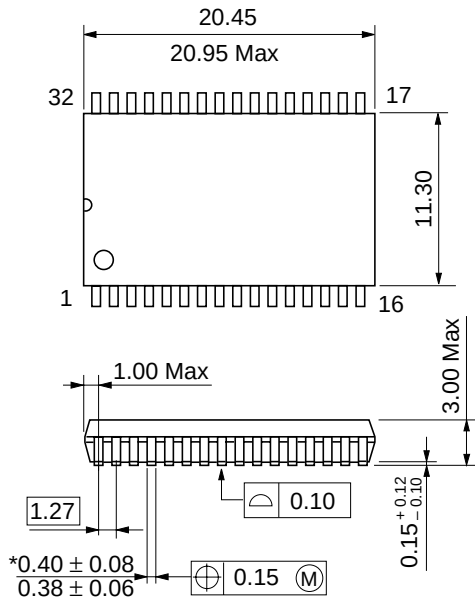


Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

Package Dimensions (cont.)

HM628512BLFP Series (FP-32D)

Unit: mm



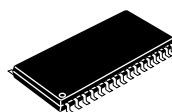
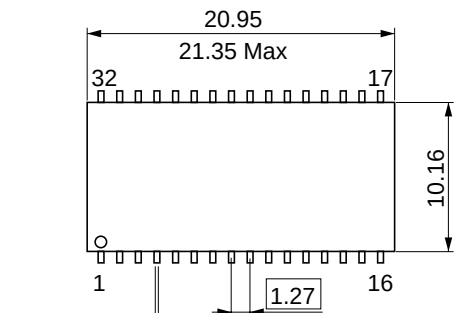
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

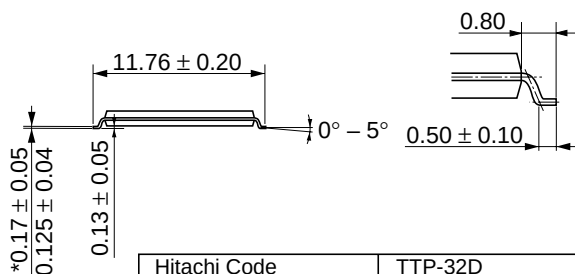
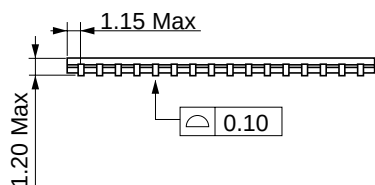
Package Dimensions (cont.)

HM628512BLTT Series (TTP-32D)

Unit: mm



* 0.42 ± 0.08
 0.40 ± 0.06



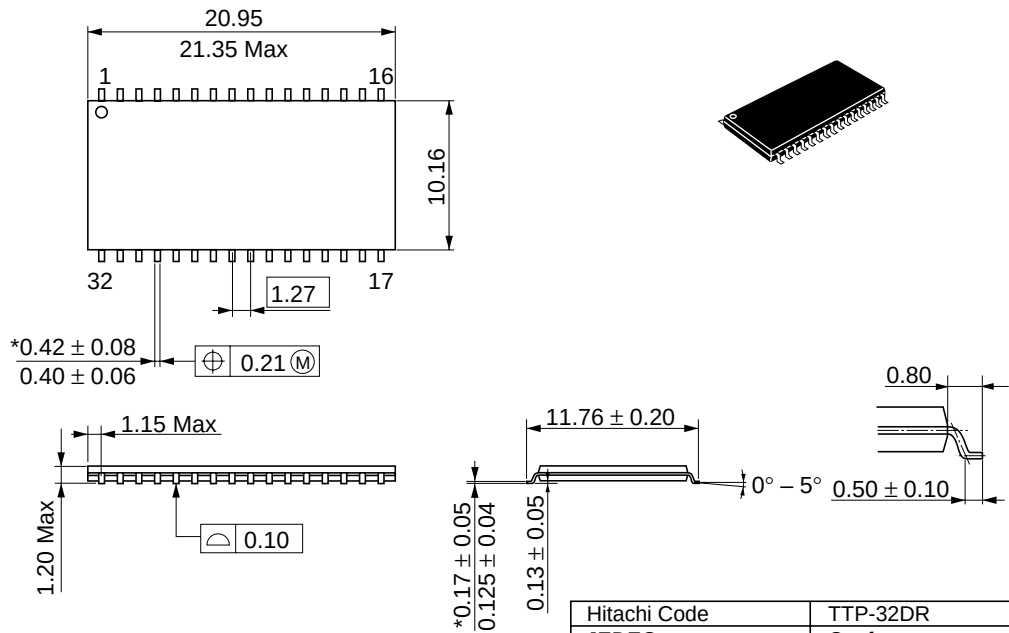
*Dimension including the plating thickness
 Base material dimension

Hitachi Code	TTP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

Package Dimensions (cont.)

HM628512BLRR Series (TTP-32DR)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
	Asia (Singapore)	:	http://www.has.hitachi.com.sg/grp3/sicd/index.htm
	Asia (Taiwan)	:	http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
	Asia (HongKong)	:	http://www.hitachi.com.hk/eng/bo/grp3/index.htm
	Japan	:	http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
---	---

Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533 Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building, No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180
--

Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX
--

Copyright © Hitachi, Ltd., 1998. All rights reserved. Printed in Japan.

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Apr. 24, 1998	Initial issue	M. Higuchi	K. Imato
0.1	Nov. 19, 1998	DC Characteristics I_{SB1} max: 40/20 μ A to 100/50 μ A Low V_{CC} Data Retention Characteristics I_{CCDR} max: 20/10 μ A to 50/15 μ A Change of note1 and 2	S. kunito	K. Imato
1.0	Jan. 13, 1999	Deletion of Preliminary Features Change of Power dissipation Standby: TBD (typ) to 10 μ W (typ) DC Characteristics I_{SB1} typ: TBD/TBD to 2/2 μ A Low V_{CC} Data Retention Characteristics I_{CCDR} typ: TBD/TBD to 1/1 μ A	S. kunito	K. Imato
2.0	Apr. 8, 1999	Addition of L-UL-version DC Characteristics I_{SB1} typ: 2/2 μ A to 2/2/2 μ A I_{SB1} max: 100/50 μ A to 100/50/20 μ A Addition of note4 Low V_{CC} Data Retention Characteristics I_{CCDR} typ: 1/1 μ A to 1/1/1 μ A I_{CCDR} max: 50/15 μ A to 50/15/10 μ A Addition of note3	S. kunito	K. Makuta
3.0	Aug. 24, 1999	Low V_{CC} Data Retention Characteristics Correct error: t_R unit ms to ns		