
HM62W16255HC Series

4M High Speed SRAM (256-kword $\times$ 16-bit)

HITACHI

ADE-203-1200 (Z)
Preliminary
Rev. 0.0
Sep. 1, 2000

Description

The HM62W16255HC is a 4-Mbit high speed static RAM organized 256-kword $\times$ 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM62W16255HC is packaged in 400-mil 44-pin SOJ and 400-mil 44-pin plastic TSOPII for high density surface mounting.

Features

- Single 3.3 V supply: 3.3 V $\pm$ 0.3 V
- Access time: 10 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current: 145 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
 - : 1 mA (max) (L-version)
- Data retention current: 0.6 mA (max) (L-version)
- Data retention voltage: 2.0 V (min) (L-version)
- Center V_{CC} and V_{SS} type pinout

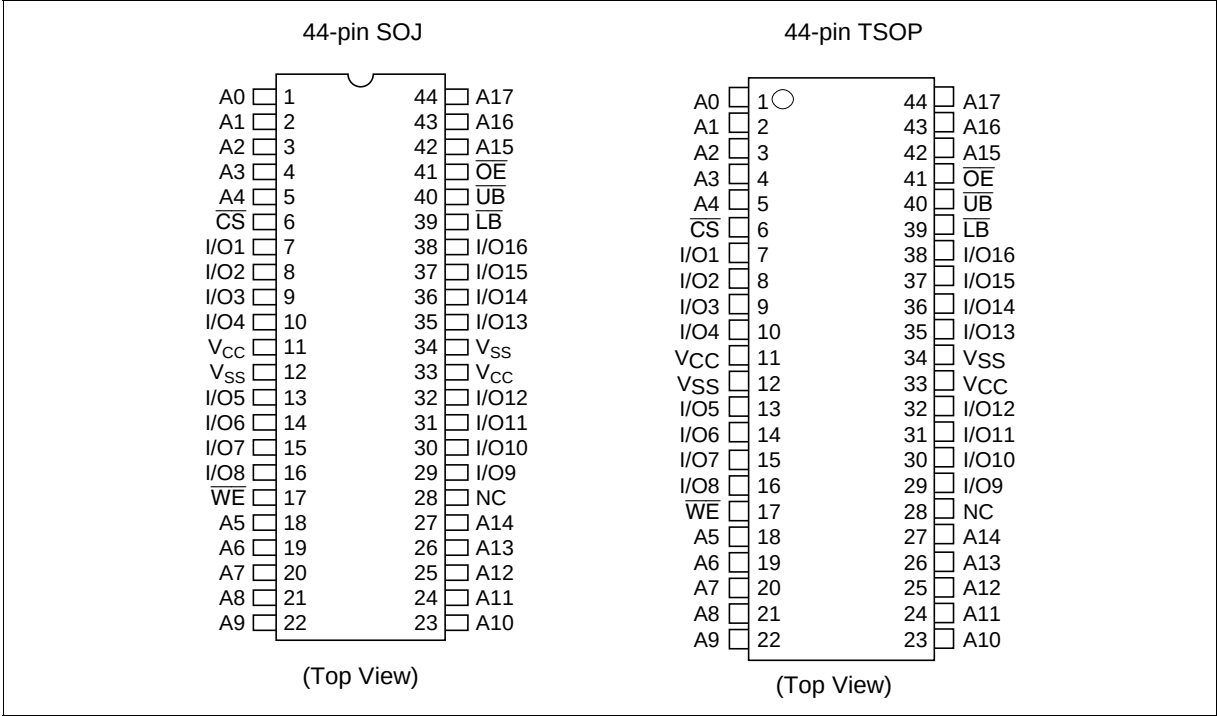
Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

HM62W16255HC Series

Ordering Information

Type No.	Access time	Package
HM62W16255HCJP-10	10 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM62W16255HCLJP-10	10 ns	
HM62W16255HCTT-10	10 ns	400-mil 44-pin plastic TSOPII (TTP-44DE)
HM62W16255HCLTT-10	10 ns	

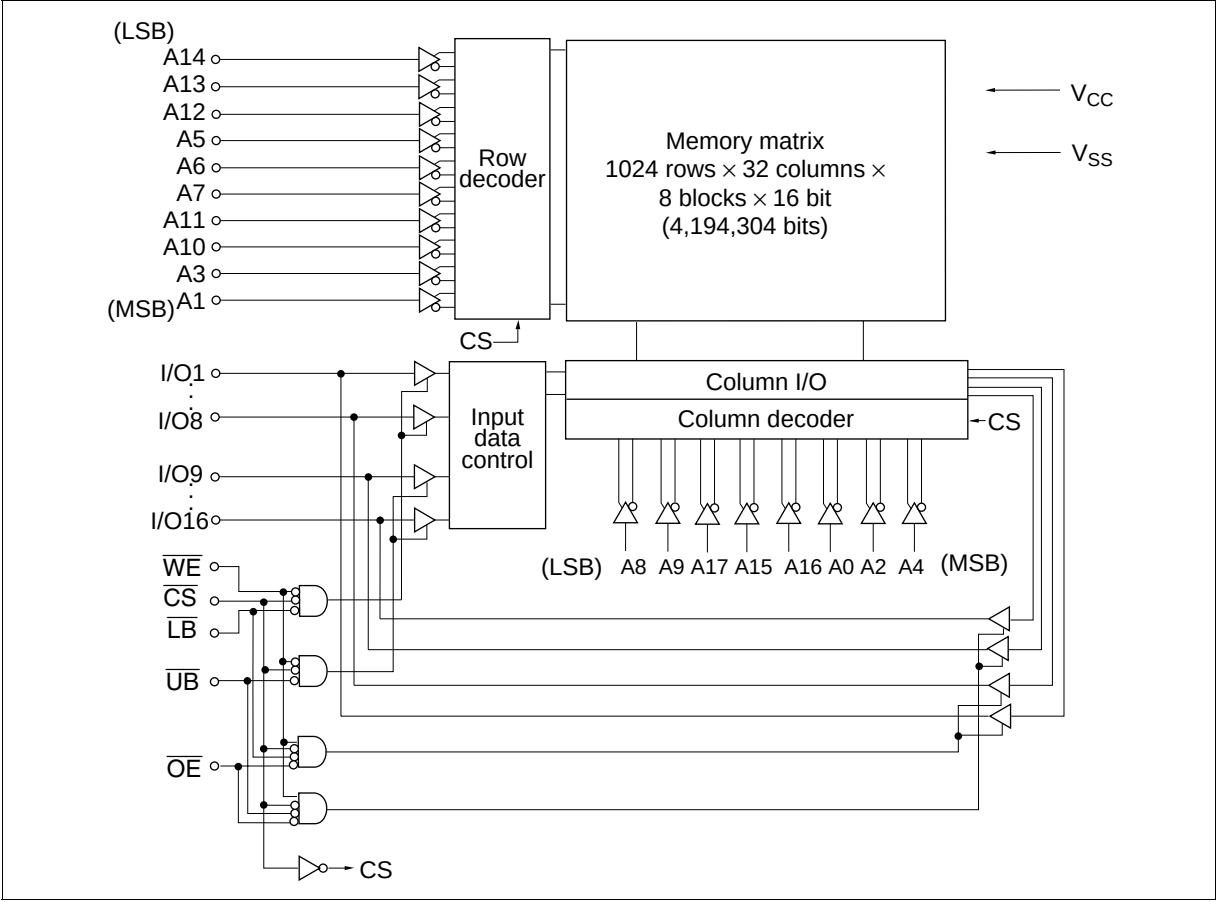
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
UB	Upper byte select
LB	Lower byte select
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	Mode	V_{CC} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	×	×	×	×	Standby	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	High-Z	—
L	H	H	×	×	Output disable	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	Read	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	—	I_{CC}	High-Z	High-Z	—
L	×	L	L	L	Write	I_{CC}	Input	Input	Write cycle
L	×	L	L	H	Lower byte write	I_{CC}	Input	High-Z	Write cycle
L	×	L	H	L	Upper byte write	I_{CC}	High-Z	Input	Write cycle
L	×	L	H	H	—	I_{CC}	High-Z	High-Z	—

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_{T}	−0.5* ¹ to V_{CC} + 0.5* ²	V
Power dissipation	P_{T}	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−10 to +85	°C

Notes: 1. V_{T} (min) = −2.0 V for pulse width (under shoot) ≤ 6 ns
2. V_{T} (max) = V_{CC} + 2.0 V for pulse width (over shoot) ≤ 6 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}^{*3}	3.0	3.3	3.6	V
	V_{SS}^{*4}	0	0	0	V
Input voltage	V_{IH}	2.0	—	$V_{CC} + 0.5^{*2}$	V
	V_{IL}	-0.5^{*1}	—	0.8	V

Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns
2. V_{IH} (max) = $V_{CC} + 2.0$ V for pulse width (over shoot) ≤ 6 ns
3. The supply voltage with all V_{CC} pins must be on the same level.
4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, $V_{CC} = 3.3$ V $\pm$ 0.3 V, $V_{SS} = 0$ V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	μ A	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2	μ A	$V_{in} = V_{SS}$ to V_{CC}
Operating power supply current	I_{CC}	—	—	145	mA	Min cycle $\overline{CS} = V_{IL}$, $I_{out} = 0$ mA Other inputs = V_{IH}/V_{IL}
Standby power supply current	I_{SB}	—	—	40	mA	Min cycle, $\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL}
	I_{SB1}	—	TBD	5	mA	$f = 0$ MHz $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, (1) 0 V $\leq V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
		—* ²	TBD* ²	1.0* ²		
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8$ mA
	V_{OH}	2.4	—	—	V	$I_{OH} = -4$ mA

Notes: 1. Typical values are at $V_{CC} = 3.3$ V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = +25°C, f = 1.0 MHz)

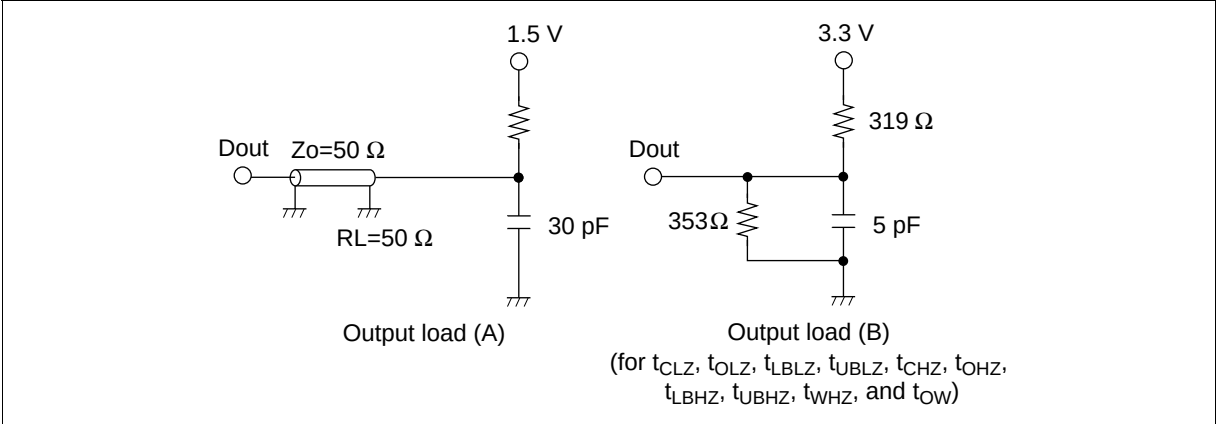
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance*1	C _{I/O}	—	—	8	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, VCC = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

		HM62W16255HC			
		-10			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	10	—	ns	
Address access time	t _{AA}	—	10	ns	
Chip select access time	t _{ACS}	—	10	ns	
Output enable to output valid	t _{OE}	—	5	ns	
Byte select to output valid	t _{LB} , t _{UB}	—	5	ns	
Output hold from address change	t _{OH}	3	—	ns	
Chip select to output in low-Z	t _{CLZ}	3	—	ns	1
Output enable to output in low-Z	t _{OLZ}	0	—	ns	1
Byte select to output in low-Z	t _{LBLZ} , t _{UBLZ}	0	—	ns	1
Chip deselect to output in high-Z	t _{CHZ}	—	5	ns	1
Output disable to output in high-Z	t _{OHZ}	—	5	ns	1
Byte deselect to output in high-Z	t _{LBHZ} , t _{UBHZ}	—	5	ns	1

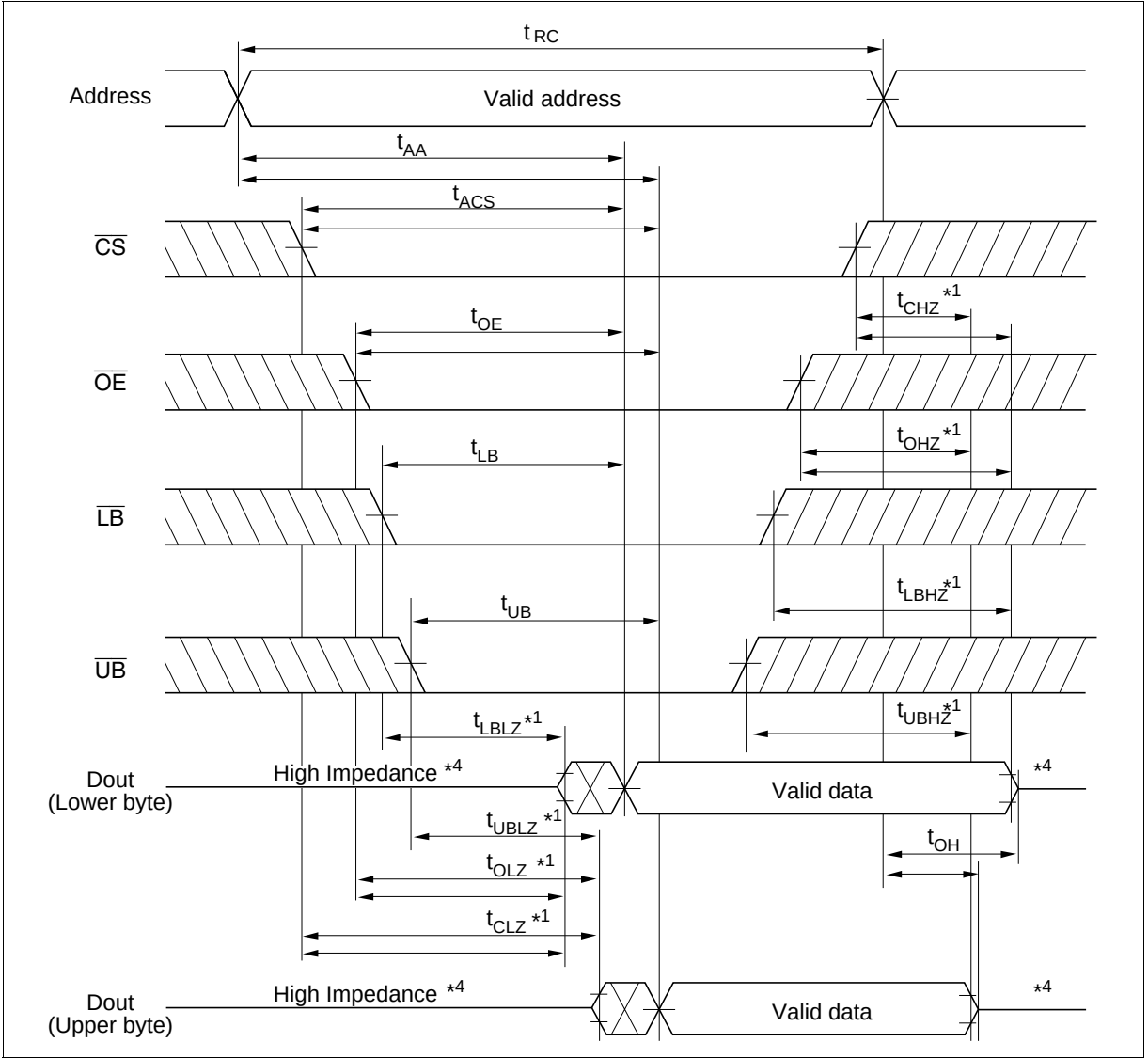
Write Cycle

		HM62W16255HC			
		-10			
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	10	—	ns	
Address valid to end of write	t _{AW}	7	—	ns	
Chip select to end of write	t _{CW}	7	—	ns	8
Write pulse width	t _{WP}	7	—	ns	7
Byte select to end of write	t _{LBW} , t _{UBW}	7	—	ns	9, 10
Address setup time	t _{AS}	0	—	ns	5
Write recovery time	t _{WR}	0	—	ns	6
Data to write time overlap	t _{DW}	5	—	ns	
Data hold from write time	t _{DH}	0	—	ns	
Write disable to output in low-Z	t _{OW}	3	—	ns	1
Output disable to output in high-Z	t _{OHZ}	—	5	ns	1
Write enable to output in high-Z	t _{WHZ}	—	5	ns	1

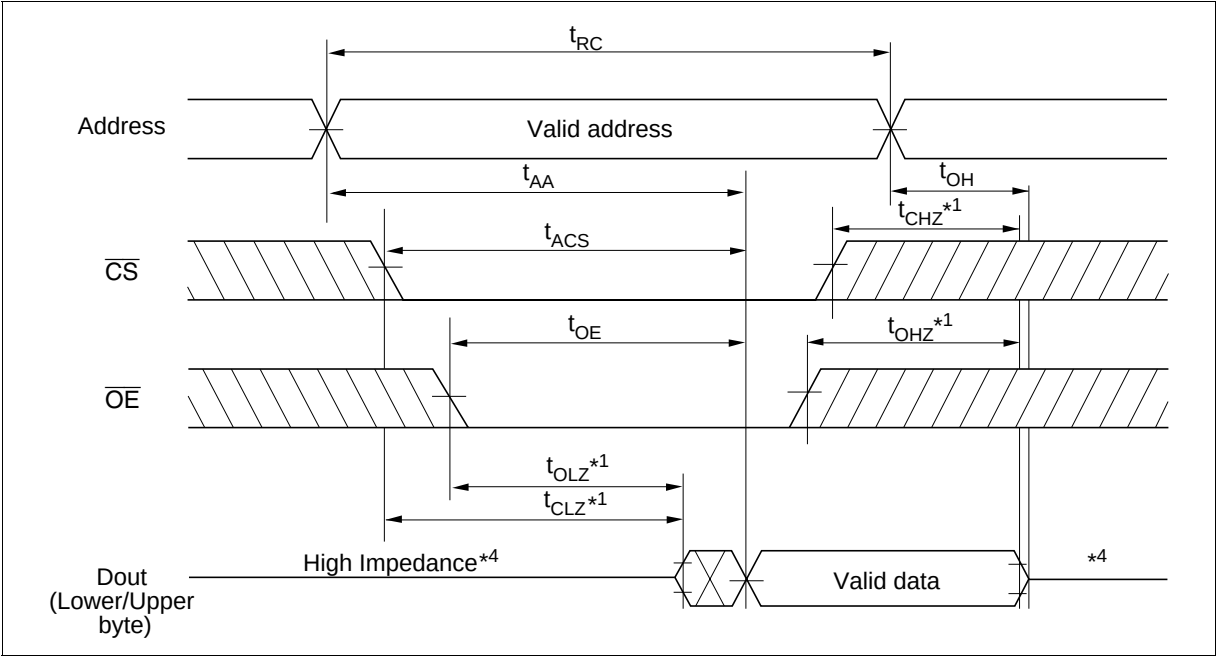
- Notes:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
 3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
 4. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 5. t_{AS} is measured from the latest address transition to the latest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going low.
 6. t_{WR} is measured from the earliest of $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ going high to the first address transition.
 7. A write occurs during the overlap of low $\overline{CS}$, low $\overline{WE}$ and low $\overline{LB}$ or low $\overline{UB}$.
 8. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.
 9. t_{LBW} is measured from the later of $\overline{LB}$ going low to the end of write.
 10. t_{UBW} is measured from the later of $\overline{UB}$ going low to the end of write.

Timing Waveforms

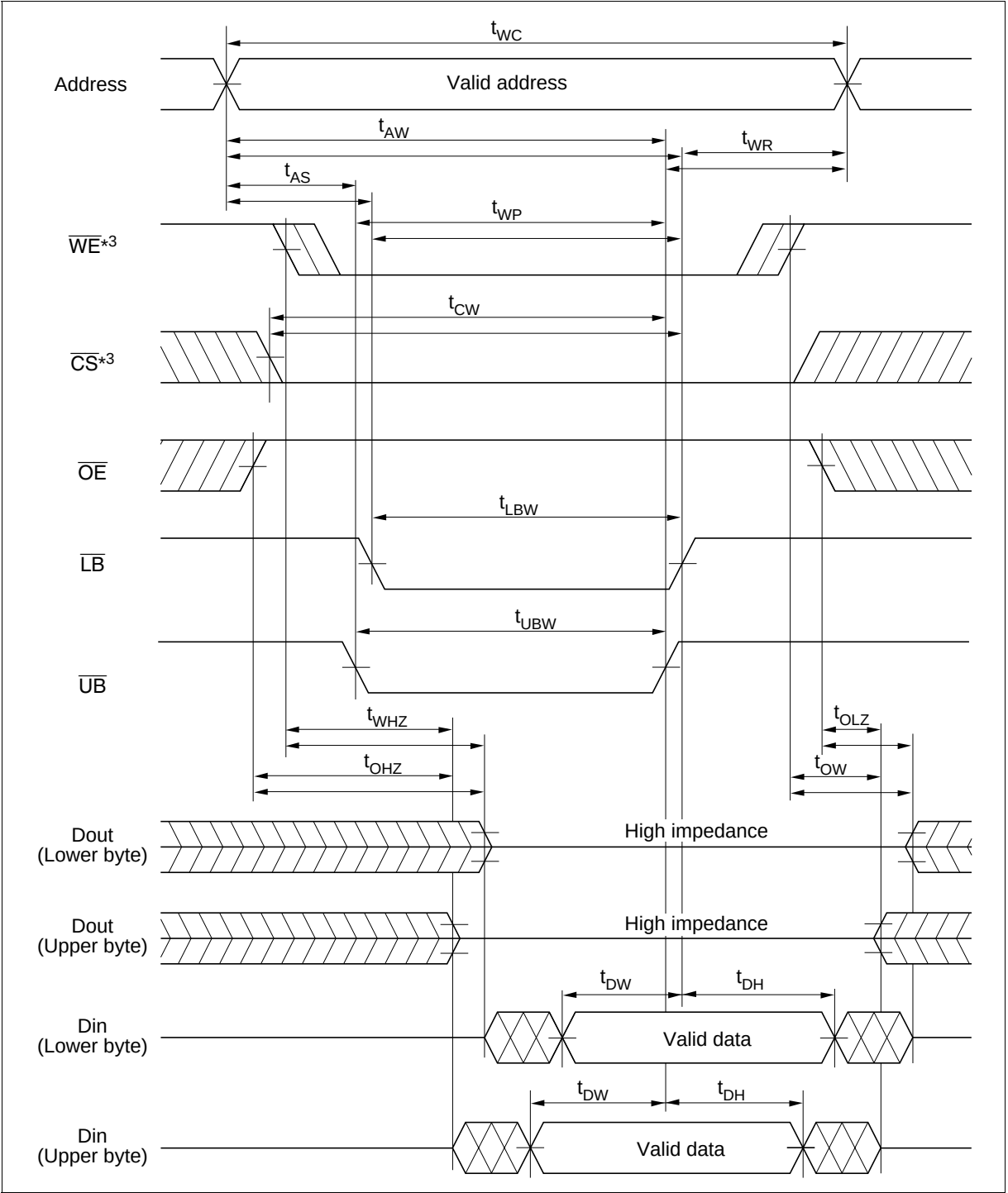
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



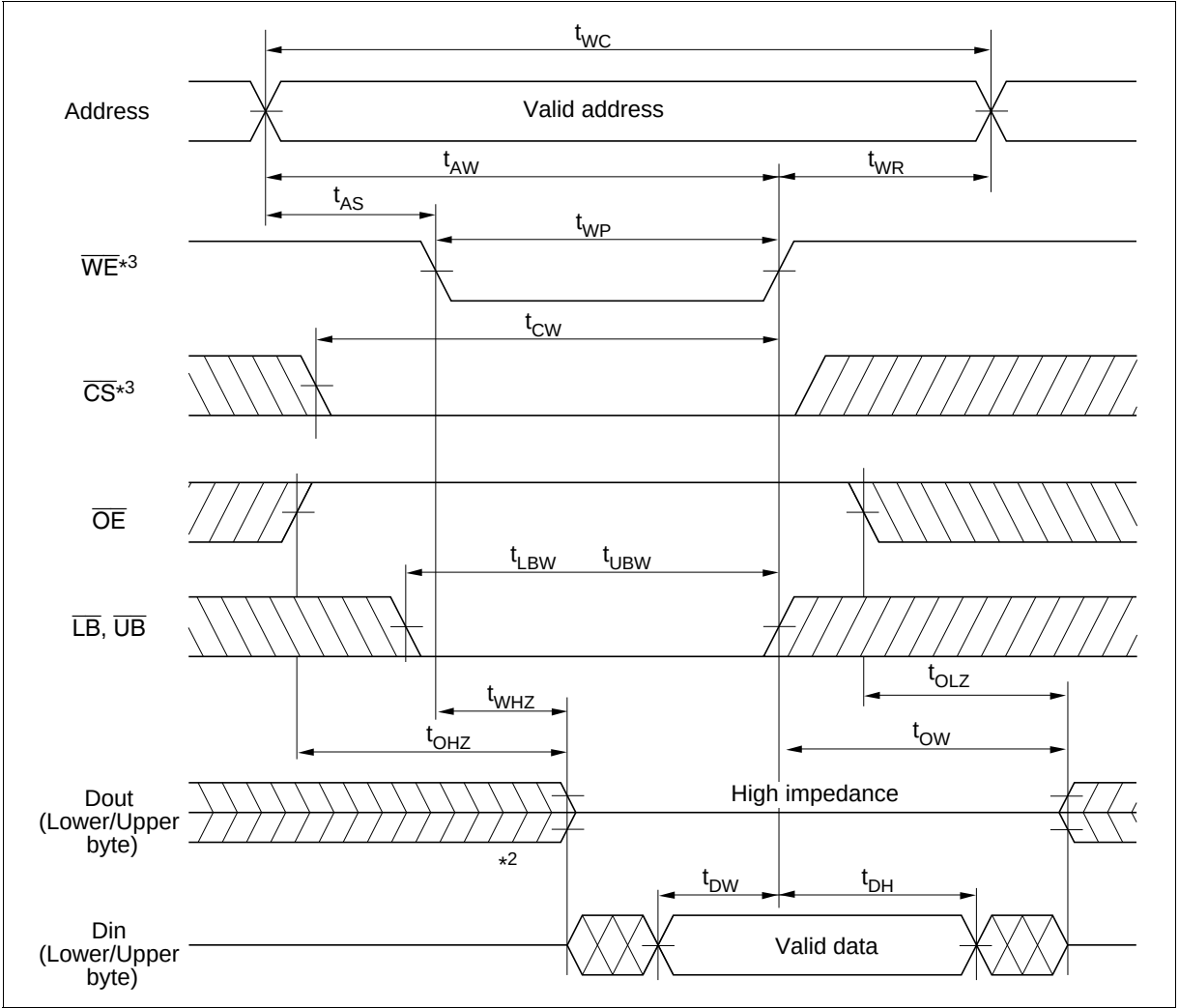
Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{LB} = V_{IL}$, $\overline{UB}_0 = V_{IL}$)



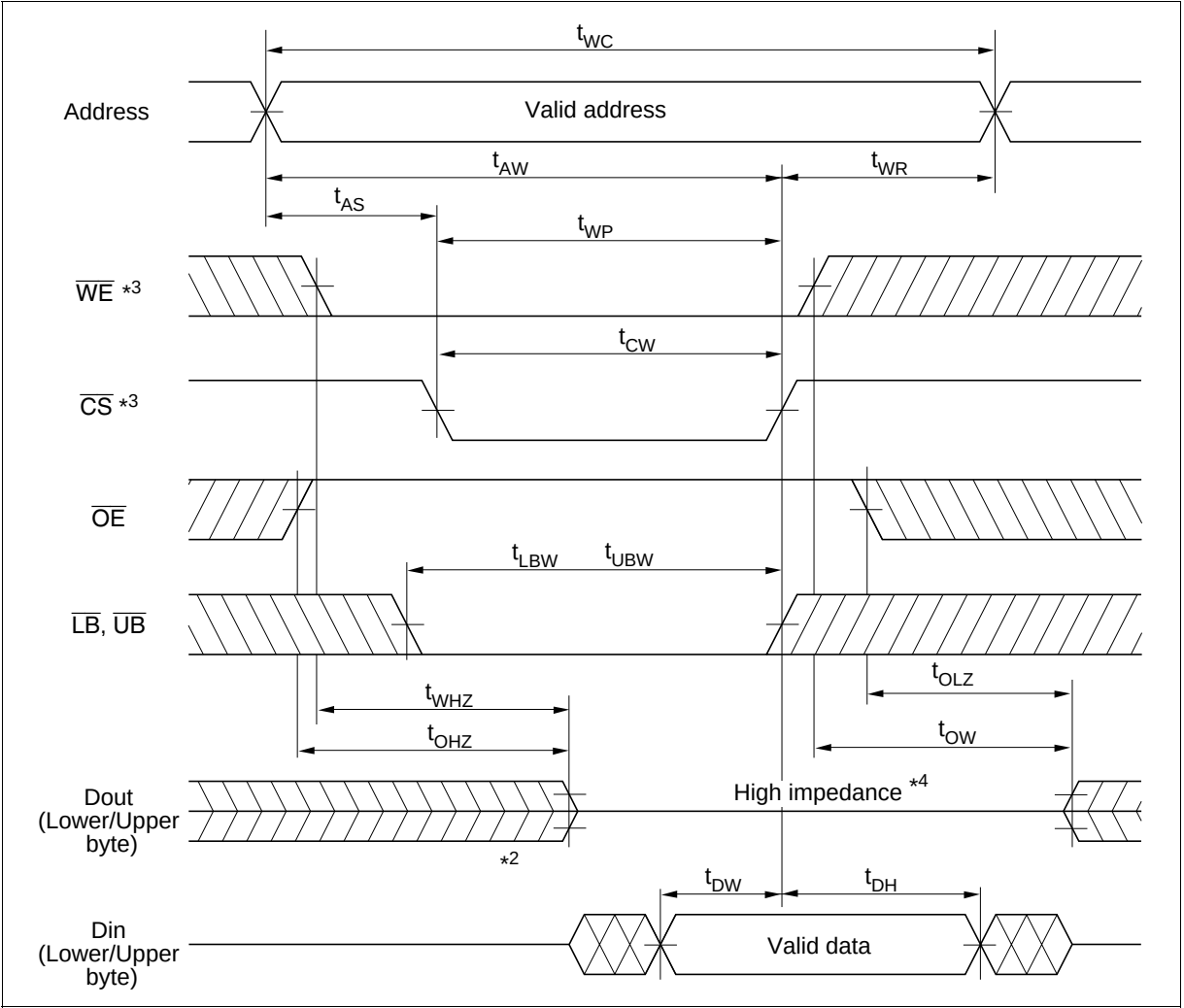
Write Timing Waveform (1) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled)



Write Timing Waveform (2) ($\overline{\text{WE}}$ Controlled)



Write Timing Waveform (3) ($\overline{\text{CS}}$ Controlled)



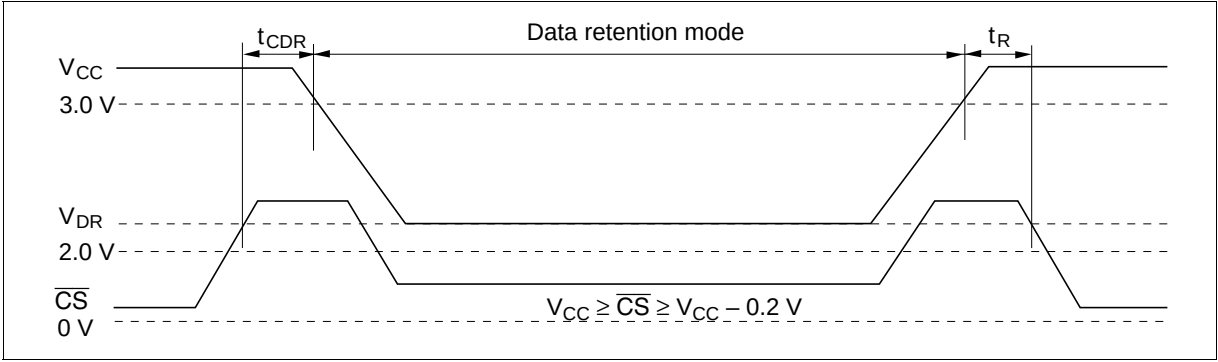
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
V _{CC} for data retention	V _{DR}	2.0	—	—	V	V _{CC} ≥ $\overline{CS}$ ≥ V _{CC} − 0.2 V, (1) 0 V ≤ Vin ≤ 0.2 V or (2) V _{CC} ≥ Vin ≥ V _{CC} − 0.2 V
Data retention current	I _{CDDR}	—	TBD	600	μA	V _{CC} = 3 V V _{CC} ≥ $\overline{CS}$ ≥ V _{CC} − 0.2 V, (1) 0 V ≤ Vin ≤ 0.2 V or (2) V _{CC} ≥ Vin ≥ V _{CC} − 0.2 V
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	5	—	—	ms	

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C, and not guaranteed.

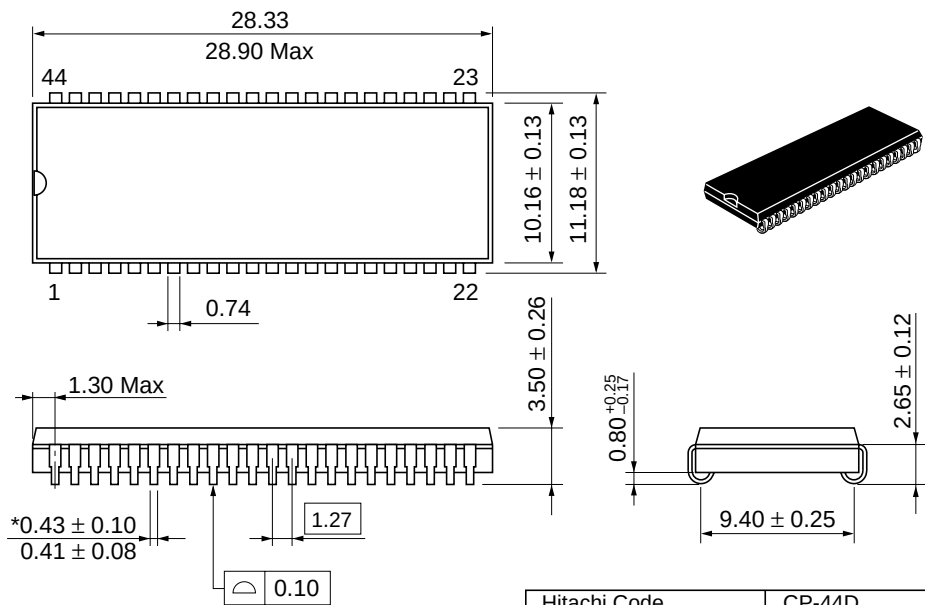
Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM62W16255HCJP/HCLJP Series (CP-44D)

Unit: mm

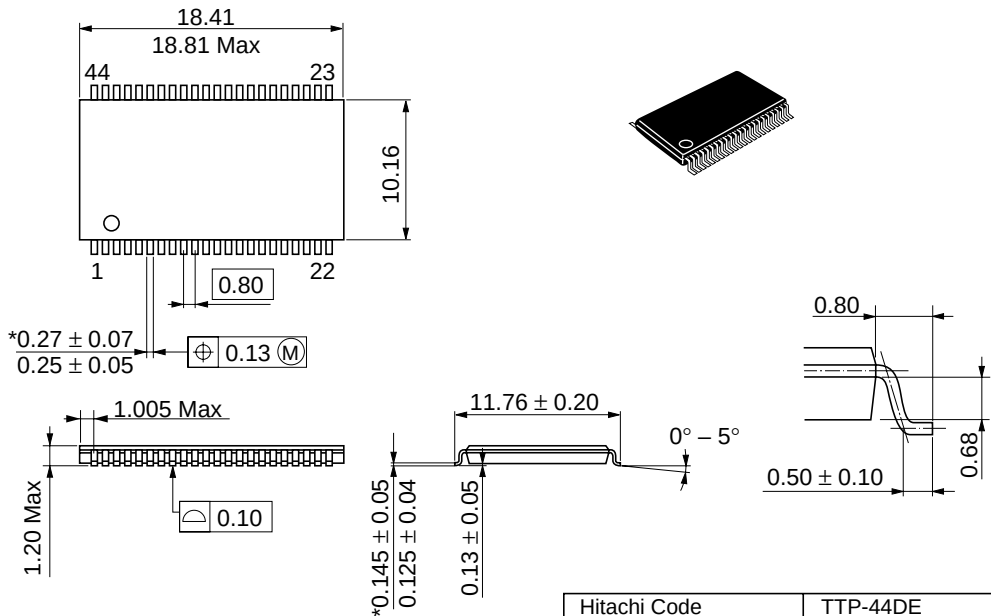


*Dimension including the plating thickness
Base material dimension

Hitachi Code	CP-44D
JEDEC	Conforms
EIAJ	—
Mass (reference value)	1.8 g

HM62W16255HCTT/HCLTT Series (TTP-44DE)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
EIAJ	—
Mass (reference value)	0.43 g

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic Components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00	Hitachi Asia Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533	Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7th Flr, North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX
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