

MB1510

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

DESCRIPTION

The Fujitsu MB1510 is a 1.1 GHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cellular telephone and cordless telephone applications.

The MB1510 has two PLL circuits on a single chip: PLL1 and PLL2. An analog switch is provided for each PLL circuit decrease lock up time. Separate power supply pins are provided for each PLL circuit as well.

1.1 GHz dual modulus prescalers are on chip and enables a pulse swallow function.

It operates from a supply voltage of 3.0V typ. and dissipates 15 mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

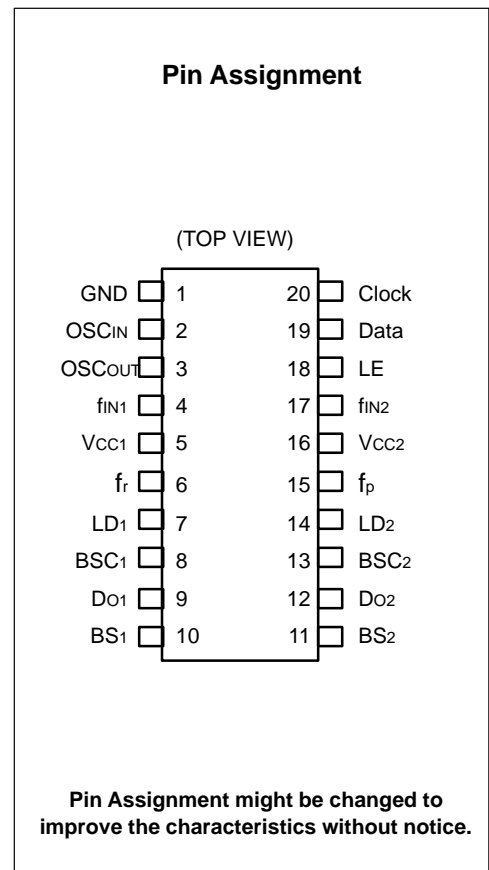
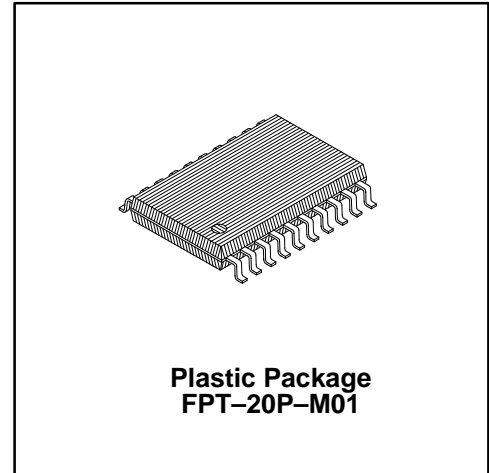
FEATURES

- High operating frequency: $f_{in} = 1.1 \text{ GHz}$ ($P_{in} = -10 \text{ dBm}$, $V_{CC} = 3V$)
- Pulse swallow function: 64/65 or 128/129
- Low power supply current: $I_{CC} = 15 \text{ mA typ. @} 3V$.
- Serial input reference divider: $R = 512$ or 1024
- Serial input 18-bit programmable divider consisting of:
 - Binary 7-bit swallow counter: 0 to 127
 - Binary 11-bit programmable counter: 16 to 2047
 - Tx and Rx programmable counters may be controlled separately.
- Low power supply voltage: $V_{CC} = 2.7$ to $5.5V$
- On-chip analog switches achieve fast lockup time
- Fast lock up by bipolar charge pumps
- Wide operating temperature: $T_A = -40$ to 85°C
- Plastic 20-pin fiat package (Suffix: -PF)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

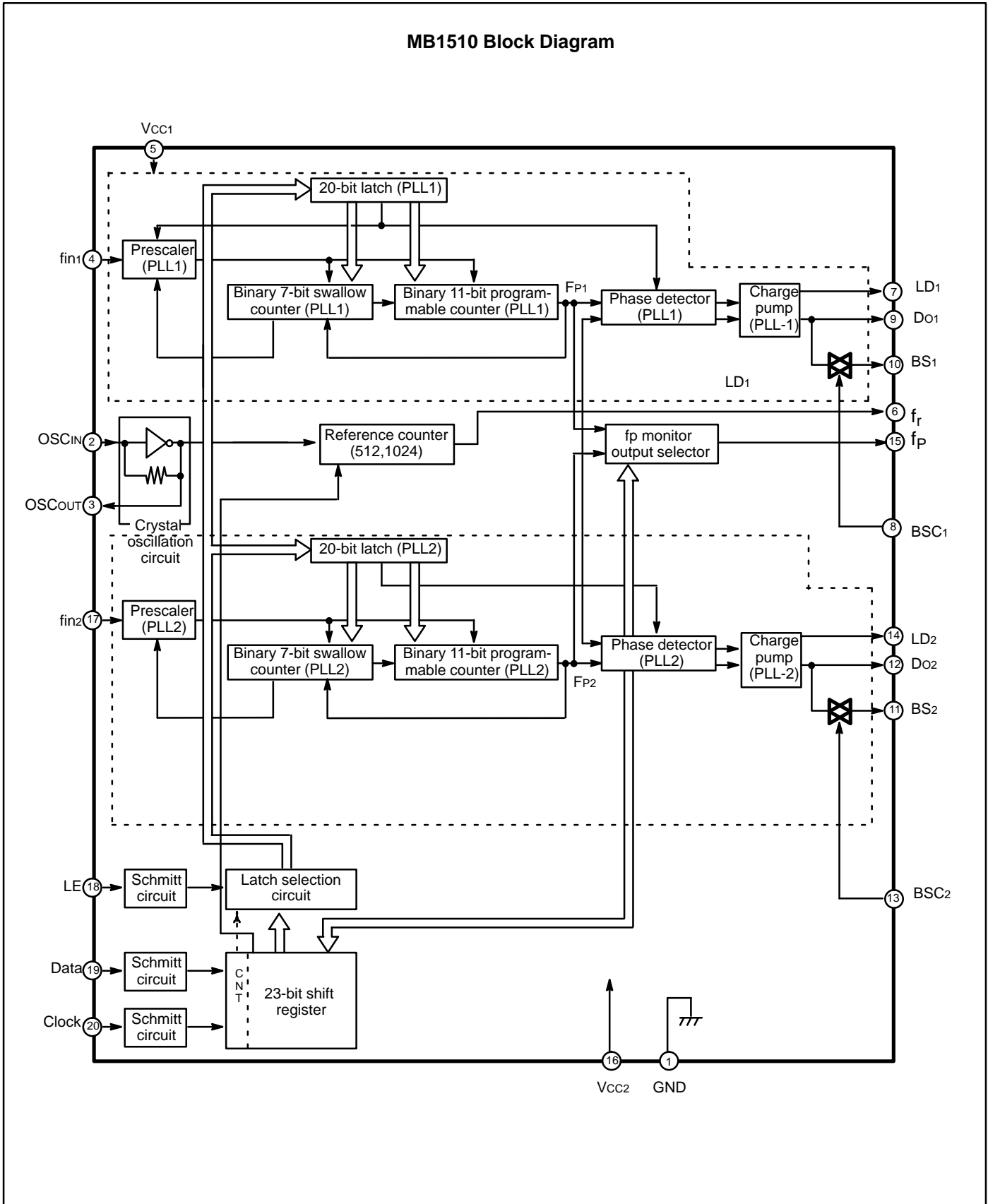
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Output Voltage	V_{OUT}	-0.5 to $V_{CC}+0.5$	V
Output Current	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	-55 to +125	$^\circ\text{C}$

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1510 Block Diagram



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions						
1	GND	—	Ground						
2 3	OSC _{IN} OSC _{OUT}	I O	Oscillator input pin Oscillator output pin A crystal is connected between OSC _{IN} pin and OSC _{OUT} pin.						
4	f _{in1}	I	Prescaler input pin of PLL1 section. The connection with VCO should be AC connection.						
5	V _{CC1}	—	Power supply voltage input pin of PLL1 section. When power is OFF, latched data of PLL1 section is cancelled.						
6	f _r	O	Monitor pin for programmable reference divider output						
7	LD1	O	Lock detect signal output pin of PLL1 section. <table border="1"> <thead> <tr> <th>Condition</th> <th>LD pin output level</th> </tr> </thead> <tbody> <tr> <td>Lock</td> <td>H</td> </tr> <tr> <td>Unlock</td> <td>L</td> </tr> </tbody> </table>	Condition	LD pin output level	Lock	H	Unlock	L
Condition	LD pin output level								
Lock	H								
Unlock	L								
8	BSC1	I	Analog switch control pin of PLL1 section. <table border="1"> <thead> <tr> <th>BSC1</th> <th>BS1 pin output</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>High-impedance</td> </tr> <tr> <td>H</td> <td>Charge pump output</td> </tr> </tbody> </table>	BSC1	BS1 pin output	L	High-impedance	H	Charge pump output
BSC1	BS1 pin output								
L	High-impedance								
H	Charge pump output								
9	Do1	O	Charge pump output pin of PLL1 section. Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.						
10	BS1	O	Analog switch output pin of PLL1 section, and controlled by BSC1.						
11	BS2	O	Analog switch output pin of PLL2 section, and controlled by BSC2.						
12	Do2	O	Charge pump output pin of PLL2 section. Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.						
13	BSC2	I	Analog switch control pin of PLL2 section. <table border="1"> <thead> <tr> <th>BSC2</th> <th>BS2 pin output</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>High-impedance</td> </tr> <tr> <td>H</td> <td>Charge pump output</td> </tr> </tbody> </table>	BSC2	BS2 pin output	L	High-impedance	H	Charge pump output
BSC2	BS2 pin output								
L	High-impedance								
H	Charge pump output								
14	LD2	O	Lock detect signal output pin of PLL2 section. <table border="1"> <thead> <tr> <th>Condition</th> <th>LD pin output level</th> </tr> </thead> <tbody> <tr> <td>Lock</td> <td>H</td> </tr> <tr> <td>Unlock</td> <td>L</td> </tr> </tbody> </table>	Condition	LD pin output level	Lock	H	Unlock	L
Condition	LD pin output level								
Lock	H								
Unlock	L								
15	f _p	O	Monitor pin for programmable divider output. This pin output divided frequency of PLL1 section or PLL2 section depending upon FP bit setting. <table border="1"> <thead> <tr> <th>Condition</th> <th>LD pin output level</th> </tr> </thead> <tbody> <tr> <td>Lock</td> <td>H</td> </tr> <tr> <td>Unlock</td> <td>L</td> </tr> </tbody> </table>	Condition	LD pin output level	Lock	H	Unlock	L
Condition	LD pin output level								
Lock	H								
Unlock	L								

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions						
16	V _{CC2}	—	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.						
17	f _{in2}	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC connection.						
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog switch becomes ON.						
19	Data	I	Serial data input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either PLL1 section or PLL2 section depending upon a control data. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Control bit data</th> <th>The destination of data</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Latch of PLL1 section</td> </tr> <tr> <td>L</td> <td>Latch of PLL2 section</td> </tr> </tbody> </table>	Control bit data	The destination of data	H	Latch of PLL1 section	L	Latch of PLL2 section
Control bit data	The destination of data								
H	Latch of PLL1 section								
L	Latch of PLL2 section								
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift register.						

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$$f_{VCO} = \{(M \times N) + A\} \times f_{osc} \div R \quad (A < N)$$

- f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
- M: Preset divide ratio of dual modulus prescaler (64 or 128)
- N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7-bit swallow counter (0 ≤ A ≤ 127)
- f_{osc}: Reference oscillation frequency
- R: Preset divide ratio of reference counter (512 or 1024)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

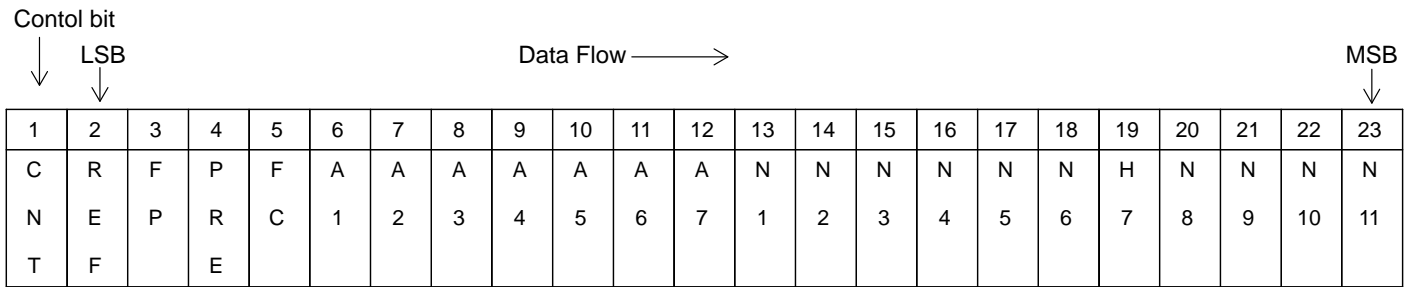
Serial data is input using three pins, Data pin, Clock pin, and LE pin. Programmable divider of PLL1 section and programmable divider of PLL2 section are controlled individually.

Serial data of binary data is input into Data pin.

On rising edge of clock shifts one bit of serial data into the shift register. When load enable signal is high, the data stored in the shift register is transferred to either the latch of PLL1 section or the latch of PLL2 section depending upon the control bit data setting.

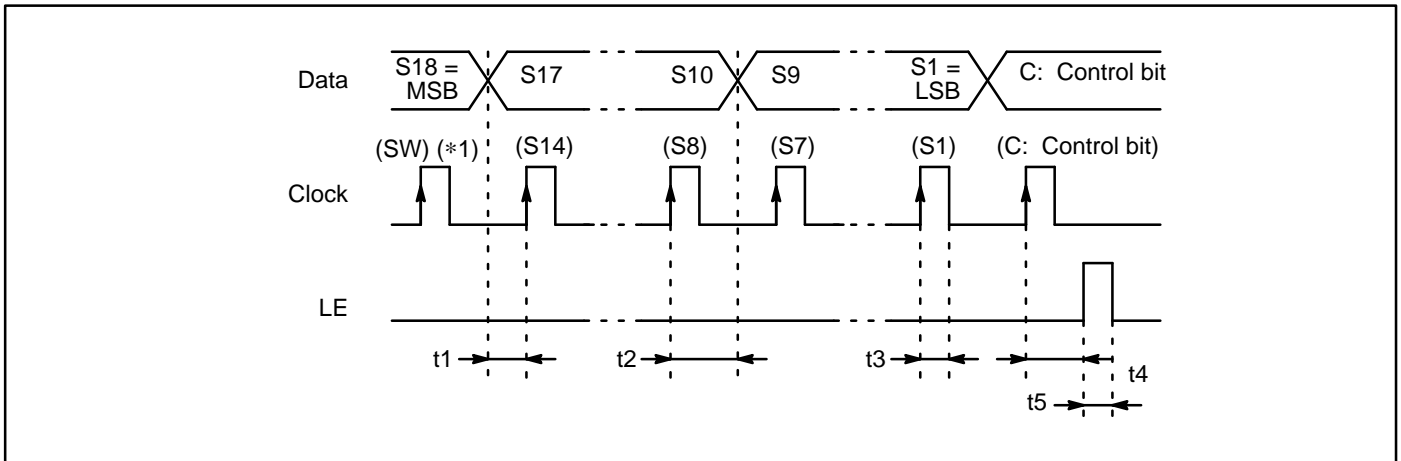
Control data	Destination of serial data
H	Latch of PLL1 section
L	Latch of PLL2 section

SHIFT REGISTER CONFIGURATION



- N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
- A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
- FC : Phase control bit of the phase detector
- PRE : Divide ratio of the prescaler setting bit (64/65,128/129)
- FP : Output of the programmable divider control bit (fp1 or fp2)
- REF : Divide ratio of the reference counter setting bit (512 to 1024)
- CHT : Control bit

SERIAL DATA INPUT TIMING



On rising edge of the dock shifts one bit of the data into the shift register.

MB1510

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited.
Divide ratio (H) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

PRE : DIVIDE RATIO (P) OF THE PRESCALER SETTING BIT
H = 64/65
L = 128/129

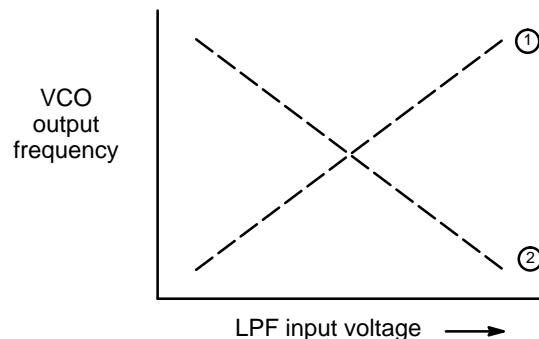
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = S12 (fr = 25.0 kHz)
L = 1024 (fr = 12.5 kHz)

FP: OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of PLL1 section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of PLL2 section

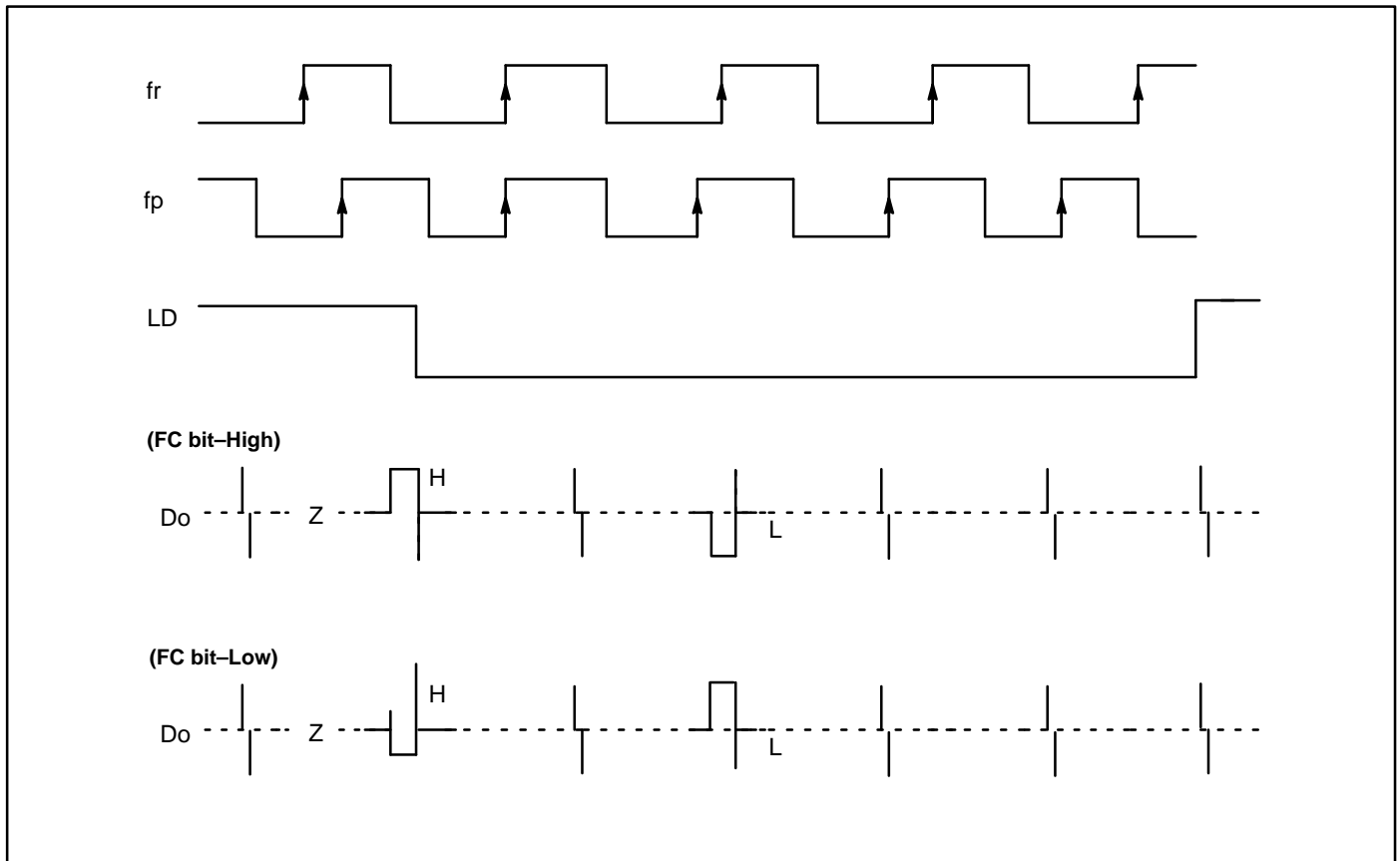
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	\downarrow	\uparrow

Note: Z = High-impedance
Depending upon the VCO polarity,
FC should be bit set.



PHASE DETECTOR OUTPUT WAVEFORM



Note: Phase difference detection range = $\leq 2\pi$ to $+2\pi$
 LD output becomes low when phase difference is tW or more.
 LD output becomes high when phase difference less than tW is repeated 3 times or more.
 (e. g. $tW = 625$ to 1250ns , $f_{\text{oscin}} = 12.8\text{ MHz}$)
 Spike appearance depends on the charge pump characteristics. The spike is output to diminish the dead band.
 When $f_r > f_p$ or $f_r < f_p$, spike might not generate depending on the charge pump characteristics.

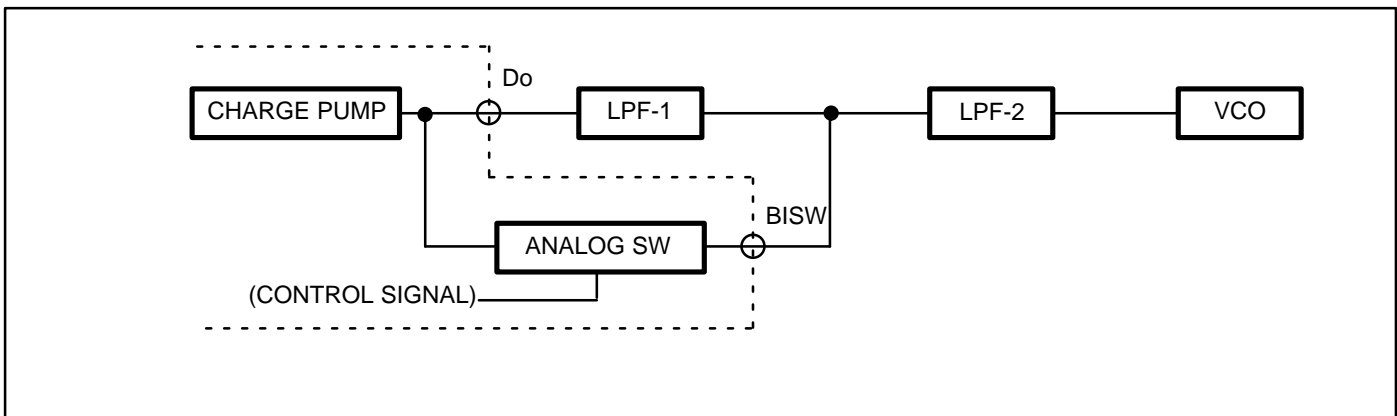
MB1510

ANALOG SWITCH

ON/OFF of the analog switch is controlled by BSC input signal. BSC1 controls the analog switch of the PLL1 circuit, BSC2 controls the analog switch of PLL2. When the analog switch is ON, BS pin output the charge pump output (D01, D02). When analog switch is OFF, BS pin is set to high-impedance.

	BCS1 (2)	
	H	L
Analog switch of PLL1 (2) section	ON	OFF
BS1 (2) output	Charge pump output Do1 (2)	High-impedance

When an analog switch is inserted between LPF-1 and LPF-2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
Input Voltage	V_{IN}	GND	—	V_{CC}	V	
Operating Temperature	T_A	-40	—	+85	°C	

HANDLING PRECAUTIONS

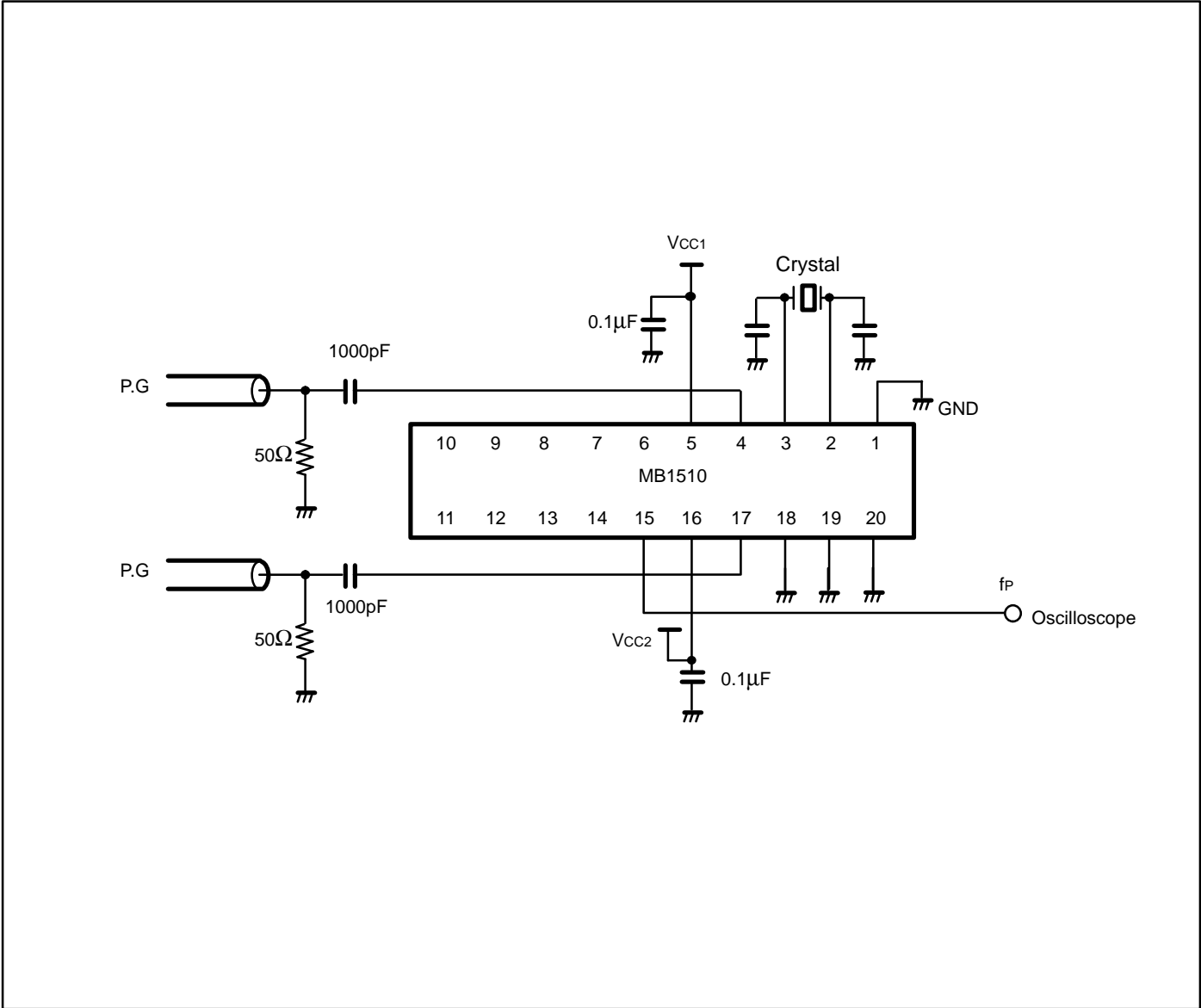
- This device should be transported and stored in anti-static containers.
- This is a static sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded.
- Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket
- Protects leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

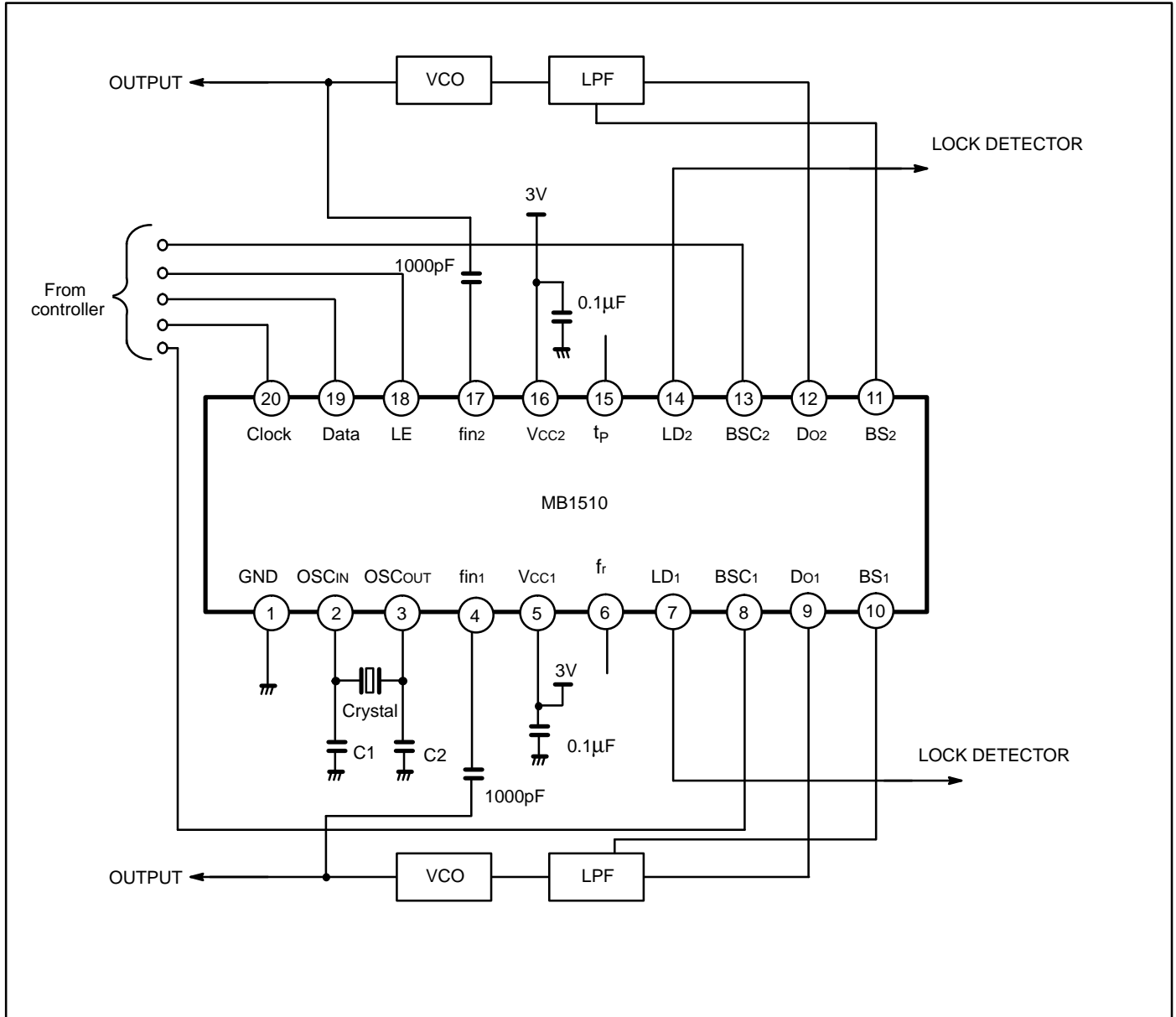
Parameter		Symbol	Condition	Value			Unit
Power Supply Current		I_{CC1}	PLL2 current	—	8.0	—	mA
		I_{CC2}	(PLL1 + PLL2) current	—	15.0	—	
Operating Frequency	f_{in}	f_{in1}	*1	10	—	1100	MHz
		f_{in2}	*2	10			
	OSC_{IN}	f_{osc}		—	12.8	20.0	
Input Sensitivity	f_{in}	P_{fin}	$V_{CC} = 2.7$ to $4.0V$, 50Ω	-10	—	0	dBm
			$V_{CC} = 4.0$ to $5.5V$, 50Ω	-4	—	2	
	OSC_{IN}	V_{OSC}		0.5	—	—	Vp-p
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		$V_{CC} \times 0.7 + 0.4$	—	—	V
Low-level Input Voltage		V_{IL}		—	—	$V_{CC} \times 0.3 - 0.4$	
High-level Input Current	Data, Clock LE	I_{IH}		—	1.0	—	μA
Low-level Input Current		I_{IL}		—	-1.0	—	
		FC	I_{FC}		—	-60	
Input Current	OSC_{IN}	I_{OSC}			± 50	—	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	$V_{CC} = 3.0 V$	2.2	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	
High-Impedance Cutoff Current	D_O , ϕP	I_{OFF}	$V_P = V_{CC}$ to $8.0 V$ $V_{OOP} = GND$ to $8.0 V$	—	—	1.1	μA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		-1.0	—	—	mA
		I_{OL}		1.0	—	—	
Analog Switch ON Resistance		R_{ON}		—	50	—	Ω

Notes: *1: Divide ratio of the prescaler is 128/129.
*2: Divide ratio of the prescaler is 64/65.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



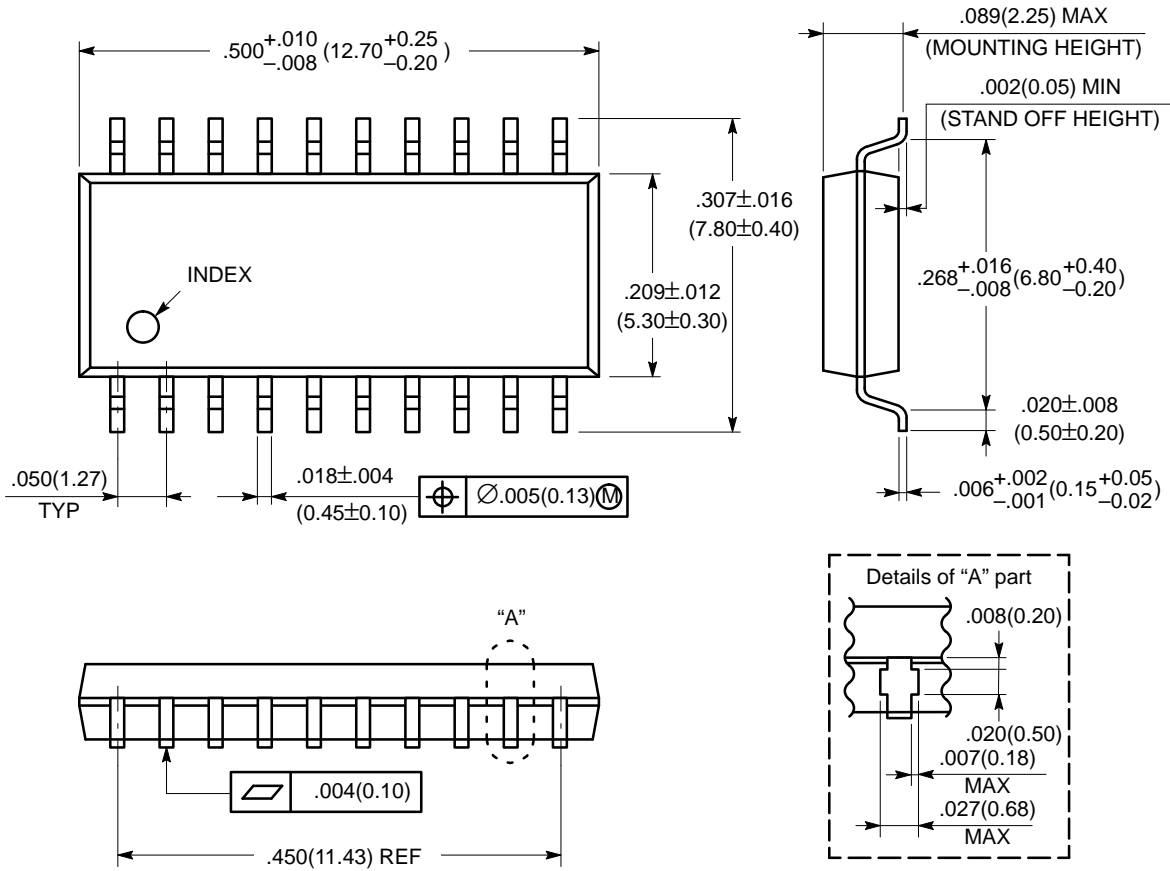
APPLICATION EXAMPLE



Note: **NOTE:**
 1 2.8MHz
 C1, C2: depends on the crystal oscillator.
 Clock, Data, LE: Using 5V logic levels (When inputs are left open, pull-down or pull-up resistors are necessary to prevent oscillation.)
 Crystal : 21.25MHz
 LD : Open drain

PACKAGE DIMENSIONS

**20-Lead Plastic Flat Package
(Case No.: FPT-20P-M01)**



All Rights Reserved.

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu assumes no responsibility for inaccuracies.

The information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu.

Fujitsu reserves the right to change products or specifications without notice.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Fujitsu.

FUJITSU LIMITED

For further information, please contact:

Japan

FUJITSU LIMITED
Semiconductor Marketing
Furukawa Sogo Bldg.
6-1,Marunouchi 2-chome
Chiyoda-ku, Tokyo 100
Japan
Tel: (03)3216-3211
Telex: 781-2224361
FAX: (03)3216-9771

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804 USA
Tel: (408)922-9000
FAX: (408)432-9044

Europe

FUJITSU MIKROELEKTRONIK GmbH
Arabella Centre 9.0G
Lyoner Strasse 44-48
D-6000 Frankfurt 71
F.R. Germany
Tel: (069) 66320
Telex: 411963
FAX: (069) 6632122

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
51 Bras Basah Road
Plaza by the Park
#06-04/07
Singapore 0718
Tel: 336-1600
Telex: 55373
FAX: 336-1609