

ASSP

1 CHANNEL 10-BIT D/A CONVERTER

MB40760

■ DESCRIPTION

MB40760 is a low-power consumption, high-speed 10-bit D/A converter.

The MB40760 is characterized by TTL compatible digital inputs, an analog output voltage from 3 to 5V, and a maximum conversion rate of 60 MHz. It provides a reference voltage from a potential divider and band-gap reference, and can also use an external reference voltage.

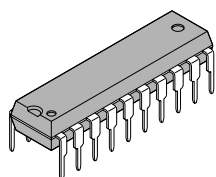
The MB40760 D/A converter is suitable for high-resolution TVs or VTRs.

■ FEATURES

- Resolution: 10 bits
- Conversion characteristics:
 - Maximum conversion rate: 60 MHz (Minimum)
 - Linearity error: $\pm 0.1\%$ (Maximum)
 - Differential linearity error: $\pm 0.1\%$ (Maximum)
- Input and output:
 - Digital input voltage: TTL levels
 - Analog output voltage: 2 V_{P-P} (3V to 5V)
- Reference voltage
 - V_{ROUT1}: Potential divider circuit (0.6 V_{CCA})
 - V_{ROUT2}: Band-gap reference circuit (V_{CCA}-2V)
- Others
 - Supply voltage: +5V single power supply
 - Power dissipation: 180 mW (Typical value at analog output voltage 2 VP-P)
140 mW (Typical value at analog output voltage 1 VP-P)

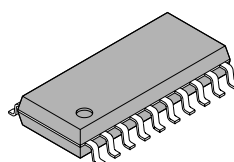
■ PACKAGES

Plastic DIP, 20 pin



(DIP-20P-M01)

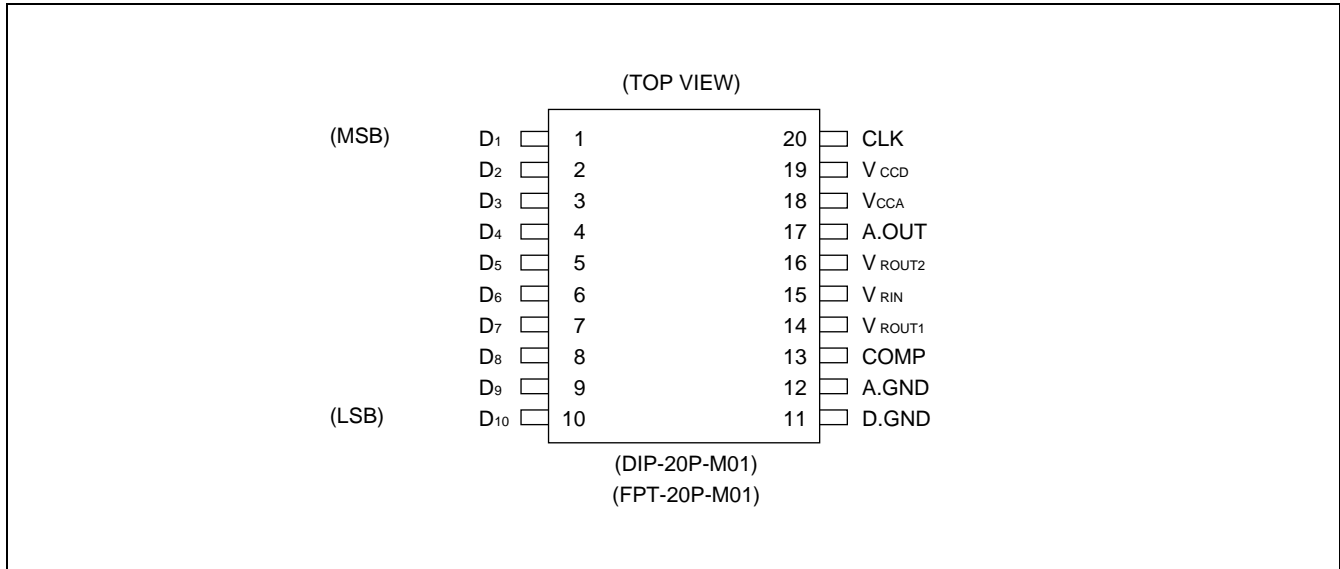
Plastic SOP, 20 pin



(FPT-20P-M01)

MB40760

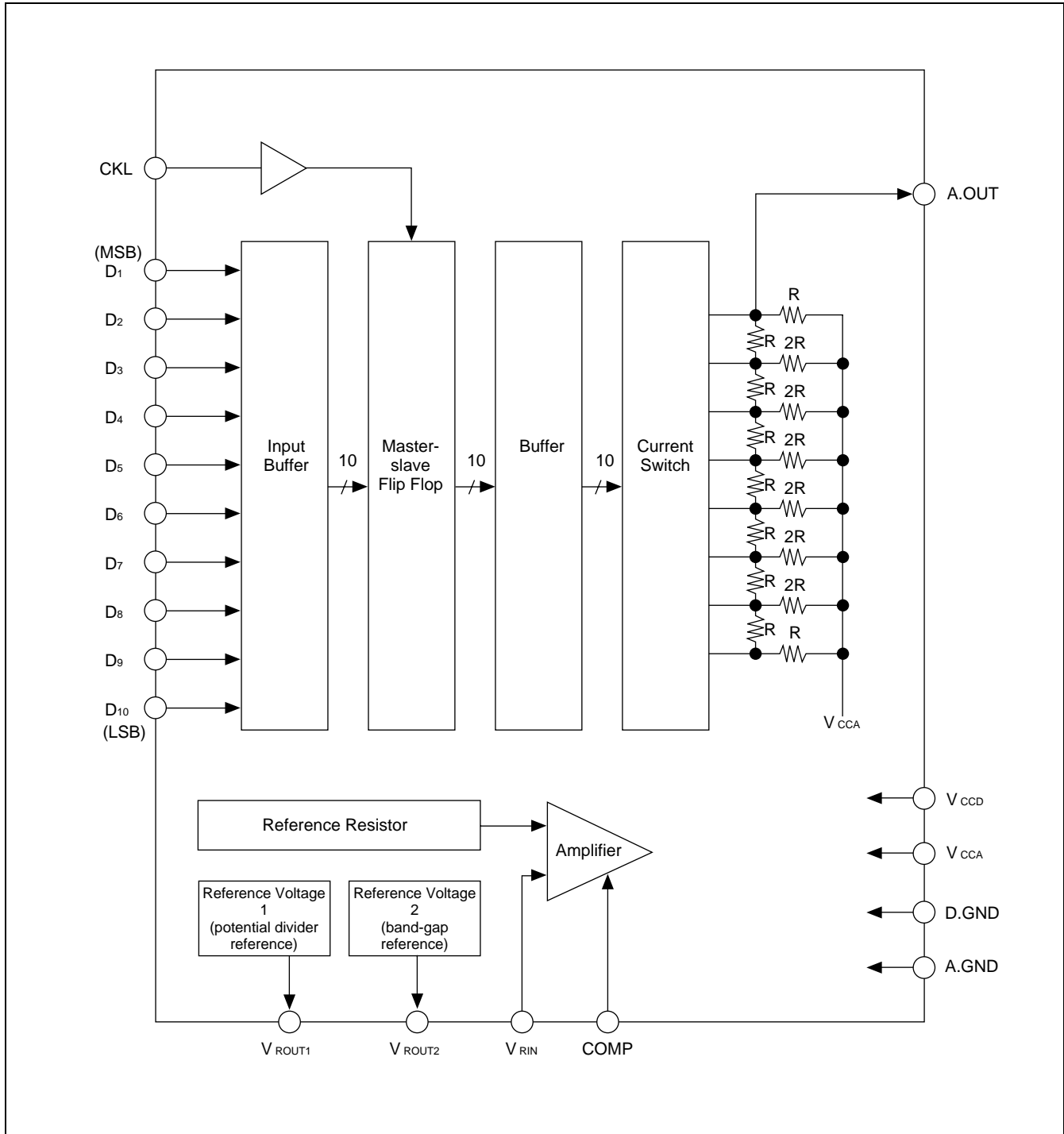
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

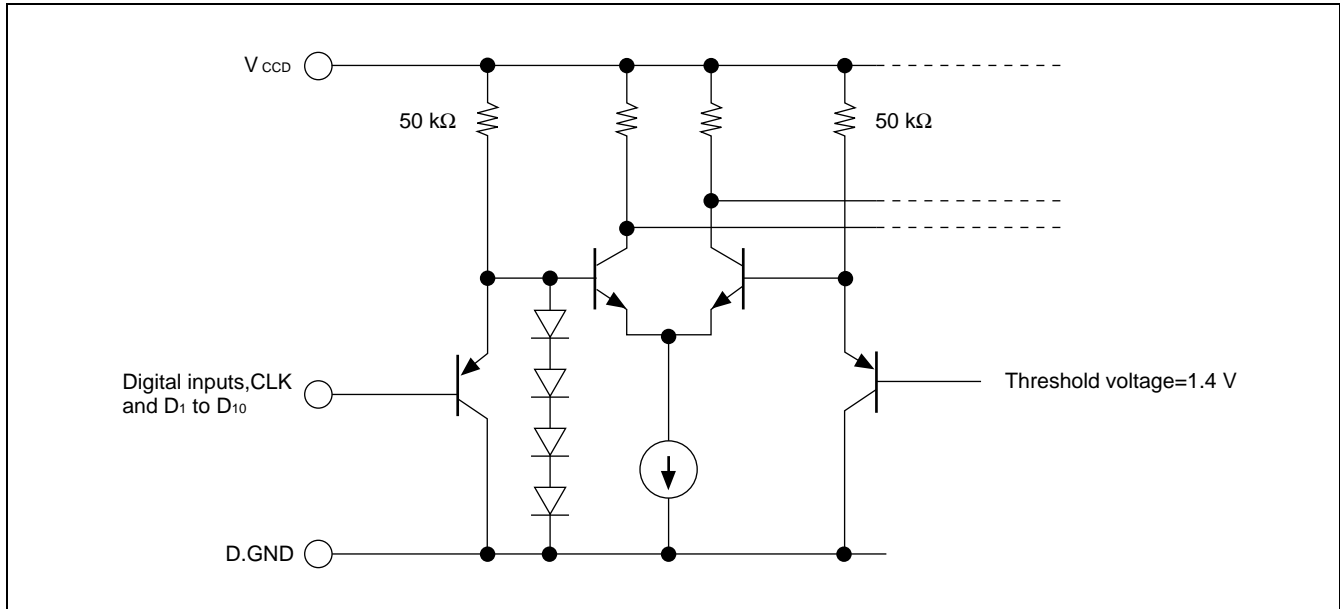
Pin No.	Symbol	I/O	Description
1 to 10	D1 to D10	I	Data signal input pin (D1: MSB, D10: LSB)
20	CLK	I	Clock signal input pin
19	VCCD	—	Digital power pin (+5V)
18	VCCA	—	Analog power pin (+5 V)
11	D.GND	—	Digital ground pin (0V)
12	A.GND	—	Analog ground pin (0V)
15	VRIN	I	Reference voltage input pin Analog output dynamic range setup pin Connect to pin 14 or 16 to use the built-in reference voltage When using an external reference voltage, the voltage on this pin must be from 2.7V to 4.3V, and VCCA-VRIN must be from 0.7V to 2.2V
14	VROUT1	O	Reference voltage output pin 1 The output voltage of the potential divider reference is fixed at 0.6 VCCA. When this pin is connected to pin 15, the analog output voltage ranges from 0.6 VCCA to VCCA
16	VROUT2	O	Reference voltage output pin 2 The output voltage of the band-gap reference is fixed at VCCA-2.0(V). When the pin is connected to pin 15, the analog output voltage ranges from VCCA-2.0(V) to VCCA
13	COMP	—	Phase compensation capacitor pin Insert a capacitor of 0.1 μF or greater between A.GND and COMP for phase compensation
17	A.OUT	O	Analog signal output pin

■ BLOCK DIAGRAM

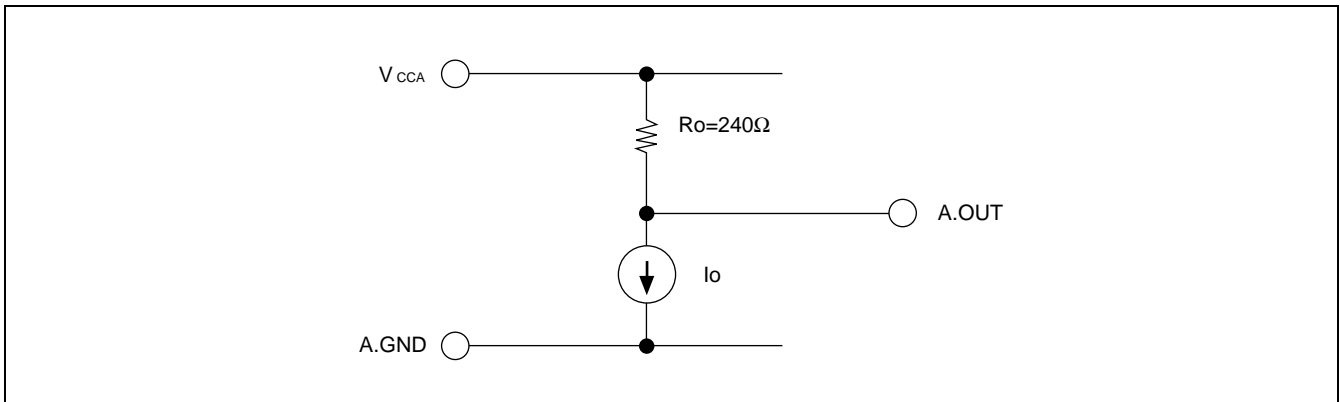


MB40760

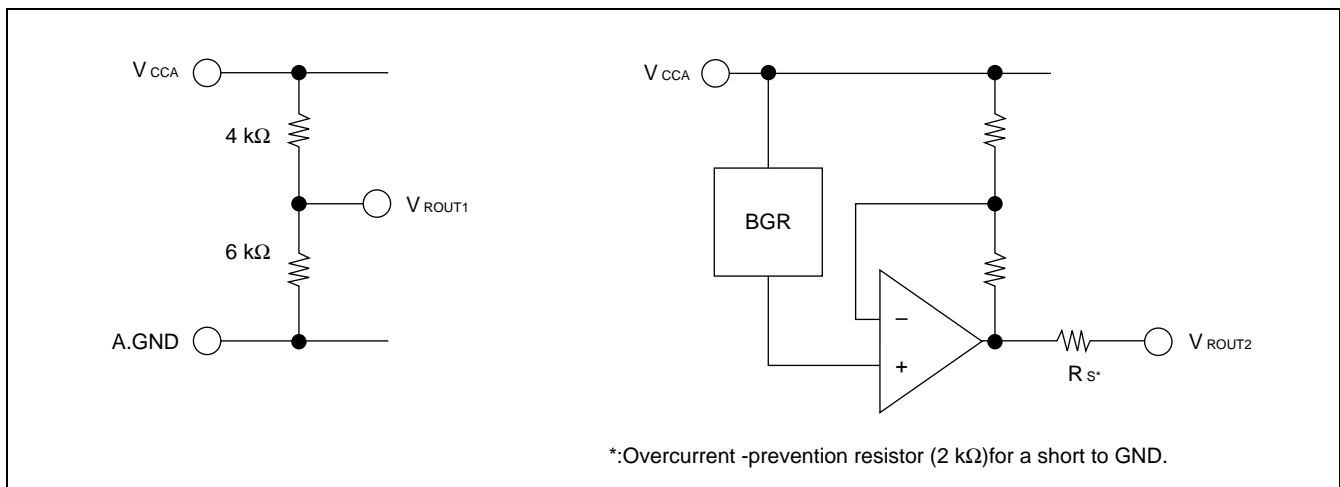
■ DIGITAL INPUT EQUIVALENT CIRCUIT



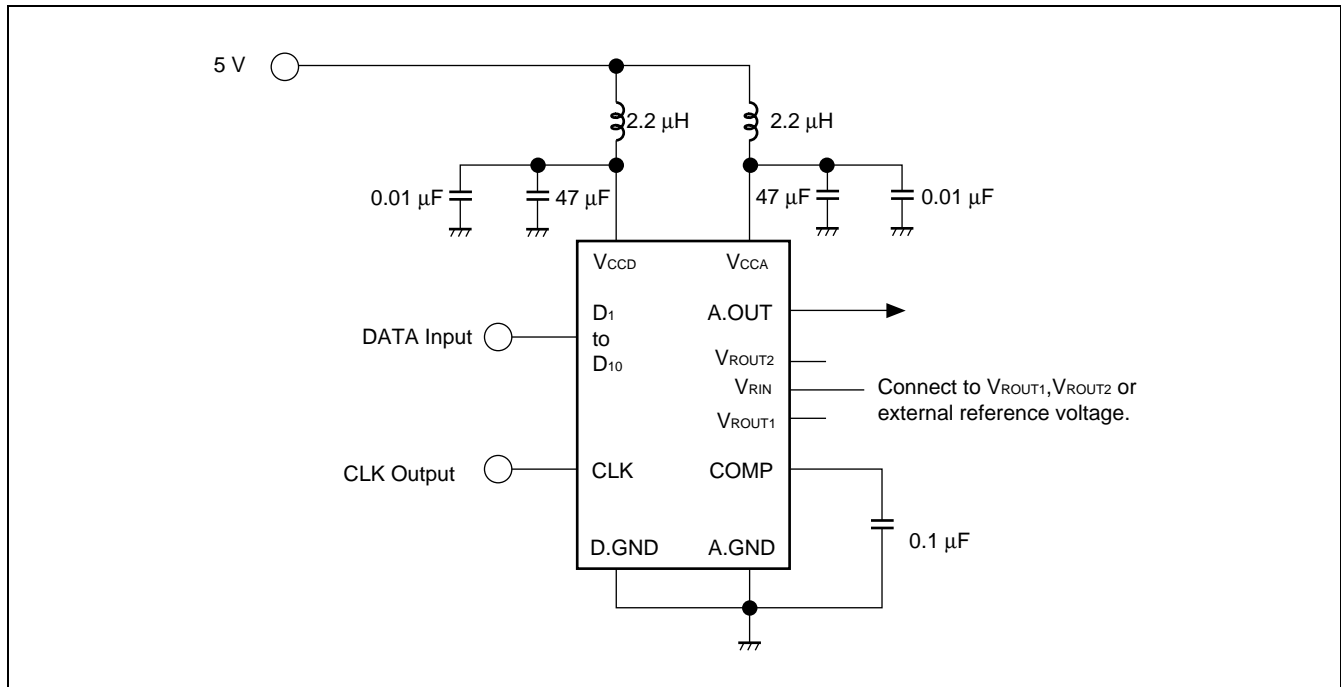
■ ANALOG OUTPUT EQUIVALENT CIRCUIT



■ REFERENCE VOLTAGE OUTPUT EQUIVALENT CIRCUIT



■ TYPICAL CONNECTION EXAMPLE



MB40760

■ ABSOLUTE MAXIMUM RATINGS

(A.GND = D.GND = 0V, Ta = +25°C)

Parameter	Symbol	Value	Unit
Analog power supply voltage	V _{CCA}	-0.5 to +7.0	V
Digital power supply voltage	V _{CCD}	-0.5 to +7.0	V
Power supply voltage difference	V _{CCD} -V _{CCA}	1.5	V
Digital signal input voltage	V _{ID}	-0.5 to +7.0	V
Storage Temperature	T _{stg}	-55 to +125	°C

Note: Permanent device damage may occur if the above Absolute Maximum Rating are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

(A.GND = D.GND = 0V, Ta = -20°C to +75°C)

Parameter		Symbol	Standard values			Unit
			Min.	Typ.	Max.	
Power supply voltage	Analog power supply voltage	V _{CCA}	4.75	5.00	5.25	V
	Digital power supply voltage	V _{CCD}	4.75	5.00	5.25	V
	Power supply voltage difference	V _{CCA} -V _{CCD}	-0.2	—	0.2	V
Analog reference voltage		V _{CCA} -V _{RIN}	0.70	2.00	2.20	V
		V _{RIN}	2.65	3.00	4.30	V
Digital input high voltage		V _{IHD}	2.0	—	—	V
Digital input low voltage		V _{ILD}	—	—	0.8	V
Clock frequency		f _{CLK}	—	—	60	MHz
Setup time		T _{su}	8	—	—	ns
Hold time		t _h	2	—	—	ns
Clock minimum pulse width high		t _{WH}	6.5	—	—	ns
Clock minimum pulse width low		t _{WL}	6.5	—	—	ns
Phase compensation capacitor		C _{COMP}	0.1	—	—	μF
Operating temperature		T _{OP}	-20	—	75	°C

■ DC CHARACTERISTICS

($V_{CCA} = V_{CCD} = 4.75$ to $5.25V$, $A.GND = D.GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

Parameter	Symbol	Conditions	Standard values			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	—	10	bit
Linearity error	LE	DC accuracy	—	—	± 0.1	%
Differential linearity error	DLE		—	—	± 0.1	%
Digital input current high	I _{IHD}	V _{IHD} = 2.7V	—	—	20	μA
Digital input current low	I _{ILD}	V _{ILD} = 0.4V	-100	—	—	μA
Reference input current	I _{RIN}	V _{RIN} = 3.000V	—	—	10	μA
Potential divider reference	Reference voltage	V _{ROUT1} V _{CCA} = 5.00V V _{CCD} = 5.00V	2.900	3.000	3.100	V
Band-gap reference	Reference voltage	V _{ROUT2}	V _{CCA} -2.100	V _{CCA} -2.000	V _{CCA} -1.900	V
	Temperature coefficient	—	—	100	—	ppm/ $^{\circ}C$
Full-scale output voltage	V _{OFS}	—	V _{CCA} -20	V _{CCA}	—	mV
Zero-scale output voltage	V _{OZS}	V _{CCA} = 5.00V V _{CCD} = 5.0V V _{RIN} = 3.000V	2.932	3.002	3.072	V
Output resistance	R _o	T _a = +25 $^{\circ}C$	192	240	288	Ω
Power dissipation	I _{CC}	V _{CCA} = 5.25V V _{CCD} = 5.25V V _{RIN} = V _{ROUT1}	—	36*	62	mA

* : $V_{CCA} = V_{CCD} = 5V$

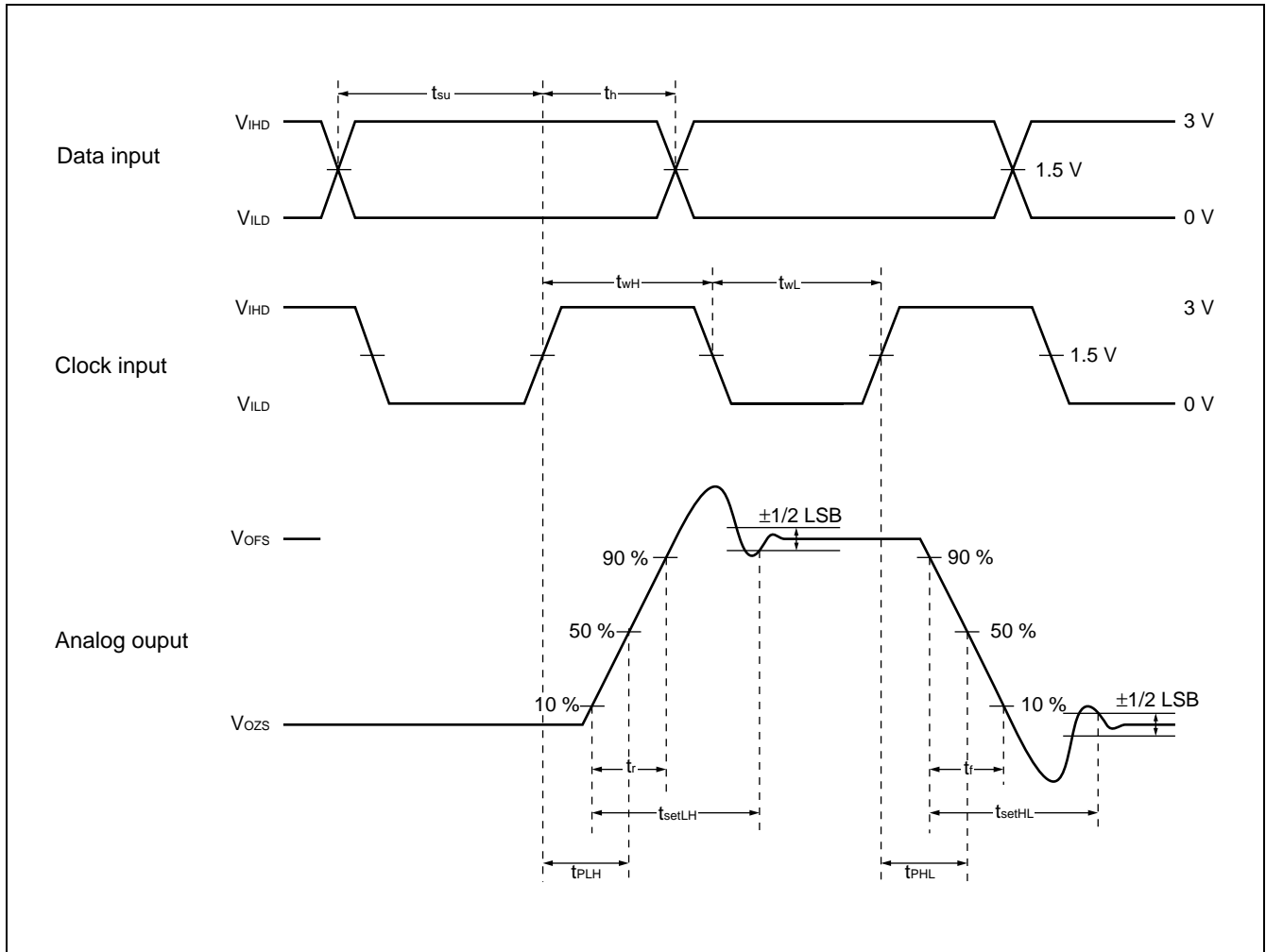
■ AC CHARACTERISTICS

($V_{CCA} = V_{CCD} = 4.75$ to $5.25V$, $A.GND = D.GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

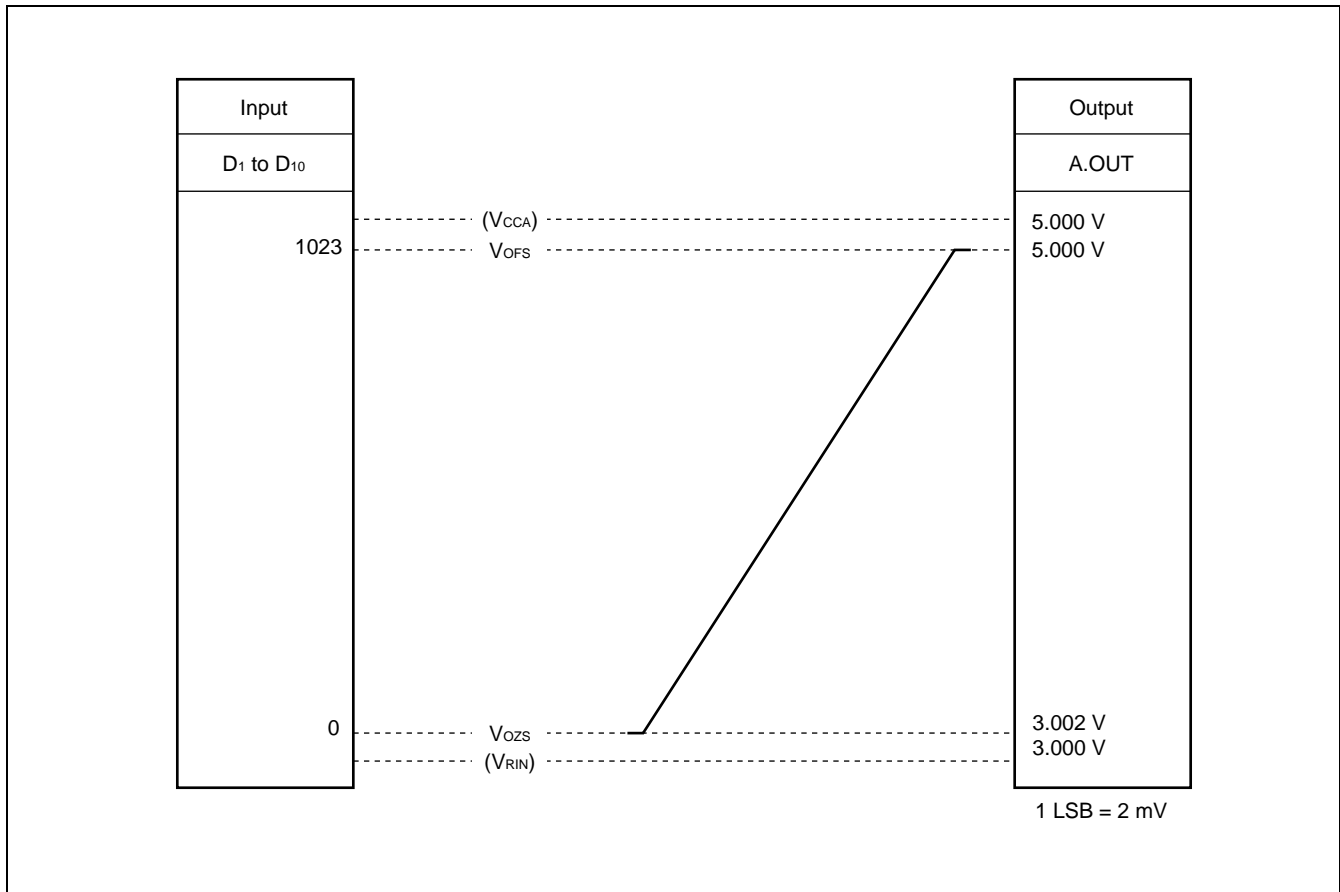
Parameter	Symbol	Conditions	Standard values			Unit
			Min.	Typ.	Max.	
Maximum conversion rate	F _s	C _L = 15pF A.OUT pin terminating resistance = 240 Ω	60	—	—	MSPS
Output propagation delay time	t _{pd}		—	7	—	ns
Output rise time	t _r		—	5	—	ns
Output fall time	t _f		—	5	—	ns
Settling time	t _{set}		—	17.5	—	ns

MB40760

■ TIMING CHART



■ DAC OUTPUT VOLTAGE CHARACTERISTICS



■ DAC OUTPUT VOLTAGE FORMULA IN IDEAL CONDITIONS

$$A.OUT = V_{CCA} - \frac{1023 - N}{1024} (V_{CCA} - V_{RIN})$$

(N: Digital input from 0 to 1023)

$$V_{OFS} = V_{CCA}$$

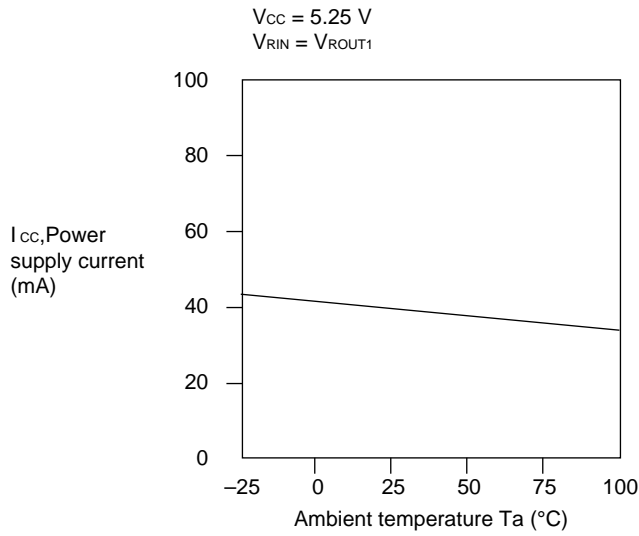
$$V_{OZS} = V_{CCA} - \frac{1023}{1024} (V_{CCA} - V_{RIN})$$

Notes:

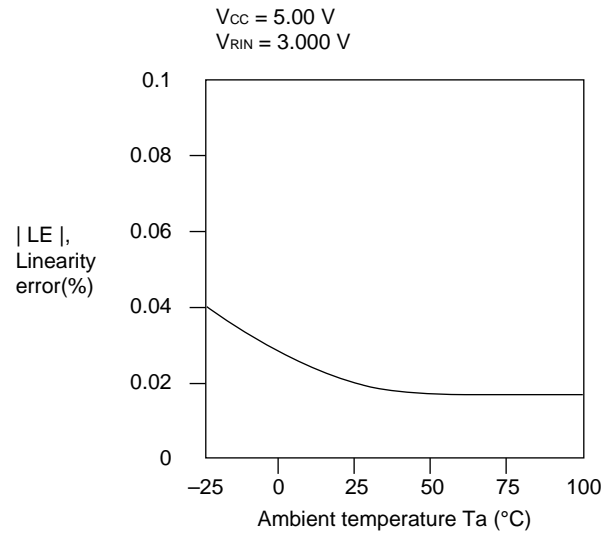
1. Preventing Switching Noise
To prevent switching noise in the analog output signal, connect noise limiting capacitors to the V_{CCA} and V_{CCD} pins as close to the A.GND and D.GND pins as possible.
2. Power Pattern
To reduce parasitic impedance, the PC board pattern to the V_{CCA} , V_{CCD} , A.GND and D.GND pins should be as wide as possible.

■ TYPICAL CHARACTERISTICS CURVES

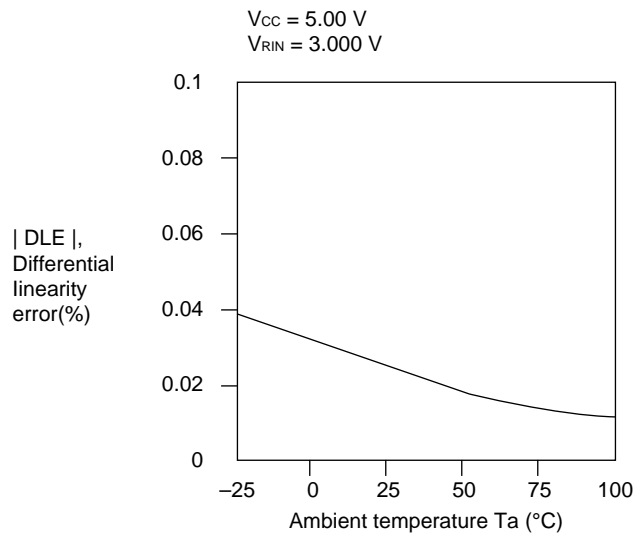
1. Power Supply Current v.s. Ambient Temperature



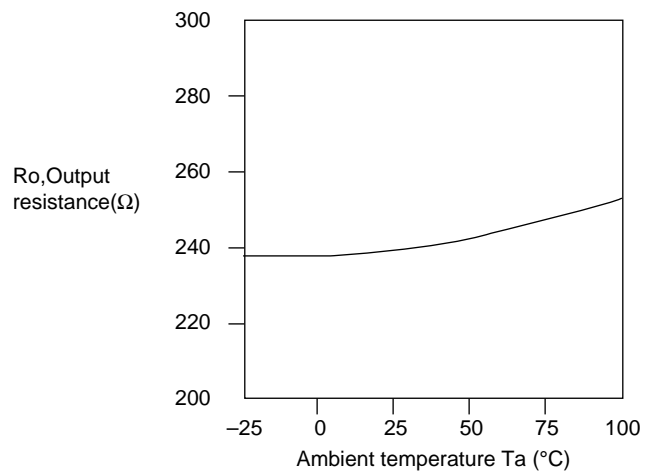
2. Linearity Error v.s. Ambient Temperature



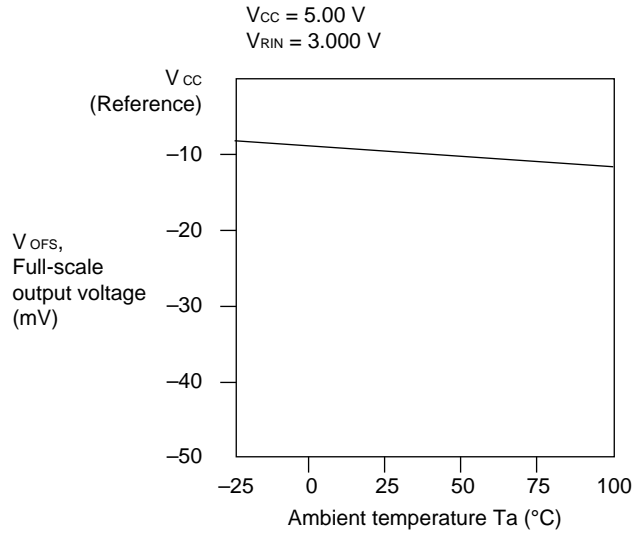
3. Differential Linearity Error v.s. Ambient Temperature



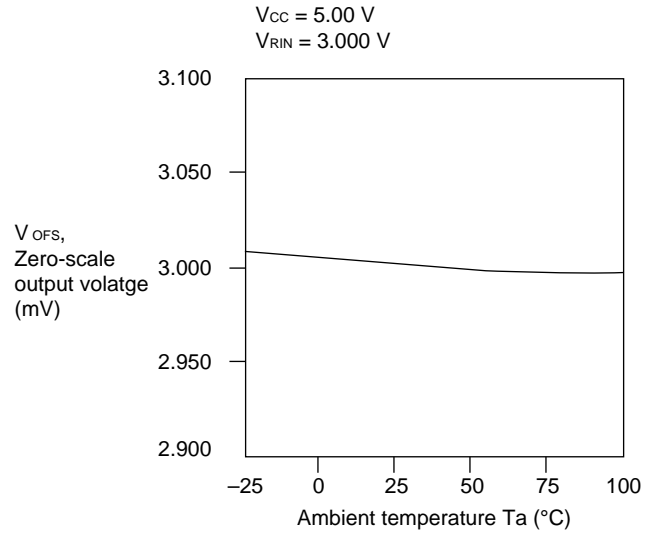
4. Output Resistance v.s. Ambient Temperature



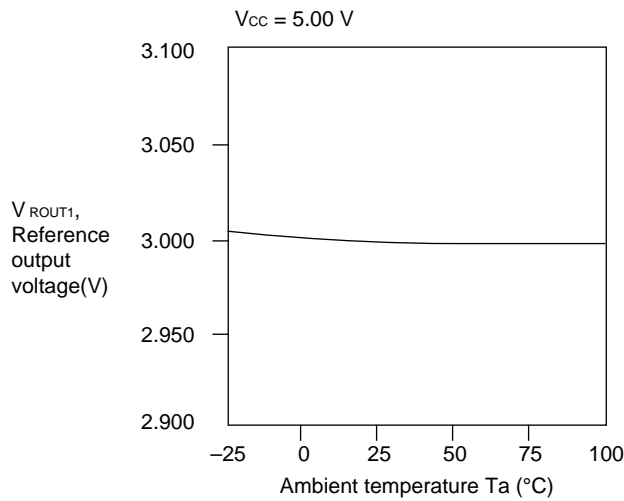
5. Full-Scale Output Voltage v.s. Ambient Temperature



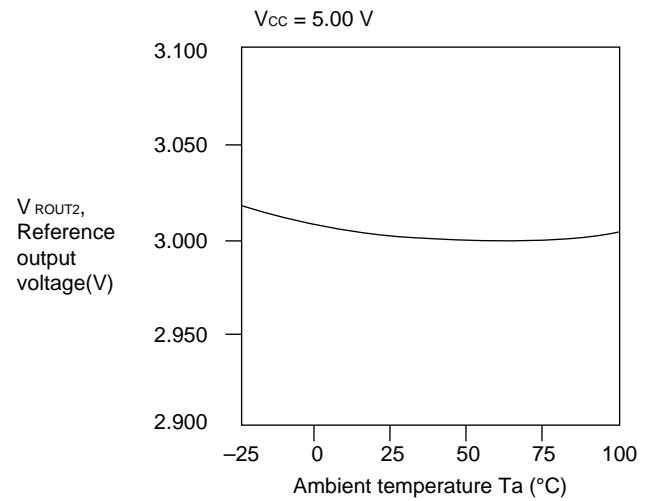
6. Zero-Scale Output Voltage v.s. Ambient Temperature



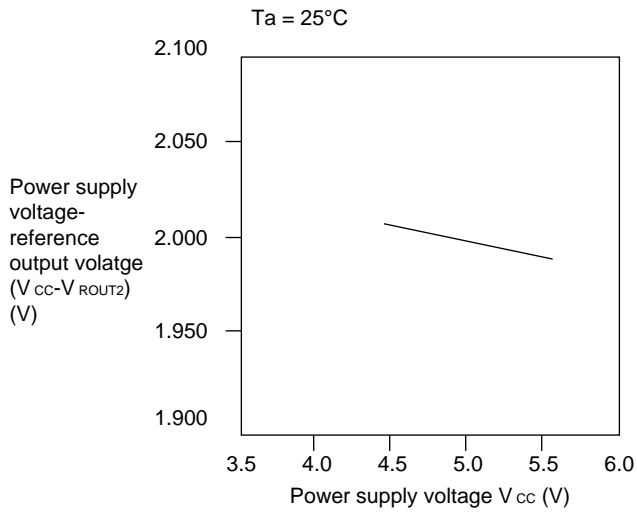
7. V_{ROUT1} Reference Output Voltage v.s. Ambient Temperature



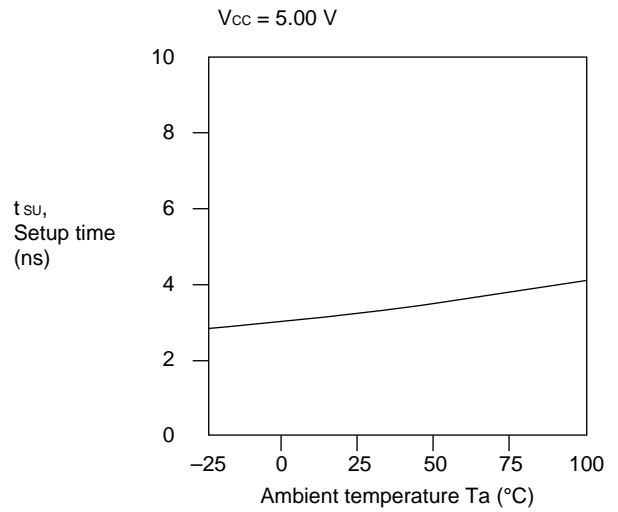
8. V_{ROUT2} Reference Output Voltage v.s. Ambient Temperature



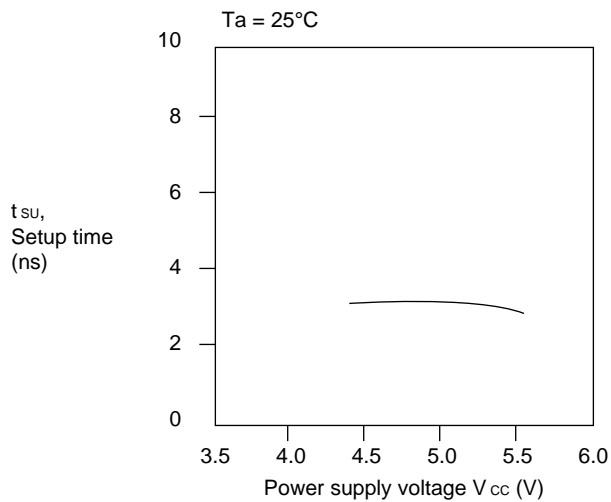
9. V_{ROUT2} Reference Output Voltage v.s. Power Supply Voltage



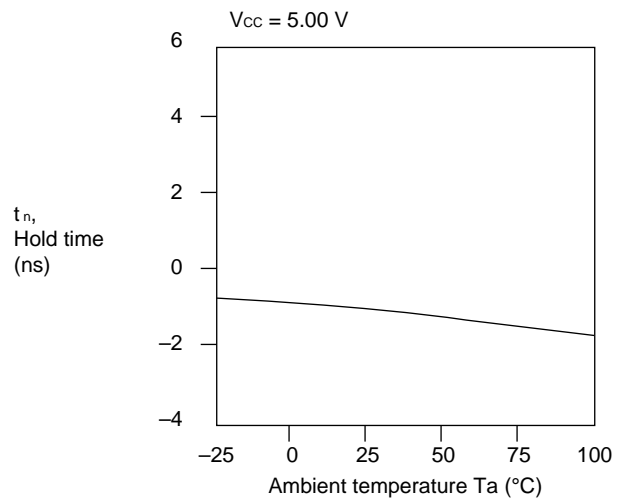
10. Setup Time v.s. Ambient Temperature



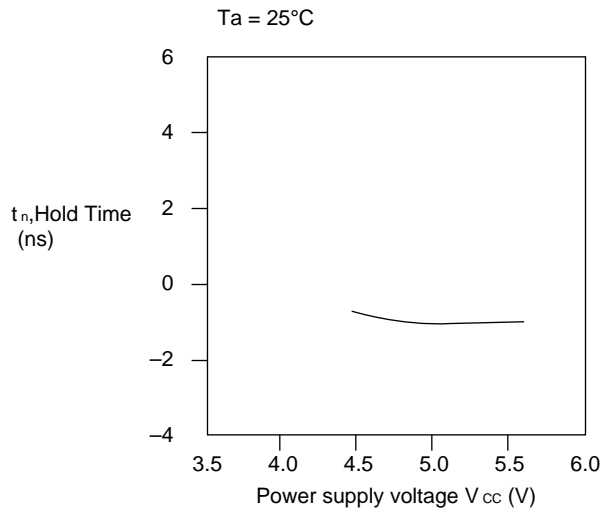
11. Setup Time v.s. Power Supply Voltage



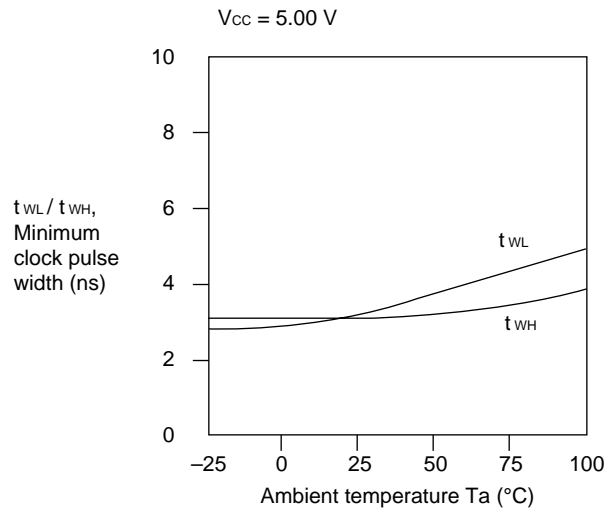
12. Hold Time v.s. Ambient Temperature



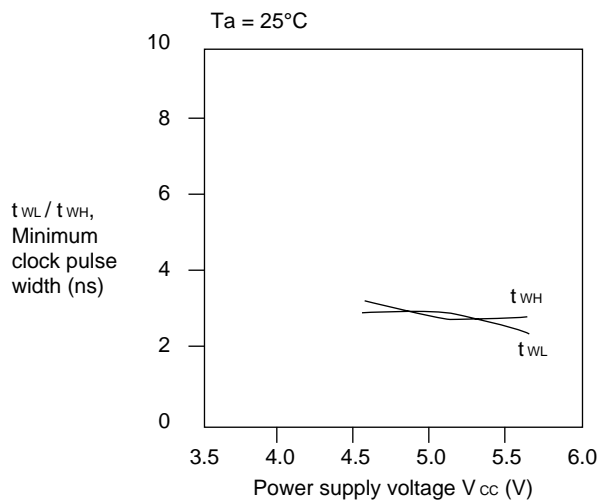
13. Hold Time v.s. Power Supply Voltage



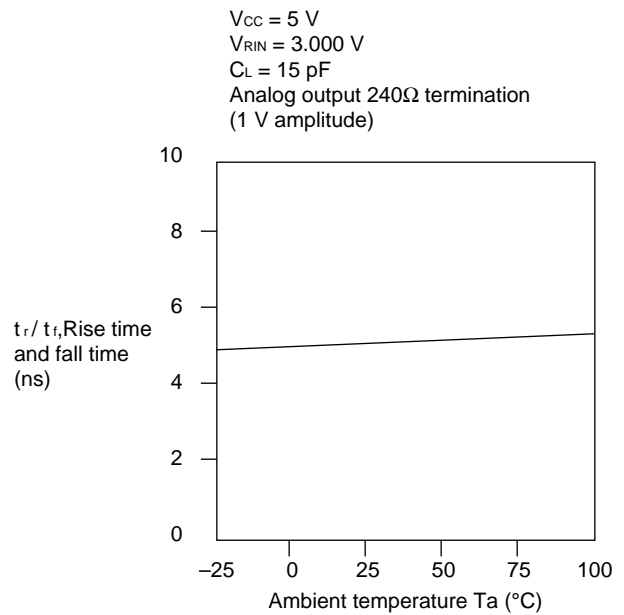
14. Minimum Clock Pulse Width v.s. Ambient Temperature



15. Minimum Clock Pulse Width v.s. Power Supply Voltage

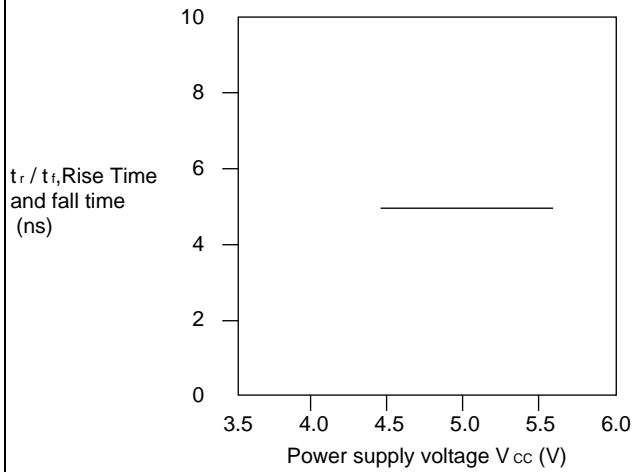


16. Rise Time / Fall Time v.s. Ambient Temperature



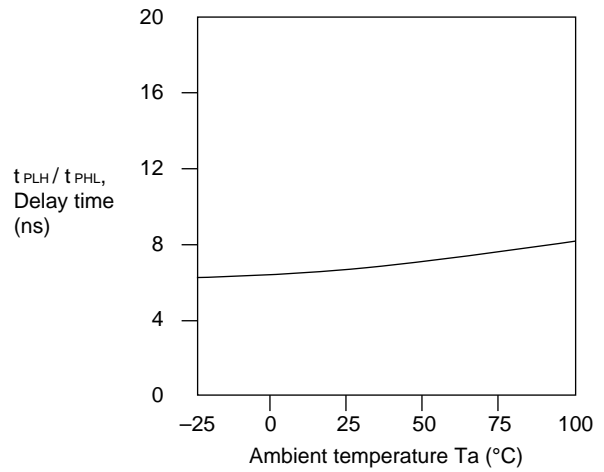
17. Rise Time / Fall Time v.s. Power Supply Voltage

$T_a = 25^\circ\text{C}$
 $V_{RIN} = 3.000\text{ V}$
 $C_L = 15\text{ pF}$
 Analog output 240Ω termination
 (1 V amplitude)



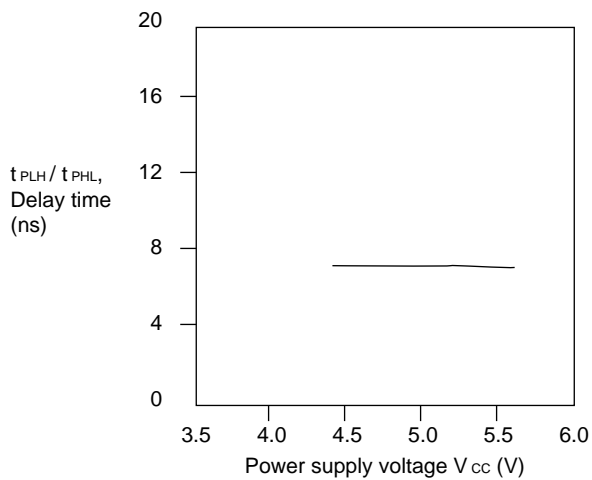
18. Delay Time v.s. Ambient Temperature

$V_{CC} = 5.00\text{ V}$
 $V_{RIN} = 3.000\text{ V}$
 $C_L = 15\text{ pF}$
 Analog output 240Ω termination
 (1 V amplitude)

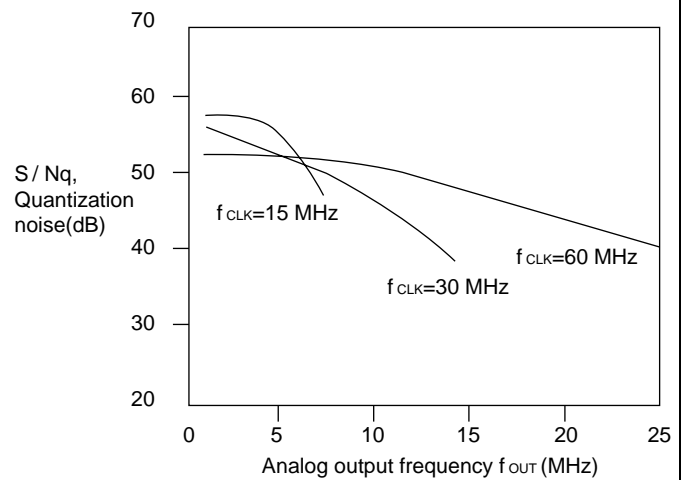


19. Delay Time v.s. Power Supply Voltage

$T_a = 25^\circ\text{C}$
 $V_{RIN} = 3.000\text{ V}$
 $C_L = 15\text{ pF}$
 Analog output 240Ω termination
 (1 V amplitude)

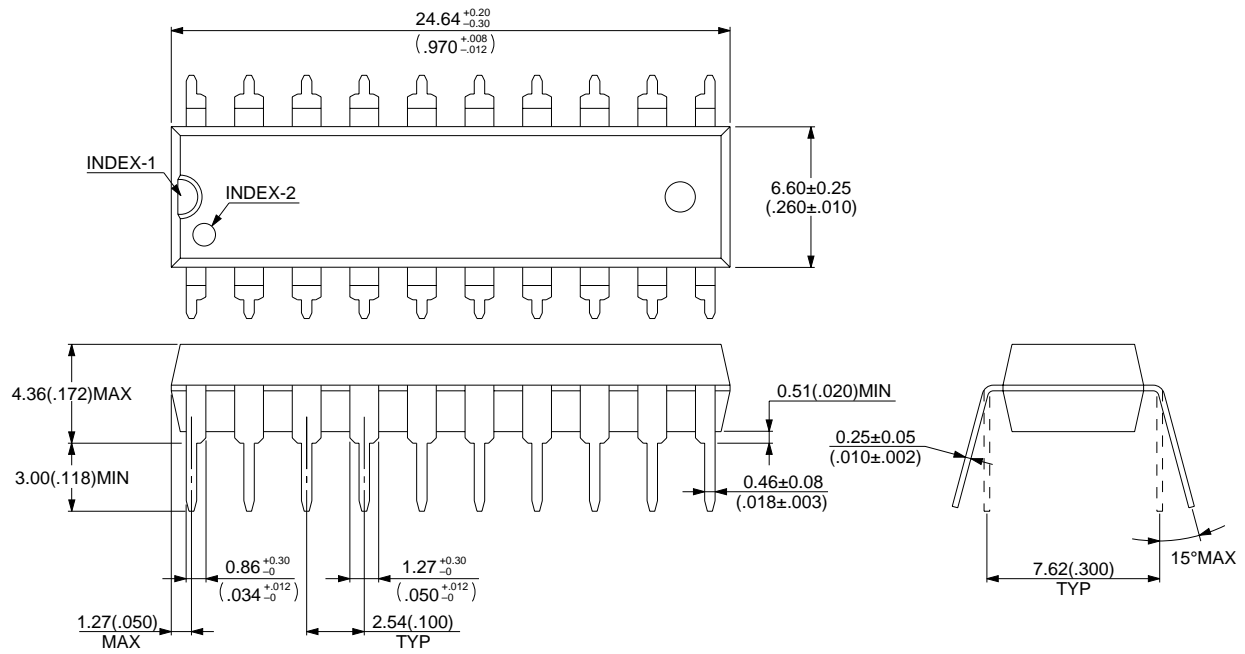


20. Quantization Noise v.s. Analog Output Frequency



■ PACKAGE DIMENSIONS

Plastic DIP, 20 pin
(DIP-20P-M01)

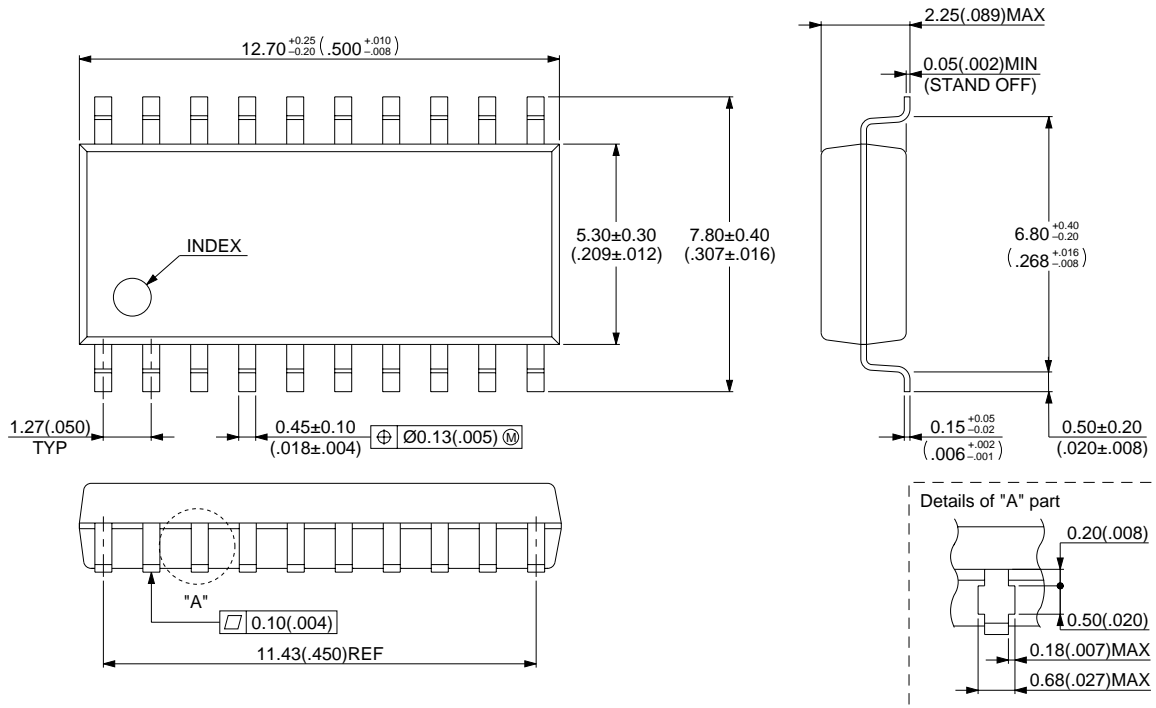


© 1994 FUJITSU LIMITED D20005S-3C-3

Dimensions in mm (inch)

MB40760

Plastic SOP, 20 pin
(FPT-20P-M01)



© 1994 FUJITSU LIMITED F20003S-5C-4

Dimensions in mm (inch)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3753
Fax: (044) 754-3329

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
No. 51 Bras Basah Road,
Plaza By The Park,
#06-04 to #06-07
Singapore 189554
Tel: 336-1600
Fax: 336-1609

All Rights Reserved.

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu assumes no responsibility for inaccuracies.

The information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu.

Fujitsu reserves the right to change products or specifications without notice.

No part of this publication may be copied or reproduced in any form or by any means, or transferred to any third party without prior written consent of Fujitsu.

The information contained in this document are not intended for use with equipments which require extremely high reliability such as aerospace equipments, undersea repeaters, nuclear control systems or medical equipments for life support.