DS05-11402-2E

MEMORY

CMOS

8 x 256K x 32 BIT, FCRAM™ CORE BASED DOUBLE DATA RATE SDRAM

MB81P643287-50/-60

**CMOS 8-BANK x 262,144-WORD x 32 BIT, FCRAM Core Based
Synchronous Dynamic Random Access Memory
with Double Data Rate**

■ DESCRIPTION

The Fujitsu MB81P643287 is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) with Fujitsu advanced FCRAM (Fast Cycle Random Access Memory) Core Technology, containing 67,108,864 memory cells accessible in an 32-bit format. The MB81P643287 features a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81P643287 is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timin.g constraints. The MB81P643287 uses Double Data Rate (DDR) where data bandwidth is twice of fast speed compared with regular SDRAMs.

The MB81P643287 is ideally suited for Digital Visual Systems, High Performance Graphic Adapters, Hardware Accelerators, Buffers, and other applications where large memory density and high effective bandwidth are required and where a simple interface is needed.

The MB81P643287 adopts new I/O interface circuitry, SSTL_2 interface, which is capable of extremely fast data transfer of quality under either terminated or point to point bus environment.

■ PRODUCT LINE

Parameter		MB81P643287	
		-50	-60
Clock Frequency	CL = 3	200 MHz Max.	167 MHz Max.
	CL = 2	133 MHz Max.	111 MHz Max.
Burst Mode Cycle Time	CL = 3	2.5 ns Min.	3.0 ns Min.
	CL = 2	3.75 ns Min.	4.5 ns Min.
Random Address Cycle Time		30 ns Min.	36 ns Min.
DQS Access Time From Clock		$0.1 \times t_{CK}$ + 0.2 ns Max.	$0.1 \times t_{CK}$ + 0.2 ns Max.
Operating Current		460 mA Max.	405 mA Max.
Power Down Current		35 mA Max.	

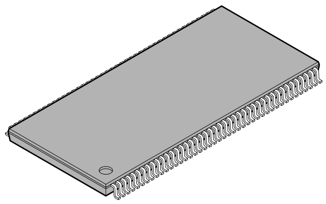
Note: FCRAM is a trademark of Fujitsu Limited, Japan.

■ FEATURES

- Double Data Rate
- Bi-directional Data Strobe Signal
- Eight bank operation
- Burst read/write operation
- Programmable burst length and CAS latency
- Byte write control by DM_0 to DM_3
- Standby Power Down Mode
- 4096 Auto-refresh cycles in 32 ms
- SSTL_2 (class 2) for all signals
- V_{DD}: +2.5V Supply ± 0.2V tolerance
- V_{DDQ}: +2.5V Supply ± 0.2V tolerance

■ PACKAGE

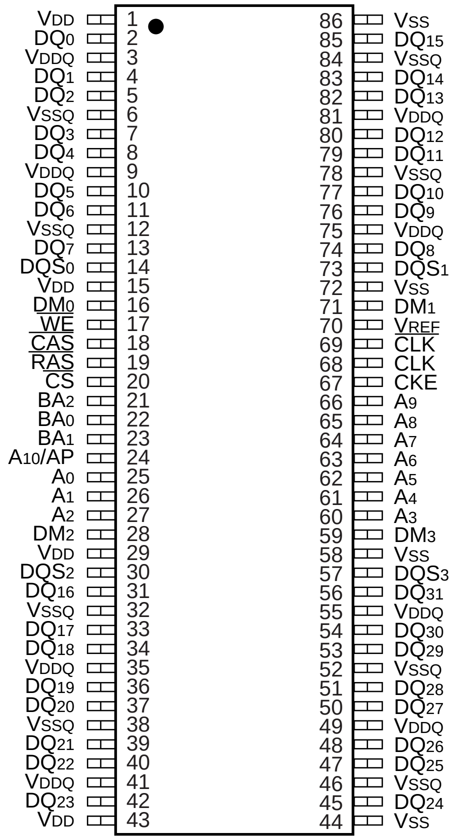
86-pin plastic TSOP(II)



(FPT-86P-M01)
(Normal Bend)

■ PIN ASSIGNMENTS

86-pin TSOP (II)
(TOP VIEW)
(Normal Bend)



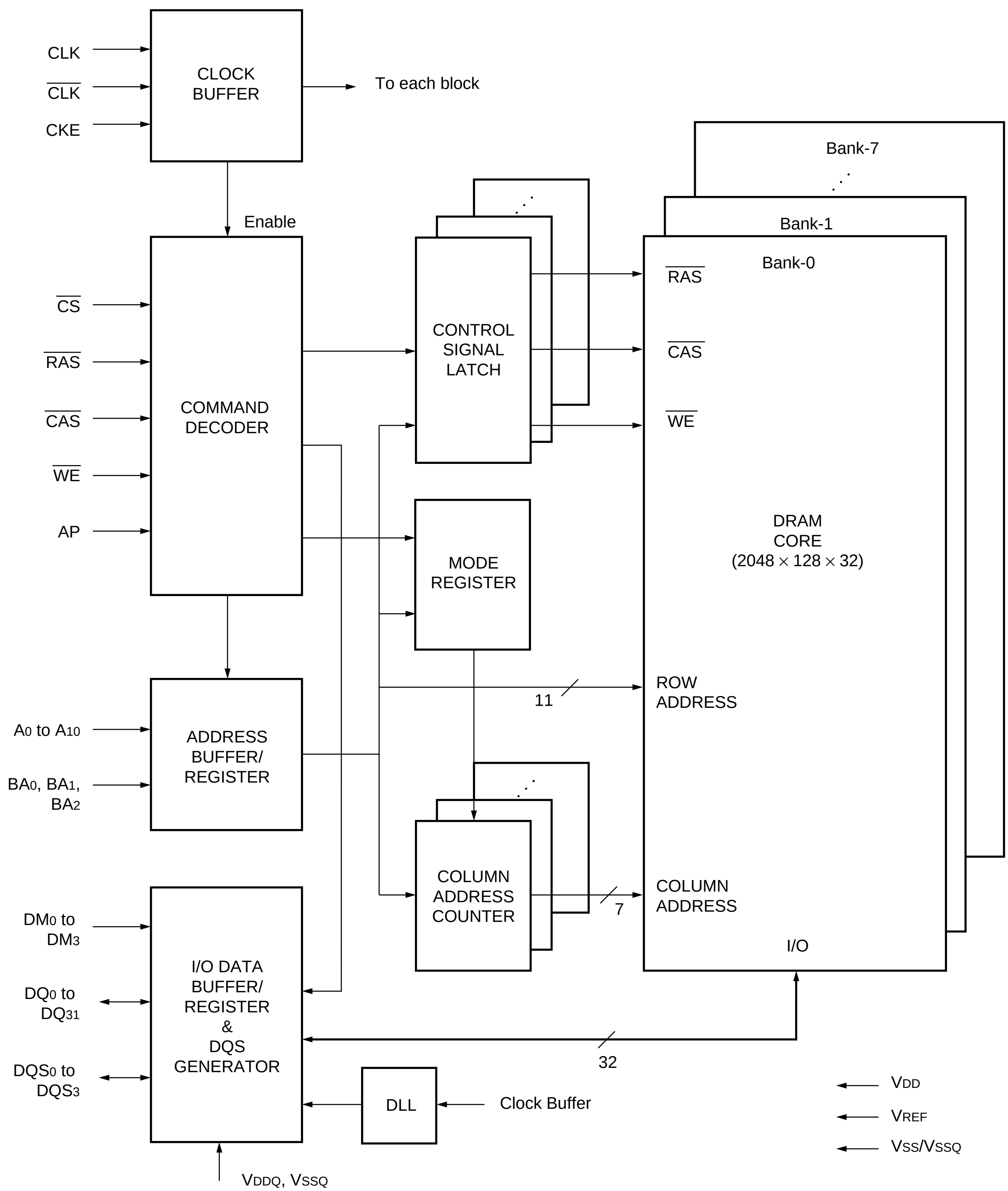
(FPT-86P-M01)

■ DESCRIPTIONS

Pin Number	Symbol	Function	
1, 3, 9, 15, 29, 35, 41, 43, 49, 55, 75, 81	V_{DD}, V_{DDQ}	Supply Voltage	
6, 12, 32, 38, 44, 46, 52, 58, 72, 78, 84, 86	V_{SS}, V_{SSQ}	Ground	
2, 4, 5, 7, 8, 10, 11, 13, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56, 74, 76, 77, 79, 80, 82, 83, 85	DQ_0 to DQ_{31}	Data I/O	• Byte 0: DQ_0 to DQ_7 • Byte 1: DQ_8 to DQ_{15} • Byte 2: DQ_{16} to DQ_{23} • Byte 3: DQ_{24} to DQ_{31}
14, 30, 57, 73	DQS_0 to DQS_3	Data Strobe	• DQS_0: for DQ_0 to DQ_7 • DQS_1: for DQ_8 to DQ_{15} • DQS_2: for DQ_{16} to DQ_{23} • DQS_3: for DQ_{24} to DQ_{31}
16, 28, 59, 71	DM_0 to DM_3	Input Mask	
17	$\overline{WE}$	Write Enable	
18	$\overline{CAS}$	Column Address Strobe	
19	$\overline{RAS}$	Row Address Strobe	
20	$\overline{CS}$	Chip Select	
21, 22, 23	BA_2, BA_1, BA_0	Bank Select (Bank Address)	
24	AP	Auto Precharge Enable	
24, 25, 26, 27, 60, 61, 62, 63, 64, 65, 66	A_0 to A_{10}	Address Input	• Row: A_0 to A_{10} • Column: A_0 to A_6
67	CKE	Power Down	
68	CLK	Clock Input	
69	$\overline{CLK}$	Clock Input	
70	V_{REF}	Input Reference Voltage	

■ BLOCK DIAGRAM

Fig. 1 - MB81P643287 BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE (Note*1)

COMMAND TRUTH TABLE (Note *2, and *3)

Function	Notes	Symbol	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA_{2-0}	A_{10}/AP	A_{9-7}	A_{6-0}
Device Deselect	*4	DESL	H	H	X	X	X	X	X	X	X
No Operation	*4	NOP	H	L	H	H	H	X	X	X	X
Burst Stop	*5	BST	H	L	H	H	L	X	X	X	X
Read	*6	READ	H	L	H	L	H	V	L	X	V
Read with Auto-precharge	*6	READA	H	L	H	L	H	V	H	X	V
Write	*6	WRIT	H	L	H	L	L	V	L	X	V
Write with Auto-precharge	*6	WRITA	H	L	H	L	L	V	H	X	V
Bank Active ($\overline{RAS}$)	*7	ACTV	H	L	L	H	H	V	V	V	V
Precharge Single Bank	*8	PRE	H	L	L	H	L	V	L	X	X
Precharge All Banks	*8	PALL	H	L	L	H	L	V	H	X	X
Mode Register Set/ Extended Mode Register Set	*8,9,10	MRS/ EMRS	H	L	L	L	L	V	L	V	V

Notes: *1. V = Valid, L = Logic Low, H = Logic High, X = either L or H, Hi-Z = High Impedance.
*2. All commands are assumed to be valid state transitions.
*3. All inputs for command are latched on the rising edge of clock(CLK).
*4. NOP and DESL commands have the same effect on the part.
Unless specifically noted, NOP will represent both NOP and DESL command in later descriptions.
*5. BST is effective after READ command is issued.
*6. READ, READA, WRIT and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to "■ STATE DIAGRAM".
*7. ACTV command should only be issued after corresponding bank has been page closed by PRE or PALL command.
*8. Either PRE or PALL command and MRS or EMRS command are required after power up.
*9. MRS or EMRS command should only be issued after all banks have been page closed (PRE or PALL command), and DQs are in Hi-Z. Refer to "■ STATE DIAGRAM".
*10. Refer to"■ MODE REGISTER TABLE".

DM TRUTH TABLE (Effective during Write mode)

Function	Command	CKE (n - 1)	CKE (n)	DM_0	DM_1	DM_2	DM_3
Data Mask for DQ_0 to DQ_7	MASK0	H	X	H	X	X	X
Data Mask for DQ_8 to DQ_{15}	MASK1	H	X	X	H	X	X
Data Mask for DQ_{16} to DQ_{23}	MASK2	H	X	X	X	H	X
Data Mask for DQ_{24} to DQ_{31}	MASK3	H	X	X	X	X	H

CKE TRUTH TABLE

Current State	Function	Notes	Command	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AP	BA_0 to BA_2	A_0 to A_{10}	DQ_0 to DQ_{31}
Idle	Auto-refresh	*11	REF	H	H	L	L	L	H	X	X	X	—
Idle	Self-refresh Entry	*11 *12	SELF	H	L	L	L	L	H	X	X	X	Hi-Z
Self-refresh	Self-refresh Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Self-refresh	Self-refresh Exit		SELFX	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z
Idle	Power Down Entry	*13	PDEN	H	L	L	H	H	H	X	X	X	Hi-Z
				H	L	H	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Exit		PDEX	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z

*11: The REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). In case of SELF command, it should also be issued after the last read data have been appeared on DQ. Refer to "■ STATE DIAGRAM".

*12: CKE must bring to Low level together with REF command.

*13: The PDEN command should only be issued after the last read data have been appeared on DQ and after the I_{DPL} is satisfied from last write data input.

OPERATION COMMAND TABLE (Applicable to single bank)(Note*13)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Bank Active after l_{RCD}	
	L	L	H	L	BA, AP	PRE	NOP	
	L	L	H	L	BA, AP	PALL	NOP	*15
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*17
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after l_{MRD})	*17
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*15
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Precharge	
	L	L	H	L	BA, AP	PALL	Precharge	*15
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	X	BST	Terminate Burst → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge	
	L	L	H	L	BA, AP	PALL	Terminate Burst, Precharge	*15
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP	*20
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge	*18
	L	L	H	L	BA, AP	PALL	Terminate Burst, Precharge	*15, *18
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read With Auto-Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write with Auto Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering with Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Write Recovering with Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Address	Command	Function	Notes
Precharging	H	X	X	X	X	DESL	NOP (Idle after t_{RP})	
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})	
	L	H	H	L	X	BST	NOP (Idle after t_{RP})	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	NOP	*16
	L	L	H	L	BA, AP	PALL	NOP	*15
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})	
	L	H	H	H	X	NOP	NOP (Bank Active after t_{RCD})	
	L	H	H	L	X	BST	NOP (Bank Active after t_{RCD})	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*19
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Write Recovering	H	X	X	X	X	DESL	NOP (Bank Active after l_{WRD})	
	L	H	H	H	X	NOP	NOP (Bank Active after l_{WRD})	
	L	H	H	L	X	BST	NOP (Bank Active after l_{WRD})	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write Recovering with Auto-precharge	H	X	X	X	X	DESL	NOP (Idle after l_{WAL})	
	L	H	H	H	X	NOP	NOP (Idle after l_{WAL})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after l_{RFC})	
	L	H	H	X	X	NOP/BST	NOP (Idle after l_{RFC})	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF/ MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after l_{MRD})	
	L	H	H	H	X	NOP	NOP (Idle after l_{MRD})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	Illegal	

Abbreviations: RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

Notes: *14. All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle.
*15. Entry may affect other banks.
*16. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
*17. Illegal if any bank is not idle.
*18. Must mask preceding data that don‘t satisfy lDPL.
*19. Legal if other bank specified in BA is idle state and lRRD is satisfied for that bank.
*20. Must mask preceding data that don‘t satisfy lWRD.

COMMAND TRUTH TABLE FOR CKE

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{PDEX} + l_{SCD} or l_{XSNR})	
	L	H	L	H	H	H	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{PDEX} + l_{SCD} or l_{XSNR})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after l_{SCD} or l_{XSNR}	
	H	H	L	H	H	H	X	Idle after l_{SCD} or l_{XSNR}	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Power Down Exit → Return to original state after t_{PDEX}	
	L	H	L	H	H	H	X	Power Down Exit → Return to original state after t_{PDEX}	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	

COMMAND TRUTH TABLE FOR CKE (continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
All Banks Idle	H	H	H	X	X	X	X	NOP	
	H	H	L	H	X	X	V	Refer to the Command Truth Table.	
	H	H	L	L	H	X	V	Refer to the Command Truth Table.	
	H	H	L	L	L	H	X	Auto-refresh	
	H	H	L	L	L	L	V	Mode Register Set	*21
	H	L	H	X	X	X	X	Power Down Entry	*22
	H	L	L	H	H	H	X	Power Down Entry	*22
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh Entry	*22
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	
Bank Active	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	

COMMAND TRUTH TABLE FOR CKE (continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Bank Activating, Read, Write, Write Recovering, Precharging	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*23
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*23
Refresh	H	L	H	L	L	L	X	Illegal	
	H	L	L	H	H	H	X	Illegal	
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	

Notes: *21. Refer to "■ MODE REGISTER TABLE".
*22. PDEN and SELF command should only be issued after the last read data have been appeared on DQ.
*23. The Clock Suspend mode is not supported on this device and it is illegal if CKE is brought to Low during the Burst Read or Write mode.

■ STATE DIAGRAM

MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

First command \ Second command (same bank)	MRS	ACTV	READ	READA	WRIT	WRITA	BST	*1 PRE	PALL	REF	SELF
MRS	l_{MRD}	l_{MRD}					l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}
ACTV			l_{RCD}	*4 l_{RCD}	l_{RCD}	*4 l_{RCD}	1	l_{RAS}	l_{RAS}		
READ			1	*4 1	*3 l_{RWD}	*3, 4 l_{RWD}	1	*4 1	*4 1		
READA	*5, 6 BL/2 + l_{RP}	BL/2 + l_{RP}						*4 BL/2 + l_{RP}	*4 BL/2 + l_{RP}	*6 BL/2 + l_{RP}	*5, 6 BL/2 + l_{RP}
WRIT			*7 l_{WRD}	*4, 7 l_{WRD}	1	*4 1		*4,7 l_{DPL}	*4,7 l_{DPL}		
WRITA	*6 l_{WAL}	l_{WAL}						*4 l_{WAL}	*4 l_{WAL}	*6 l_{WAL}	*6 l_{WAL}
BST			1	1	*3 l_{BSNC}	*3 l_{BSNC}	1	*4 1	*4 1		
PRE	*5, 6 l_{RP}	l_{RP}					1	1	*4 1	*6 l_{RP}	*5, 6 l_{RP}
PALL	*5 l_{RPA}	l_{RPA}					1	1	1	l_{RPA}	*5 l_{RPA}
REF	l_{RFC}	l_{RFC}					l_{RFC}	l_{RFC}	l_{RFC}	l_{RFC}	l_{RFC}
SELFX	l_{XSNR}	l_{XSNR}					l_{XSNR}	l_{XSNR}	l_{XSNR}	l_{XSNR}	l_{XSNR}

Notes: *1. BL/2 = $t_{CK} \times$ BL / 2. (Example: In case of BL = 4, BL/2 means 2 clocks.)
*2. Assume PALL command does not affect any operation on the other bank(s).
*3. Assume no I/O conflict.
*4. l_{RAS} must be satisfied.
*5. Assume all outputs are in High-Z state.
*6. Assume all other banks are in idle state.
*7. l_{DPL} and l_{WRD} are specified from last data input and assumed preceding pair of write data are masked by DM_0 to DM_3 input.

Illegal Command

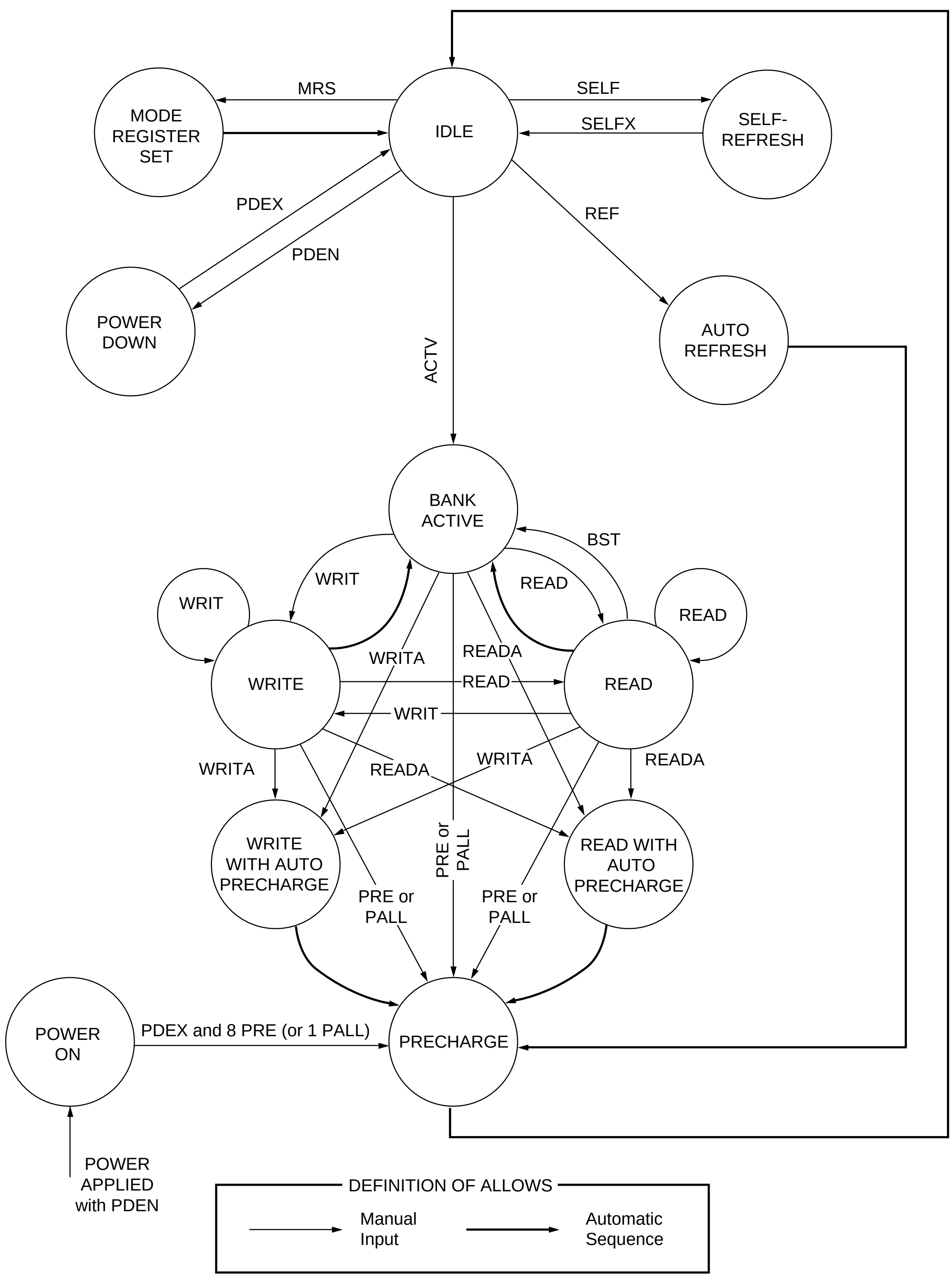
MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTIPLE BANK OPERATION

Second command (other bank) *10 / First command	MRS	ACTV	*8 READ	*8 READA	*8 WRIT	*8 WRITA	*9 BST	*2, 9 PRE	PALL	REF	SELF
MRS	l_{MRD}	l_{MRD}					l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}	l_{MRD}
ACTV		*6 l_{RRD}	*11 1	*11 1	*11 1	*11 1	*11 1	1	l_{RAS}		
READ		*6 1	1	1	* 3 l_{RWD}	*3 l_{RWD}	1	1	*4 1		
READA	*5, 6 BL/2 + l_{RP}	*6 1	*4 1	*4 1	* 3, 4 l_{RWD}	* 3, 4 l_{RWD}		1	BL/2 + l_{RP}	*6 BL/2 + l_{RP}	*5, 6 BL/2 + l_{RP}
WRIT		*6 1	*7 l_{WRD}	*7 l_{WRD}	1	1		1	*4,7 l_{DPL}		
WRITA	*6 l_{WAL}	*6 1	*4 BL/2 + l_{WRD}	*4 BL/2 + l_{WRD}	*4 1	*4 1		1	l_{WAL}	*6 l_{WAL}	*6 l_{WAL}
BST		*6 1	*11 1	*11 1	*3, 11 l_{BSNC}	*3, 11 l_{BSNC}	1	1	*4 1		
PRE	*5, 6 l_{RP}	*6 1	*11 1	*11 1	*3, 11 1	*3, 11 1	*11 1	1	*4 1	*6 l_{RP}	*5, 6 l_{RP}
PALL	*5 l_{RPA}	l_{RPA}					1	1	1	l_{RPA}	*5 l_{RPA}
REF	l_{RFC}	l_{RFC}					l_{RFC}	l_{RFC}	l_{RFC}	l_{RFC}	l_{RFC}
SELFX	l_{XSNR}	l_{XSNR}					l_{XSNR}	l_{XSNR}	l_{XSNR}	l_{XSNR}	l_{XSNR}

Notes: *1. BL/2 = $t_{CK} \times BL / 2$. (Example: In case of BL = 4, BL/2 means 2 clocks.)
*2. Assume PALL command does not affect any operation on the other bank(s).
*3. Assume no I/O conflict.
*4. l_{RAS} must be satisfied.
*5. Assume all outputs are in High-Z state.
*6. Assume the other bank(s) is in idle state.
*7. l_{DPL} and l_{WRD} are specified from last data input and assumed preceding pair of write data are masked by DM_0 to DM_3 input.
*8. Assume the other bank(s) is in active state and l_{RCD} is satisfied.
*9. Assume the other bank(s) is in active state and l_{RAS} is satisfied.
*10. Second command have to follow the minimum clock latency or delay time of single bank operation in other bank (second command is asserted.)
*11. Assume other banks are not in READA/WRITA state.

Illegal Command.

Fig. 2 - STATE DIAGRAM (Simplified for Single Bank Operation)



■ FUNCTIONAL DESCRIPTION

DDR, Double Data Rate Function

The regular SDRAM read and write cycle have only used the rising edge of external clock input. When clock signal goes to High from Low at the read mode, the read out data will be available at every rising clock edge after the specified latency up to burst length. The MB81P643287 DDR FCRAM features a twice of data transfer rate within a same clock period by transferring data at every rising and falling clock edge. Refer to Figure 3.

FCRAM™

The MB81P643287 utilizes FCRAM core technology. The FCRAM is an acronym of Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

CLOCK INPUT (CLK, $\overline{\text{CLK}}$)

The MB81P643287 adopts differential clock scheme. CLK is a master clock and its rising edge is used to latch all command and address inputs. $\overline{\text{CLK}}$ is a complementary clock input.
The MB81P643287 implements Delay Locked Loop (DLL) circuit. This internal DLL tracks the signal cross point between CLK and $\overline{\text{CLK}}$ and generate some clock cycle delay for the output buffer control at Read mode.
The internal DLL circuit requires some Lock-on time for the stable delay time generation. In order to stabilize the delay, a constant stable clock input for l_{PCD} period is required during the Power-up initialization and a constant stable clock input for l_{SCD} period is also required after Self-refresh exit as specified l_{SCD} prior to the any command.

POWER DOWN (CKE)

CKE is a synchronous input signal and enables power down mode.
When all banks are in idle state, CKE controls Power Down (PD) and Self-refresh mode. The PD and Self-refresh is entered when CKE is brought to Low and exited when it returns to High.
During the Power Down and Self-refresh mode, both CLK and $\overline{\text{CLK}}$ are disabled after specified time.
CKE does not have a Clock Suspend function unlike CKE pin of regular SDRAMs, and it is illegal to bring CKE into Low if any read or write operation is being performed. For the detail, refer to Timing Diagrams.
It is recommended to maintain CKE to be Low until V_{DD} gets in the specified operating range in order to assure the power-up initialization.

CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ enables all commands inputs, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$, and address input. When $\overline{\text{CS}}$ is High, all command signals are negated but internal operation such as burst cycle will not be suspended.

COMMAND INPUTS ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$)

As well as regular SDRAMs, each combination of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ input in conjunction with $\overline{\text{CS}}$ input at a rising edge of the CLK determines SDRAM operation. Refer to “■FUNCTION TRUTH TABLE”.

BANK ADDRESS (BA_0 to BA_2)

The MB81P643287 has eight internal banks and each bank is organized as 256K words by 32-bit.
Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and Precharge(PRE) command.

ADDRESS INPUTS (A_0 to A_{10})

Address input selects an arbitrary location of a total of 2,097,152 words of each memory cell matrix within each bank. A total of twenty address input signals are required to decode such a matrix. DDR SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), eleven Row addresses are initially latched as well as three Bank addresses and the remainder of seven Column addresses are then latched by a Column address strobe command of either a read command (READ or READA) or write command (WRIT or WRITA).

DATA STROBE (DQS_0 to DQS_3)

DQS_0 to DQS_3 are bi-directional signal and represent byte 0 to byte 3, respectively. During Read operation, DQS_0 to DQS_3 provides the read data strobe signal that is intended to use input data strobe signal at the receiver circuit of the controller(s). It turns Low before first data is coming out and toggle High to Low or Low to High till end of burst read. Refer to Figure 3 for the timing example.
The CAS Latency is specified to the first Low to High transition of these DQS_0 to DQS_3 output.
During the write operation, DQS_0 to DQS_3 are used to latch write data and Data Mask signals. As well as the behavior of read data strobe, the first rising edge of DQS_0 to DQS_3 input latches first input data and following falling edge of DQS_0 to DQS_3 signal latches second input data. This sequence shall be continued till end of burst count. Therefore, DQS_0 to DQS_3 must be provided from controller that drives write data.
Note that DQS_0 to DQS_3 input signal should not be tristated from High at the end of write mode.

DATA INPUTS AND OUTPUTS (DQ_0 to DQ_{31})

Input data is latched by DQS_0 to DQS_3 input signal and written into memory at the clock following the write command input. Output data is obtained together with DQS_0 to DQS_3 output signals at programmed read CAS latency.
The polarity of the output data is identical to that of the input. Data is valid after DQS_0 to DQS_3 output signal transitions (t_{QSQ}) as specified in Data Valid Time (t_{DV}).

WRITE DATA MASK (DM_0 to DM_3)

DM_0 to DM_3 are active High enable inputs and represent byte 0 to byte 3 respectively. DM_0 to DM_3 have a data input mask function, and are also sampled by DQS_0 to DQS_3 input signal together with input data.
During write cycle, DM_0 to DM_3 provide byte mask function. When DMx = High is latched by a DQS_0 to DQS_3 signal edge, data input at the same edge of DQS_0 to DQS_3 is masked.

During read cycle, all DM_0 to DM_3 are inactive and do not have any effect on read operation.
Refer to DM_0 to DM_3 TRUTH TABLE.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access and MB81P643287 read and write operations are burst oriented. The burst mode is implemented by keeping the same Row address and by automatic strobing Column address in every single clock edge till programmed burst length(BL). Access time of burst mode is specified as t_{ACC}. The internal column address counter operation is determined by a mode register which defines burst type(BT) and burst count length(BL) of 2, 4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 2, the following combinations will be required.

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	**Burst Stop Command (BST)**
		2nd Step	Write Command after l_{BSNC}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	1st Step	**Data Mask Input**
		2nd Step	Read Command after l_{WRD} from last data input
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	1st Step	**Data Mask Input**
		2nd Step	Precharge Command after l_{DPL} from last data input

The burst type is sequential only. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to the least significant address(= 0). If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode
2	X X 0	0 – 1
	X X 1	1 – 0
4	X 0 0	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0
	X 1 0	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6

BURST STOP COMMAND (BST)

The Burst Stop command (BST) terminates the burst read operation except for a case that Auto-precharge option is asserted. When the BST command is issued during the burst read operation, the all output buffers, DQs and DQS_0 to DQS_3, will turn to High-Z state after some latencies that to be matched with programmed CAS latency and internal bank state remains active state.
In a case of terminating the burst write operation, the BST command should not be issued at any time during burst write operation. Refer to previous page for the write interrupt and termination rule.

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

The DDR SDRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the precharge operation (PRE or PALL). With the precharge operation, DDR SDRAM will automatically be in standby state after specified precharge time (l_{RP}, l_{RPA}).
The precharged bank is selected by combination of AP and bank address (BA) when precharge command is issued. If AP = High, all banks are precharged regardless of BA (PALL command). If AP = Low, a bank to be selected by BA is precharged (PRE command).
The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command issue. This auto-precharge is entered by AP = High when a Read (READ) or Write (WRIT) command is issued.
Applying BST is illegal if the Auto-precharge option is used.
Refer to "■FUNCTION TRUTH TABLE".

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The MB81P643287 Auto-refresh command (REF) automatically generates Bank Active and Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be issued within every 8 µs period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh operation until cancelled by SELFX.
The Self-refresh mode is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once MB81P643287 enters the self-refresh mode, all inputs except for CKE can be either logic high or low level state and outputs will be in a High-Z state. During Self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELFX)

To exit Self-refresh mode, CKE must bring to High for at least 2 clock cycles together with NOP condition.
Refer to Timing Diagram for the detail procedure. It is recommended to issue at least one Auto-refresh command just after the l_{RFC} period to avoid the violation of refresh period.

WARNING: A stable clock for l_{SCD} period with a constant duty cycle must be supplied prior to applying any read command to insure the DLL is locked against the latest device conditions.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted both before the self-refresh entry and after the self-refresh exit.

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS Latency, and Test Mode Entry (This Test Mode Entry must not be used). Refer to MODE REGISTER TABLE.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all banks are in idle state and all DQS are in High-Z. The condition of the mode register is undefined after the power-up stage. It is required to set each field at power-up initialization.

Refer to POWER-UP INITIALIZATION below.

Note: The Extended Mode Register Set command (EMRS) and its DLL Enable function of EMRS field is only used at power-on sequence.

POWER-UP INITIALIZATION

The MB81P643287 internal condition at and after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply V_{DD} voltage to all V_{DD} pins before or at the same time as V_{DDQ} pins and attempt to maintain all input signals to be Low state (or at least CKE to be Low state).
2. Apply V_{DD} voltage to all V_{DDQ} pins before or at the same time as V_{REF} and V_{TT}.
3. Apply V_{REF} and V_{TT}. (V_{TT} is applied to the system).
4. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200 µs.
5. After the minimum of 200 µs stable power and clock, apply NOP condition and take CKE to be High state.
6. Issue Precharge All Banks (PALL) command or Precharge Single Bank (PRE) command to every banks.
7. Issue EMRS to enable DLL, DE = Low.
8. Issue Mode Register Set command (MRS) to reset DLL, DR = High. An additional clock input for I_{PCD}*[1] period is required to lock the DLL.
9. Apply minimum of two Auto-refresh command (REF).*[2]
10. Program the mode register by Mode Register Set command (MRS) with DR = Low.*[2]

*1: The I_{PCD} depends on operating clock period. The I_{PCD} is counted from “DLL Reset” at step-8 to any command input at step-10.

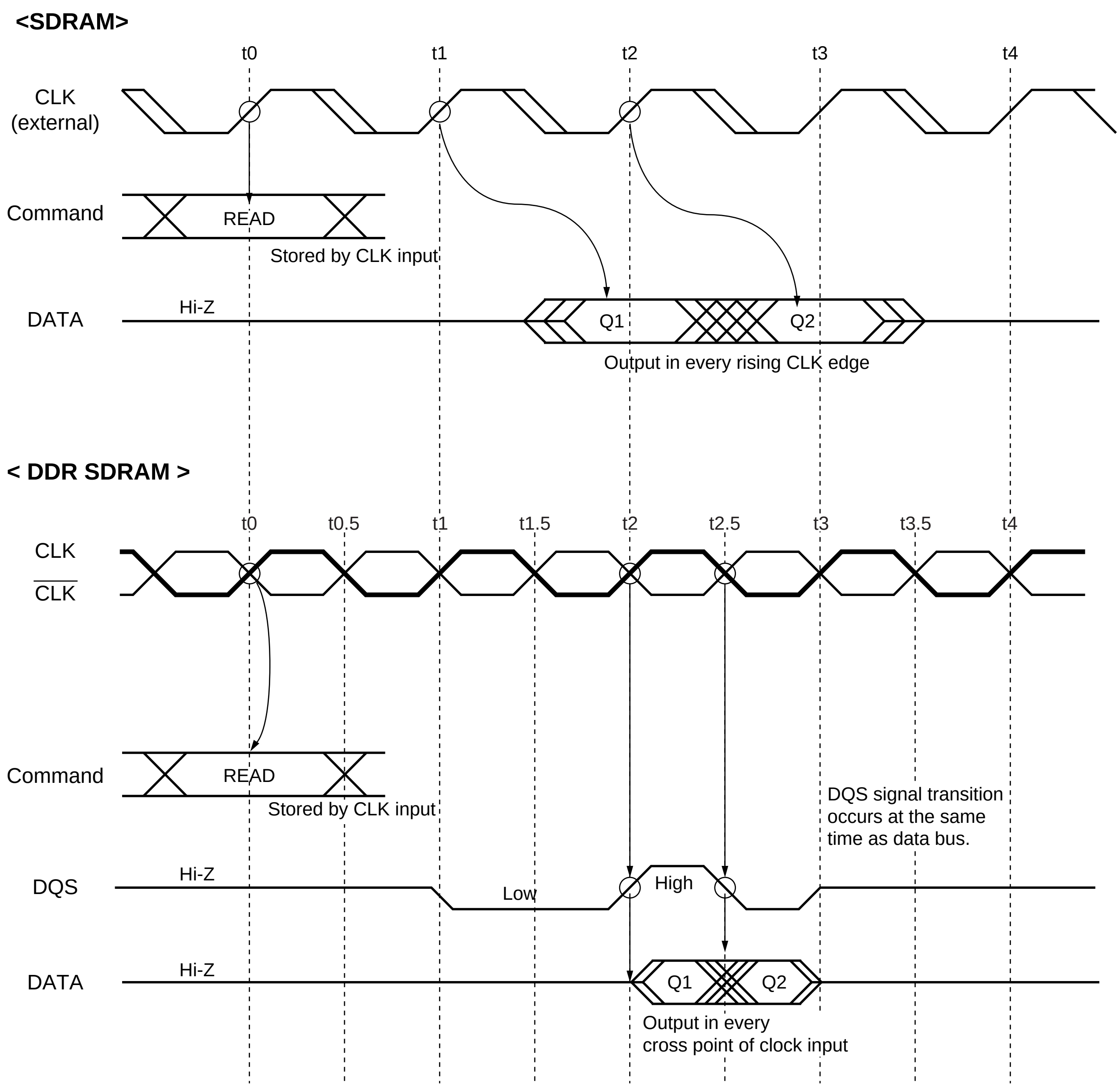
*2: The Mode Register Set command (MRS) can be issued before two Auto-refresh cycle.

POWER-DOWN

The MB81P643287 uses multiple power supply voltage. It is required to follow the reversed sequence of above Power On Sequence.

1. Take all input signals to be V_{SS} or High-Z.
2. Deapply V_{DDQ}.
3. Deapply V_{DD} at the same time as V_{DDQ}.

Fig. 3 - SDRAM READ TIMING EXAMPLE (@ CL=2 & BL=2)



■ MODE REGISTER TABLE

MODE REGISTER SET

ADDRESS	BA_2	BA_1	BA_0	A_{10}	A_9	A_8	A_7	A_6 to A_4	A_3	A_2 to A_0
REGISTER	0*1	0*1	0*1	0	0	DR	TE	CL	BT	BL

A_6	A_5	A_4	CAS Latency (CL)
0	0	X	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length (BL)
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	X	X	Reserved

A_7	Test Mode Entry (TE)
0	Normal Operation
1	Test Mode (Used for Supplier Test Mode)

A_3	Burst Type (BT)
0	Sequential (Wrap round, Binary up)
1	Reserved

A_8	DLL RESET (DR)
0	Normal Operation
1	RESET DLL

EXTENDED MODE REGISTER SET (Note *4)

ADDRESS	BA_2	BA_1	BA_0	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
EXTENDED MODE REGISTER	0*2	0*2	1*2	RESERVED *3										DE

A_0	DLL Enable (DE)
0	DLL Enable
1	DLL Disable

*1: A combination of $BA_2 = BA_1 = BA_0 = 0$ (Low) selects standard Mode Register.

*2: A combination of $BA_1 = BA_2 = 0$ and $BA_0 = 1$ (High) selects Extended Mode Register.

*3: These RESERVED field in EMRS must be set as 0.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}, V_{DDQ}	–0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	2.0	W
Storage Temperature	T_{STG}	–55 to +125	°C

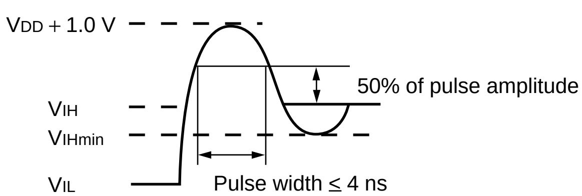
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

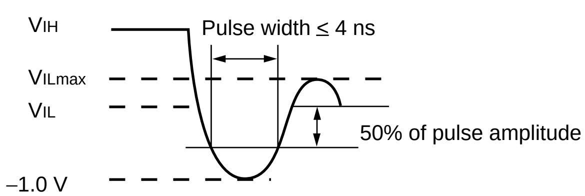
(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	2.3	2.5	2.7	V
		V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V
		V_{SS}, V_{SSQ}	0	0	0	V
Input Reference Voltage	*1	V_{REF}	$V_{DDQ} \times 0.49$	$V_{DDQ} \times 0.5$	$V_{DDQ} \times 0.51$	V
Termination Voltage	*2	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
Single Ended SSTL DC Level Input High Voltage	*3	$V_{IH\ (DC)}$	V_{REF} + 0.25	—	V_{DDQ} + 0.1	V
Single Ended SSTL DC Level Input Low Voltage	*3	$V_{IL\ (DC)}$	- 0.1	—	V_{REF} - 0.25	V
Single Ended SSTL AC Level Input High Voltage	*3, *5	$V_{IH\ (AC)}$	V_{REF} + 0.35	—	—	V
Single Ended SSTL AC Level Input Low Voltage	*3, *5	$V_{IL\ (AC)}$	—	—	V_{REF} - 0.35	V
Differential DC Level Input Voltage Range	*3	$V_{IN\ (DC)}$	- 0.1	—	V_{DDQ} + 0.1	V
Differential DC Level Differential Input Voltage	*3	$V_{SWING\ (DC)}$	0.5	—	V_{DDQ} + 0.2	V
Differential AC Level Differential Input Voltage	*3	$V_{SWING\ (AC)}$	0.7	—	—	V
Differential AC Level Input Crosspoint Voltage	*3	$V_{X\ (AC)}$	V_{DDQ}/2 - 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	V
Differential Input Signal Offset Voltage	*4	$V_{ISO\ (AC)}$	V_{DDQ}/2 - 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	V
Termination Resistor (SSTL I/Os)	*2	R_T	—	50	—	Ω
Ambient Temperature		T_A	0	—	70	°C

Note 5.



Note 6.



Notes: *1. V_{REF} is expected to track variations in the DC level of V_{DDQ} of the transmitting device. Peak-to-Peak noise level on V_{REF} may not exceed ± 2% of the supplied DC value.

*2. V_{TT} is used for SSTL_2 bus and is not applied to the device. V_{TT} is expected to be set equal to V_{REF} and must be track variations in the DC level of V_{REF}.

*3. Applicable when signal(s) is terminated to the V_{TT} of SSTL_2 bus.

*4. V_{ISO} means $\{V_{IN(CLK)} + V_{IN(\overline{CLK})}\} / 2$. Refer to Differential Input Signal Definition.

*5. Overshoot limit: V_{IH} (Max.) = V_{DD} + 1.0V for pulse width ≤ 4 ns acceptable, pulse width measured at 50% of pulse amplitude.

*6. Undershoot limit: V_{IL} (Min.) = V_{SS} -1.0V for pulse width ≤ 4 ns acceptable, pulse width measured at 50%of pulse amplitude.

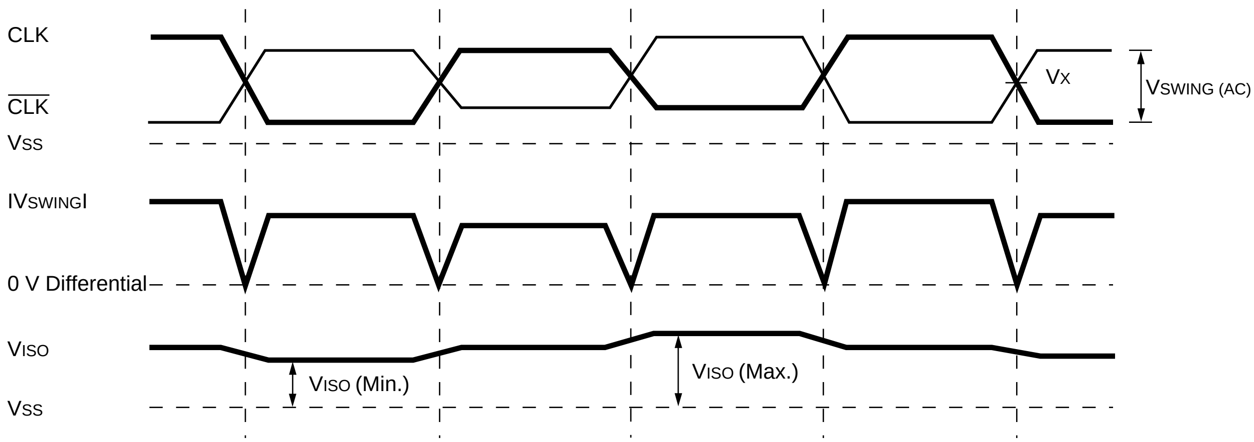
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Differential Input Signal Definition

Fig. 4 - Differential Input Signal Offset Voltage (For Clock Input)



■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Address & Control	C_{IN1}	2.5	—	3.5	pF
Input Capacitance, CLK & $\overline{CLK}$	C_{IN2}	2.5	—	3.5	pF
Input Capacitance, DM_0 to DM_3	C_{IN3}	4.0	—	5.5	pF
I/O Capacitance	$C_{I/O}$	4.0	—	5.5	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note *1,*2,*3

<table>
<tr><th colspan="2" rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Condition</th><th colspan="2">Value</th><th rowspan="2">Unit</th></tr>
<tr><th>Min.</th><th>Max.</th></tr>
<tr><td colspan="2">Output Minimum Source DC Current</td><td>$I_{OH(DC)}$</td><td>V_{DDQ} = 2.3V,
V_{OH} = V_{DDQ}-0.43V</td><td>-15.2</td><td>—</td><td>mA</td></tr>
<tr><td colspan="2">Output Minimum Sink DC Current</td><td>$I_{OL(DC)}$</td><td>V_{DDQ} = 2.3V,
V_{OL} = +0.35V</td><td>15.2</td><td>—</td><td>mA</td></tr>
<tr><td colspan="2">Input Leakage Current (any input)</td><td>I_{LI}</td><td>0 V ≤ V_{IN} ≤ V_{DD};
All other pins not under test = 0 V</td><td>-10</td><td>10</td><td>µA</td></tr>
<tr><td colspan="2">Output Leakage Current</td><td>I_{LO}</td><td>0 V ≤ V_{IN} ≤ V_{DD};
Data out disabled</td><td>-10</td><td>10</td><td>µA</td></tr>
<tr><td colspan="2">V_{REF} Current</td><td>I_{REF}</td><td></td><td>-10</td><td>10</td><td>µA</td></tr>
<tr><td rowspan="2">Operating Current
(Average Power
Supply Current)</td><td>MB81P643287-50</td><td rowspan="2">I_{DD1S}</td><td rowspan="2">Burst Length = 2
t_{CK} = Min.,
One bank active,
Address change up to 3 times during I_{RC} (Min.)
0 V ≤ V_{IN} ≤ V_{IL} (Max.),
V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}</td><td rowspan="2">—</td><td>460</td><td rowspan="2">mA</td></tr>
<tr><td>MB81P643287-60</td><td>405</td></tr>
<tr><td rowspan="2">Standby Current</td><td>MB81P643287-50</td><td rowspan="2">I_{DD2N}</td><td rowspan="2">CKE = V_{IH}, t_{CK} = Min.
All banks idle,
NOP commands only,
Input signals (except to CMD) are changed one time during 20 ns
0 V ≤ V_{IN} ≤ V_{IL} (Max.),
V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}</td><td rowspan="2">—</td><td>85</td><td rowspan="2">mA</td></tr>
<tr><td>MB81P643287-60</td><td>75</td></tr>
<tr><td colspan="2">Power Down Current</td><td>I_{DD2P}</td><td>CKE = V_{IL}, t_{CK} = Min.
All banks idle,
0 V ≤ V_{IN} ≤ V_{DD}</td><td>—</td><td>35</td><td>mA</td></tr>
<tr><td rowspan="2">Active Standby Current
(Power Supply Current)</td><td>MB81P643287-50</td><td rowspan="2">I_{DD3N}</td><td rowspan="2">CKE = V_{IH}, t_{CK} = Min.
All banks Active,
NOP commands only,
Input signals (except to CMD) are changed one time during 20 ns
0 V ≤ V_{IN} ≤ V_{IL} (Max.),
V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}</td><td rowspan="2">—</td><td>260</td><td rowspan="2">mA</td></tr>
<tr><td>MB81P643287-60</td><td>225</td></tr>
</table>

(Continued)

(Continued)

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Burst Read Current (Average Power Supply Current)	MB81P643287-50	I_{DD4R}	Burst Length = 4, CAS Latency = 3, All bank active, Gapless data, t_{CK} = Min., 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	535	mA
	MB81P643287-60				460	
Burst Write Current (Average Power Supply Current)	MB81P643287-50	I_{DD4W}	Burst Length = 4, CAS Latency = 3, All bank active, Gapless data, t_{CK} = Min., 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	595	mA
	MB81P643287-60				505	
Auto-refresh Current (Average Power Supply Current)	MB81P643287-50	I_{DD5}	Auto-refresh; t_{CK} = Min., 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	320	mA
	MB81P643287-60				270	
Self-refresh Current (Average Power Supply Current)		I_{DD6}	Self-refresh; CKE = V_{IL}, 0 V ≤ V_{IN} ≤ V_{DD}	—	5	mA

Notes: *1. All voltages referenced to V_{SS}.
*2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.
*3. I_{DD} depends on the output termination or load conditions, clock cycle rate, and number of address and command change within certain period. The specified values are obtained with the output open.

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note *1,*2,*3

AC PARAMETERS (CAS LATENCY DEPENDENT)

Parameter	Symbol		MB81P643287-50		MB81P643287-60		Unit
			Min.	Max.	Min.	Max.	
Clock Period	t_{CK}	CL = 3	5.0	9.0	6.0	10.5	ns
		CL = 2	7.5	10.5	9.0	10.5	

Parameter	Notes	Symbol	MB81P643287-50		MB81P643287-60		Unit
			Min.	Max.	Min.	Max.	
Input Setup Time (Except for DQS, DM and DQs)	*4	t_{IS}	1.0	—	1.2	—	ns
Input Hold Time (Except for DQS, DM and DQs)	*4	t_{IH}	1.0	—	1.2	—	ns
DM and Data Input Setup Time	*5	t_{DS}	0.6	—	0.7	—	ns
DM and Data Input Hold Time	*5	t_{DH}	0.6	—	0.7	—	ns
DQS First Input Setup Time (Input Preamble Setup Time)	*6	t_{DSPRES}	0	—	0	—	ns
Last Data Output to CKE High Level Hold Time		t_{QCKEH}	0	—	0	—	ns
Input Transition Time	*7	t_T	0.1	0.8	0.1	0.9	ns
Precharge Power Down Exit and Self-refresh Exit Time	*4	t_{PDEX}	3.0	—	3.6	—	ns
Time between Refresh	*8	t_{REF}	—	32	—	32	ms
Time between Auto-refresh Command	*8	t_{AREF}	—	8.0	—	8.0	µs
Pause Time after Power-on		t_{PAUSE}	200	—	200	—	µs

AC PARAMETERS (FREQUENCY DEPENDANT) Note *9

Parameter	Notes	Symbol	Min.	Max.	Unit
Clock High Time	*4	t_{CH}	$0.45 \times t_{CK}$	—	ns
Clock Low Time	*4	t_{CL}	$0.45 \times t_{CK}$	—	ns
DQS Low to High Input Transition Setup Time from CLK	*4, *10	t_{DQSS}	$0.75 \times t_{CK}$	$1.25 \times t_{CK}$	ns
DQS Low Input Pulse Width		t_{DSL}	$0.4 \times t_{CK}$	—	ns
DQS High Input Pulse Width		t_{DSH}	$0.4 \times t_{CK}$	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	*4	t_{DSPREH}	$0.25 \times t_{CK}$	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)		t_{DSPRE}	$0.4 \times t_{CK}$	—	ns
DQS Last Low Input Hold Time (Input Postamble Hold Time)		t_{DSPST}	$0.4 \times t_{CK}$	—	ns
DQS Access Time from Clock	*4	t_{QSCK}	$- 0.1 \times t_{CK} - 0.2$	$0.1 \times t_{CK} + 0.2$	ns
DQS Output Valid Time		t_{QSV}	$0.3 \times t_{CK}$	—	ns
DQS Output in Low-Z (Output Preamble Setup Time)	*4, *11	t_{QSLZ}	$- 0.1 \times t_{CK} - 0.2$	—	ns
DQS First Low Output Hold Time (Output Preamble Hold Time)	*4	t_{QSPRE}	$0.9 \times t_{CK} - 0.2$	$1.1 \times t_{CK} + 0.2$	ns
DQS Last Low Output Hold Time (Output Postamble Hold Time)	*4, *12	t_{QSPST}	$0.4 \times t_{CK} - 0.2$	$0.6 \times t_{CK} + 0.2$	ns
DQS Last Low Output in High-Z from CLK or $\overline{\text{CLK}}$	*12	t_{QSHZ}	—	$0.1 \times t_{CK} + 0.2$	ns
DQ Access Time from CLK & $\overline{\text{CLK}}$	*4	t_{ACC}	$- 0.1 \times t_{CK} - 0.2$	$0.1 \times t_{CK} + 0.2$	ns
DQ Access Time from DQS	*5	t_{QSQ}	$- 0.1 \times t_{CK}$	$0.1 \times t_{CK}$	ns
DQ Output Data Valid Time from DQS		t_{DV}	$0.3 \times t_{CK}$	—	ns
DQ Output in Low-Z	*4, *11	t_{LZ}	$- 0.1 \times t_{CK} - 0.2$	—	ns
DQ Output in High-Z	*4, *12	t_{HZ}	$- 0.1 \times t_{CK} - 0.2$	$0.1 \times t_{CK} + 0.2$	ns
DQ & DM Input Pulse Width		t_{DIPW}	$0.4 \times t_{CK}$	—	ns
DQS Falling Edge to Clock Hold Time		t_{DSCH}	$0.2 \times t_{CK}$ (1.5 ns Min.)	—	ns
DQS Falling Edge to Clock Setup Time		t_{DSCS}	$0.2 \times t_{CK}$ (1.5 ns Min.)	—	ns

EXAMPLE OF FREQUENCY DEPENDANT AC PARAMETERS (@ Minimum t_{CK})

Parameter	Symbol	t_{CK} = 5ns		t_{CK} = 6ns		t_{CK} = 7.5ns		t_{CK} = 9ns		t_{CK} = 10.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock High Time	t_{CH}	2.3	—	2.7	—	3.4	—	4.1	—	4.8	—	ns
Clock Low Time	t_{CL}	2.3	—	2.7	—	3.4	—	4.1	—	4.8	—	ns
DQS Low to High Input Transition Setup Time from CLK	t_{DQSS}	3.8	6.3	4.5	7.5	5.7	9.4	6.8	11.3	7.9	13.2	ns
DQS Low Input Pulse Width	t_{DSL}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS High Input Pulse Width	t_{DSH}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	t_{DSPREH}	1.3	—	1.5	—	1.9	—	2.3	—	2.7	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)	t_{DSPRE}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Last Low Input Hold Time (Postamble Hold Time)	t_{DSPST}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Access Time from Clock	t_{QSCK}	-0.7	0.7	-0.8	0.8	-1.0	1.0	-1.1	1.1	-1.3	1.3	ns
DQS Output Valid Time	t_{QSV}	1.5	—	1.8	—	2.3	—	2.7	—	3.2	—	ns
DQS Output in Low-Z (Output Preamble)	t_{QSLZ}	-0.7	—	-0.8	—	-1.0	—	-1.1	—	-1.3	—	ns
DQS First Low Output Hold Time (Output Preamble)	t_{QSPRE}	4.3	5.7	5.2	6.8	6.6	8.5	7.9	10.1	9.3	11.8	ns
DQS Last Low Output Hold Time (Output Postamble)	t_{QSPST}	1.8	3.2	2.2	3.8	2.8	4.7	3.4	5.6	4.0	6.5	ns
DQS Last Low Output in High-Z from CLK or $\overline{CLK}$	t_{QSHZ}	—	0.7	—	0.8	—	1.0	—	1.1	—	1.3	ns
DQ Output Access Time from CLK & $\overline{CLK}$	t_{ACC}	-0.7	0.7	-0.8	0.8	-1.0	1.0	-1.1	1.1	-1.3	1.3	ns
DQ Output Access Time from DQS	t_{QSQ}	-0.5	0.5	-0.6	0.6	-0.8	0.8	-0.9	0.9	-1.1	1.1	ns
DQ Output Data Valid Time from DQS	t_{DV}	1.5	—	1.8	—	2.3	—	2.7	—	3.2	—	ns
DQ Output in Low-Z	t_{LZ}	-0.7	—	-0.8	—	-1.0	—	-1.1	—	-1.3	—	ns
DQ Output in High-Z	t_{HZ}	-0.7	0.7	-0.8	0.8	-1.0	1.0	-1.1	1.1	-1.3	1.3	ns
DQ & DM Input Pulse Width	t_{DIPW}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Falling Edge to Clock Hold Time	t_{DSCH}	1.5	—	1.5	—	1.5	—	1.8	—	2.1	—	ns
DQS Falling Edge to Clock Setup Time	t_{DSCS}	1.5	—	1.5	—	1.5	—	1.8	—	2.1	—	ns

LATENCY

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81P643287-50		MB81P643287-60		Unit
			Min.	Max.	Min.	Max.	
$\overline{RAS}$ Cycle Time *13	CL = 3	l_{RC}	6	—	6	—	t_{CK}
	CL = 2		5	—	5	—	t_{CK}
$\overline{RAS}$ Active Time	CL = 3	l_{RAS}	4	11000	4	11000	t_{CK}
	CL = 2		3	7333	3	7333	t_{CK}
$\overline{RAS}$ Precharge Time		l_{RP}	2	—	2	—	t_{CK}
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	CL = 3	l_{RCD}	3	—	3	—	t_{CK}
	CL = 2		2	—	2	—	t_{CK}
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		l_{RRD}	1	—	1	—	t_{CK}
Precharge All Bank to Active	CL = 3	l_{RPA}	4	—	4	—	t_{CK}
	CL = 2		3	—	3	—	t_{CK}
Read Command to Write Command Delay	CL = 3	l_{RWD}	BL/2+3	—	BL/2+3	—	t_{CK}
	CL = 2		BL/2+2	—	BL/2+2	—	t_{CK}
Last Input Data to Read Command Delay	*14	l_{WRD}	2.5	—	2.5	—	t_{CK}
Last Input Data to Precharge Command Lead Time	*14	l_{DPL}	2.5	—	2.5	—	t_{CK}
Write with Auto Precharge Command to Active command Delay	*14	l_{WAL}	BL/2+3+l_{RP}	—	BL/2+3+l_{RP}	—	t_{CK}
Mode Register Access to Next Command Input Delay		l_{MRD}	2	—	2	—	t_{CK}
$\overline{CAS}$ to $\overline{CAS}$ Delay		l_{CCD}	1	—	1	—	t_{CK}
$\overline{CAS}$ Bank Delay		l_{CBD}	1	—	1	—	t_{CK}
Precharge Power Down Exit to Next Command Input Delay		l_{PDEXP}	2	—	2	—	t_{CK}
Minimum Stable Clock Input After Self-refresh Exit Before READ Command Input	*15	l_{SCD}	400	—	400	—	t_{CK}
Minimum Stable Clock Input After Self-refresh Exit Before non-READ Command Input		l_{XSNR}	12	—	12	—	t_{CK}
Minimum Stable Clock Input for DLL Lock-on in Power-up Initialization sequence. *16	$t_{CK} \leq 7.5$ns	l_{PCD}	400	—	400	—	t_{CK}
	$t_{CK} \leq 10.5$ns		630	—	630	—	t_{CK}
Auto-refresh Cycle Time		l_{RFC}	12	—	12	—	t_{CK}

LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81P643287-50	MB81P643287-60	Unit
BST Command to Output in High-Z	CL = 3	l_{BSH}	3	3	t_{CK}
	CL = 2		2	2	t_{CK}
BST Command to New Command Input *17	CL = 3	l_{BSNC}	3	3	t_{CK}
	CL = 2		2	2	t_{CK}
DM to Input Data Delay		l_{DQD}	0	0	t_{CK}
Precharge to Output in High-Z	CL = 3	l_{ROH}	3	3	t_{CK}
	CL = 2		2	2	t_{CK}
CKE Low to Command/Address Input Inactive		l_{CKE}	1	1	t_{CK}

Notes: *1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure and stable clock input with constant clock period and with 50% duty cycle.

*2. Access Times assume input slew rate of 1ns/volt between V_{REF}+0.35V to V_{REF}-0.35V, where V_{REF} is V_{DDQ}/2, with SSTL_2 output load conditions. Refer to AC TEST LOAD CIRCUIT.

*3. V_{REF} = 1.25V is a typical reference level for measuring timing of input signals.
Transition times are measured between V_{IH}(Min.) and V_{IL}(Max.) unless otherwise noted.
Refer to AC TEST CONDITIONS.

*4. This parameter is measured from the cross point of CLK and $\overline{\text{CLK}}$ input.

*5. This parameter is measured from signal transition point of DQS_0 to DQS_3 input crossing V_{REF} level.

*6. The specific requirement is that DQS be valid (HIGH or LOW) on or before this CLK edge. The case shown (DQS going from High-Z to logic LOW) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be HIGH at this time, depending on t_{DSS}.

*7. t_T is defined as the transition time between $V_{IH\ (AC)}$(Min.) and $V_{IL\ (AC)}$(Max.).

*8. Total of 4096 REF command must be issued within t_{REF} (Max.). t_{AREF} is a reference value for distributed refresh and specifies the time between one REF command to next REF command except for a condition where CKE = Low during Self-refresh mode.

*9. This parameter is scalable by actual clock period (t_{CK}) and affected by an abrupt change of duty cycle, jitters on clock input, T_A and level of V_{DD} and V_{DDQ}.The internal DLL circuit can adjust delay time against the change of following condition :

$T_A \leq 0.1\ °C$ / 20 ns,
$V_{DD} \leq 1$ mV / 10 ns,
$V_{DDQ} \leq 1$ mV / 10 ns,

if change rate is bigger than these values, frequency dependent AC parameters affected by DLL jitters.

*10. More than 2 signal edge of DQS_0 to DQS_3 should not be input within 1 clock (t_{CK}) cycle.

*11. Low-Z (Low Impedance State) is specified and measured at $V_{TT} \pm$ 200mV.

*12. t_{QSPST}, t_{QSHZ} and t_{HZ} are specified where output buffer is no longer driven.

*13. Actual clock count of l_{RC} will be sum of clock count of l_{RAS} and l_{RP}.

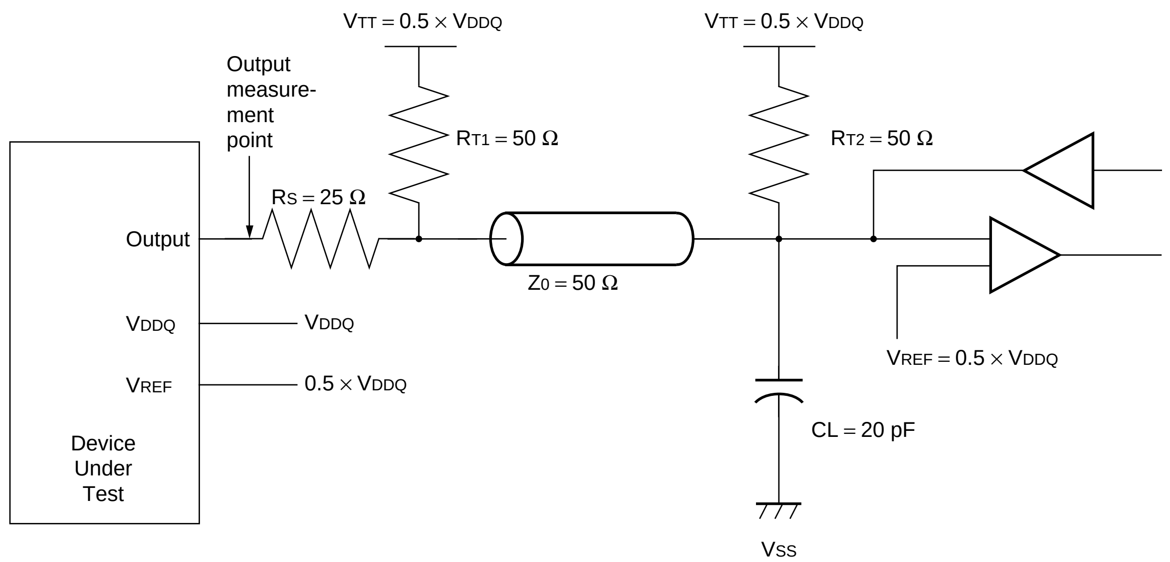
*14. Assume $t_{DQSS} = 1 \times t_{CK}$. If actual t_{DQSS} is within specified minimum and maximum range, those parameters can be assumed $t_{DQSS} = 1 \times t_{CK}$.

*15. Applicable also if device operating conditions such as supply voltages, case temperature, and/or clock frequency (t_{CK} difference must be 0.2 ns or less) is changed during any operation.

*16. Clock period must satisfy specified t_{CK} and it must be stable.

*17. Assume BST is effective to read operation (issued prior to the end of burst read).

Fig. 5 - AC TEST LOAD CIRCUIT (SSTL_2, Class II)



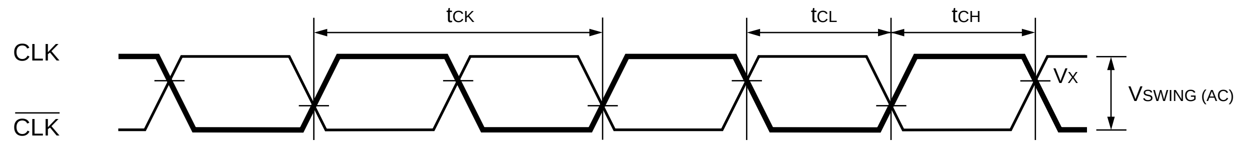
Note: AC characteristics are measured in this condition. This load circuit is not applicable for DC Test.

AC TEST CONDITIONS

Parameters	Symbol	Value	Unit
Single-end Input			
Input High Level	V_{IH}	$V_{REF} + 0.35$	V
Input Low Level	V_{IL}	$V_{REF} - 0.35$	V
Input Reference Level	V_{REF}	$V_{DDQ} / 2$	V
Input Slew Rate	SLEW	1.0	V/ns
Differential Input (CLK and $\overline{\text{CLK}}$)			
Input Reference Level	Vr	$V_{X\,(AC)}$*	V
Input Level	V_{SWING}	0.7	V
Input Slew Rate	SLEW	1.0	V/ns

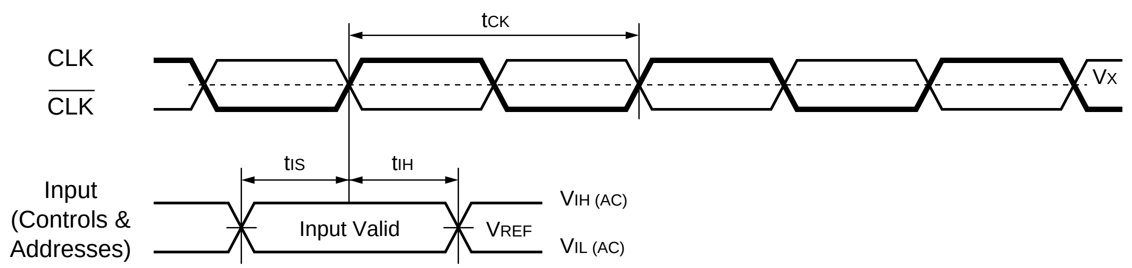
* : V_X means the actual cross point between CLK and $\overline{\text{CLK}}$ input.

Fig. 6 - AC TIMING of CLK & $\overline{\text{CLK}}$



Note: Reference level for AC timings of clock are the cross point of CLK and $\overline{\text{CLK}}$ as specified in V_X.

Fig. 7 - AC TIMING of Command Input & Address



Note: The cross point of CLK and $\overline{\text{CLK}}$ (V_X) is used for command and address input.
The reference level of single ended input is V_{REF}.

Fig. 8 - AC TIMING of Write Mode (Data Strobe, Write Data and Data Mask Input)

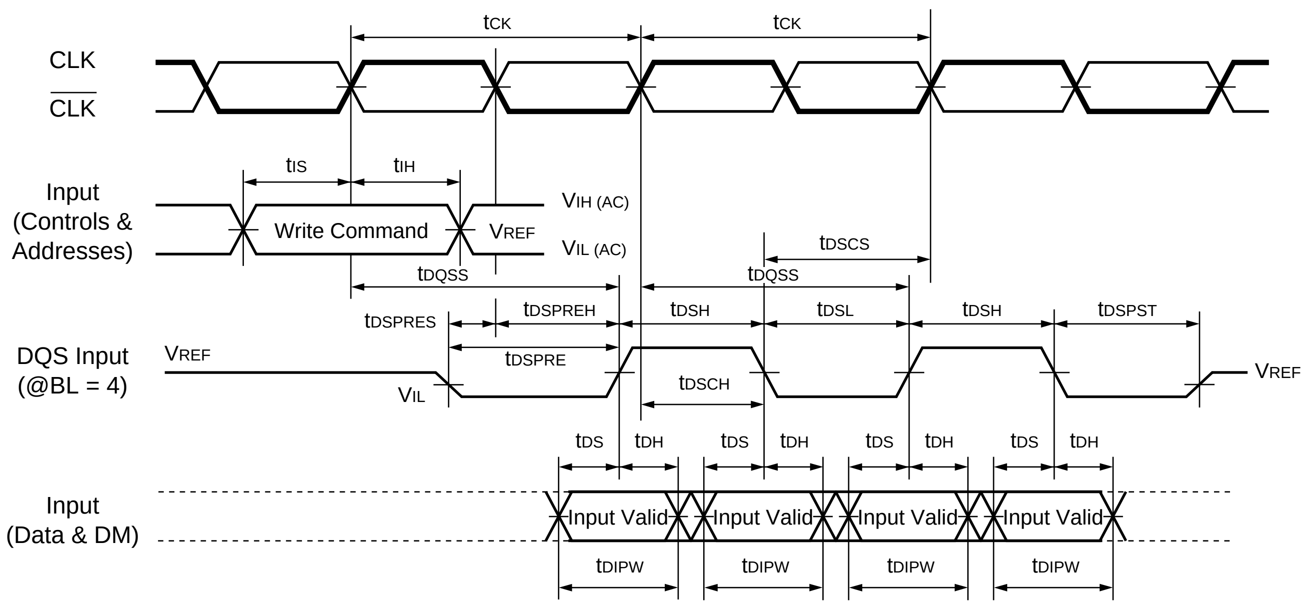
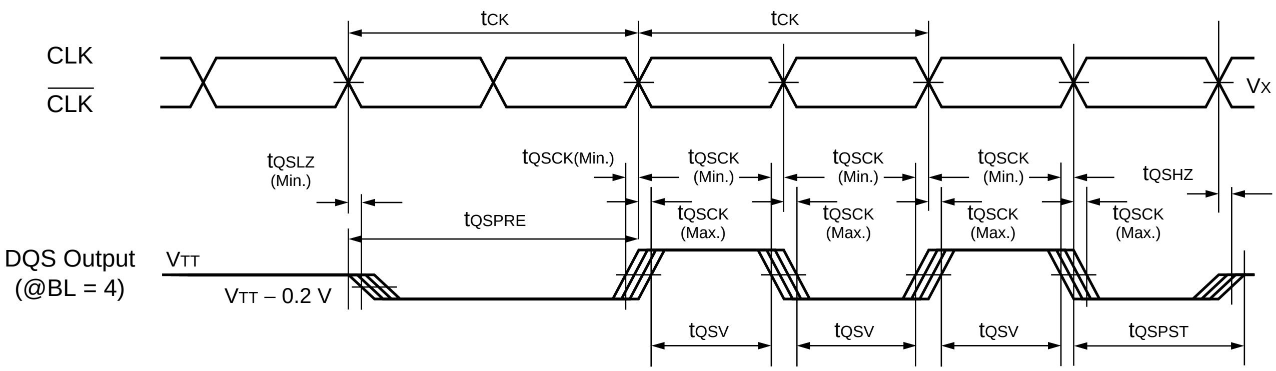
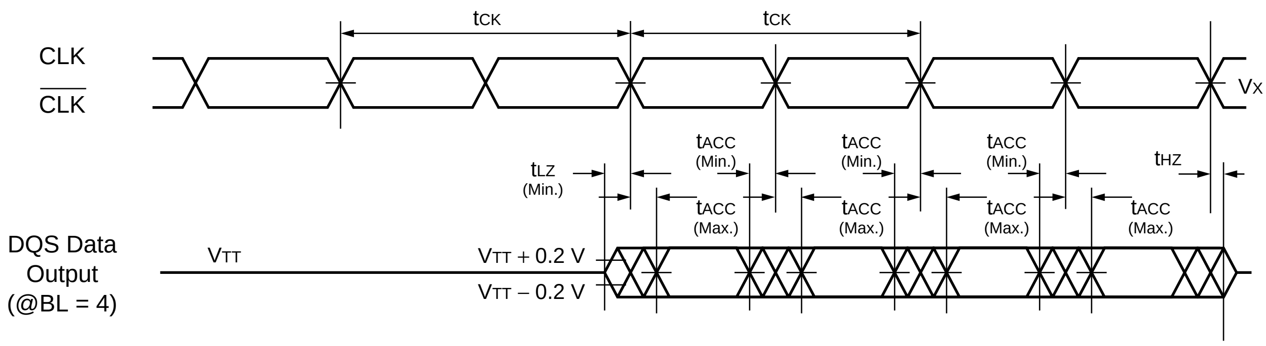


Fig. 9 - AC TIMING of Read Mode (Clock to DQS Output Delay Time)



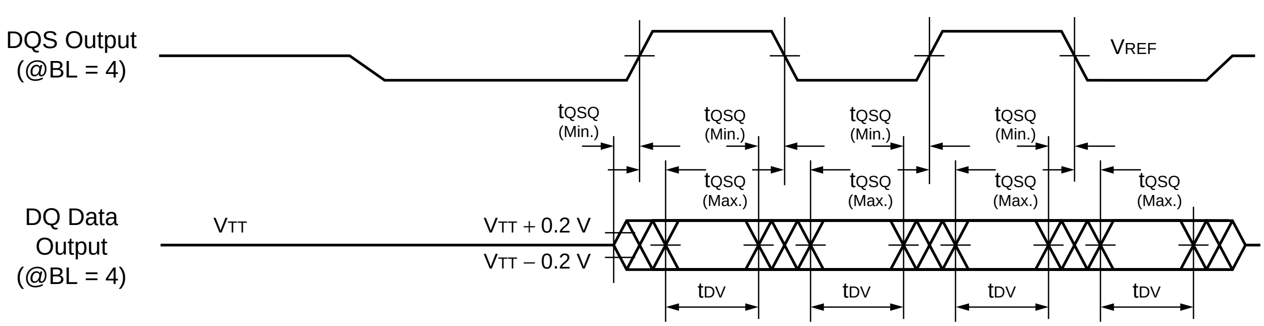
Note: DQS Access time (t_{QSCK}) is measured from the cross point of clock (V_X) and V_{REF}.
The end of t_{QSPST} and t_{QSHZ} specification is defined at where output buffer is no longer driven.

Fig. 10 - AC TIMING of Read Mode (Clock to Data Output Delay Time)



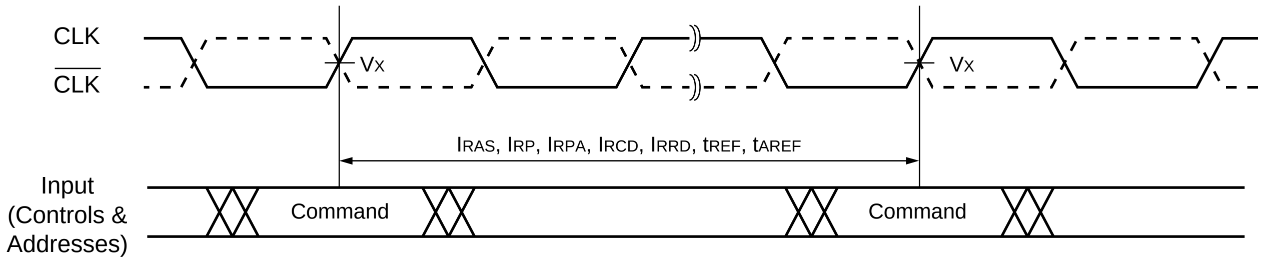
Note: Access time (t_{ACC}) is measured from the cross point of clock (V_X) and V_{REF}.
The end of t_{HZ} specification is defined at where output buffer is no longer driven.

Fig. 11 - AC TIMING of Read Mode (DQS Output to Data Output Delay Time)



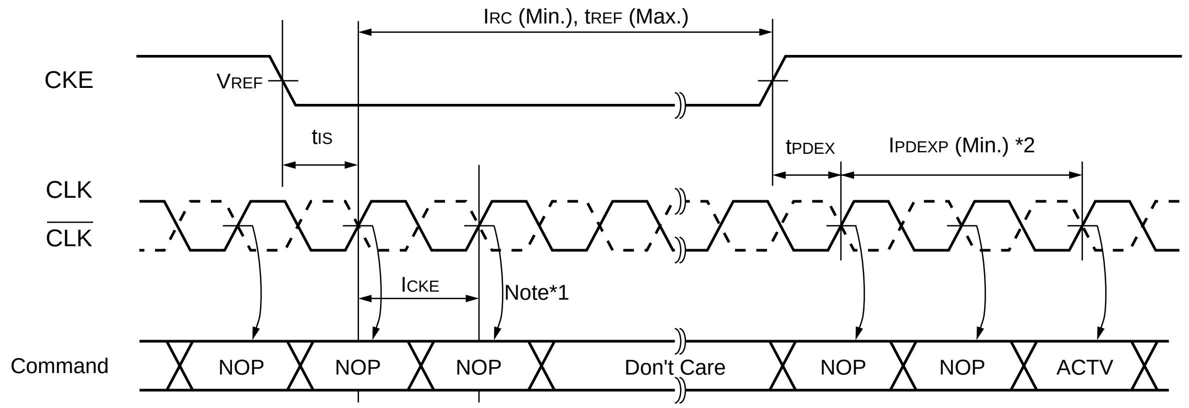
Note: DQS Output Edge to Data Output Edge Skew Time (t_{QSQ}) is measured from V_{TT} to V_{TT}.

Fig. 12 - AC TIMING, PULSE WIDTH



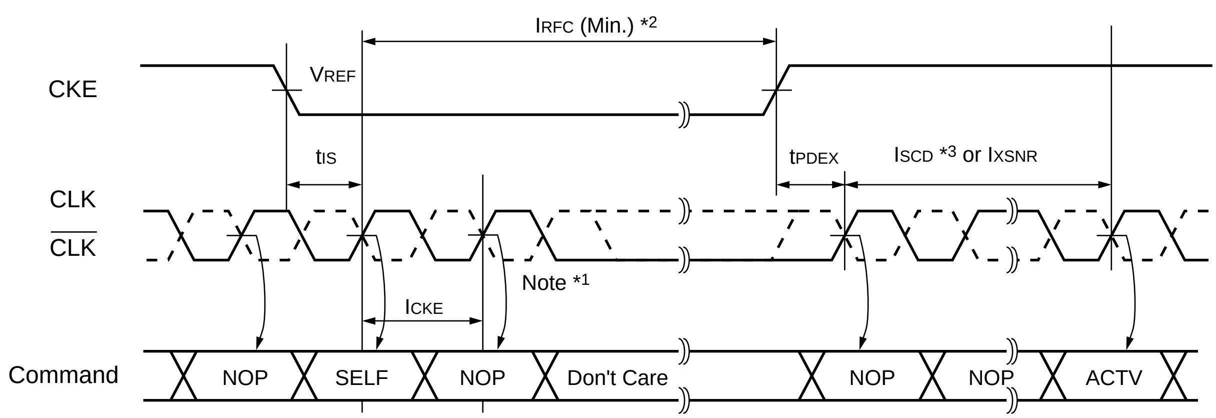
Note: All parameters listed above are measured from the cross point at rising edge of the CLK and falling edge of $\overline{\text{CLK}}$ of one command input to next command input.

Fig. 13 - AC TIMING of Precharge Power Down Mode



Notes: *1. Minimum 2 clock cycles is required for complete power down on clock buffer.
*2. If either any supply voltage or clock input condition is changed from the previous operating condition (other than PDEN and REF), l_{SCD} must be satisfied prior to any command input.

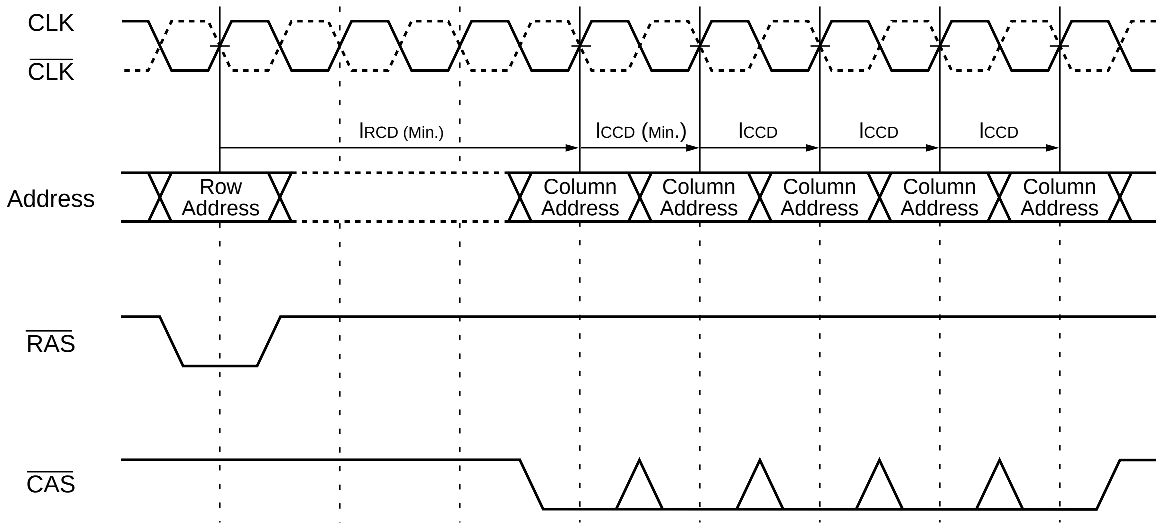
Fig. 14 - AC TIMING of Self-refresh Mode



Notes: *1. Minimum 2 clock cycles is required for complete power down on clock buffer.
*2. CKE must maintain High level and clock must be provided during the l_{SCD} period. l_{SCD} must be satisfied before read command input.
*3. l_{SCD} must be satisfied before read command input.

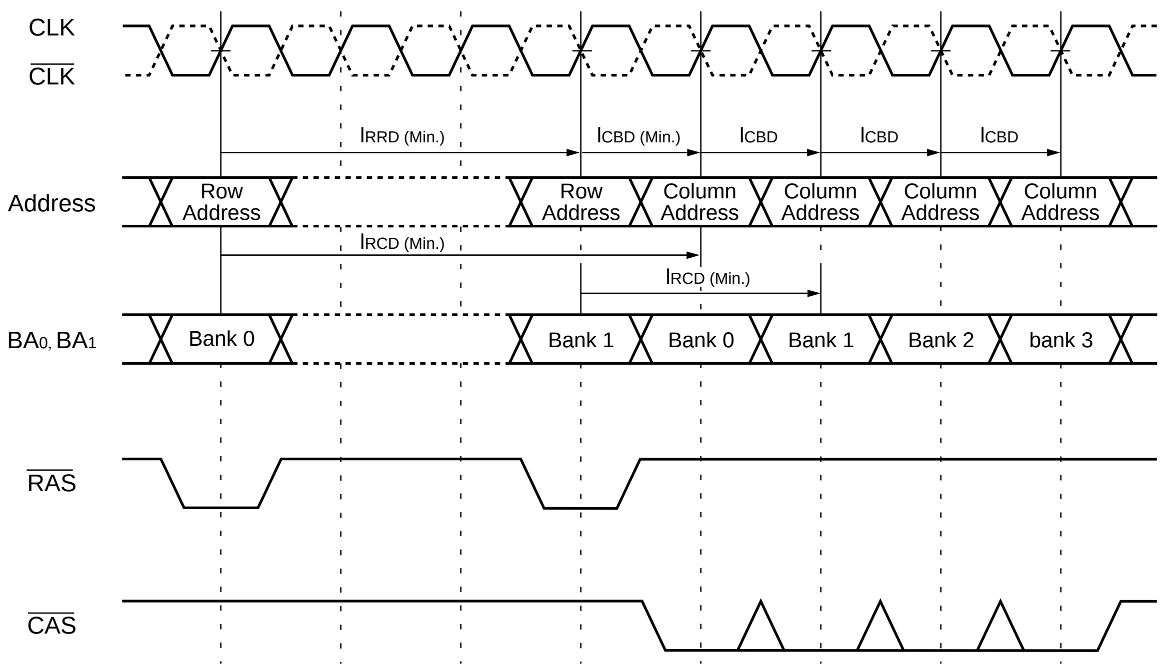
■ TIMING DIAGRAMS

TIMING DIAGRAM - 1: COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY

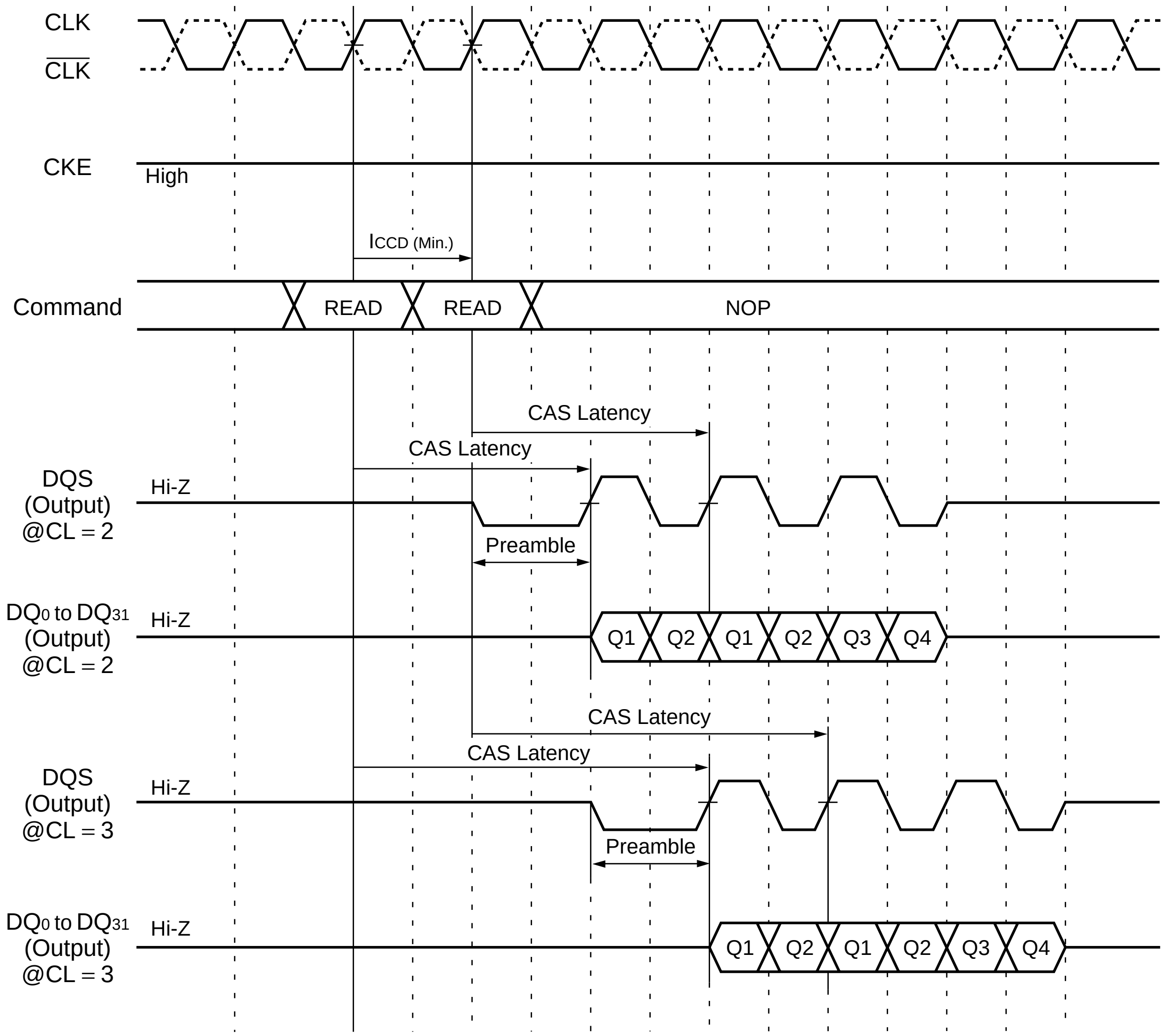


Note: lCCD, CAS to CAS address delay, is applicable to the same bank access and it can be one or more clock period.

TIMING DIAGRAM - 2: DIFFERENT BANK ADDRESS INPUT DELAY

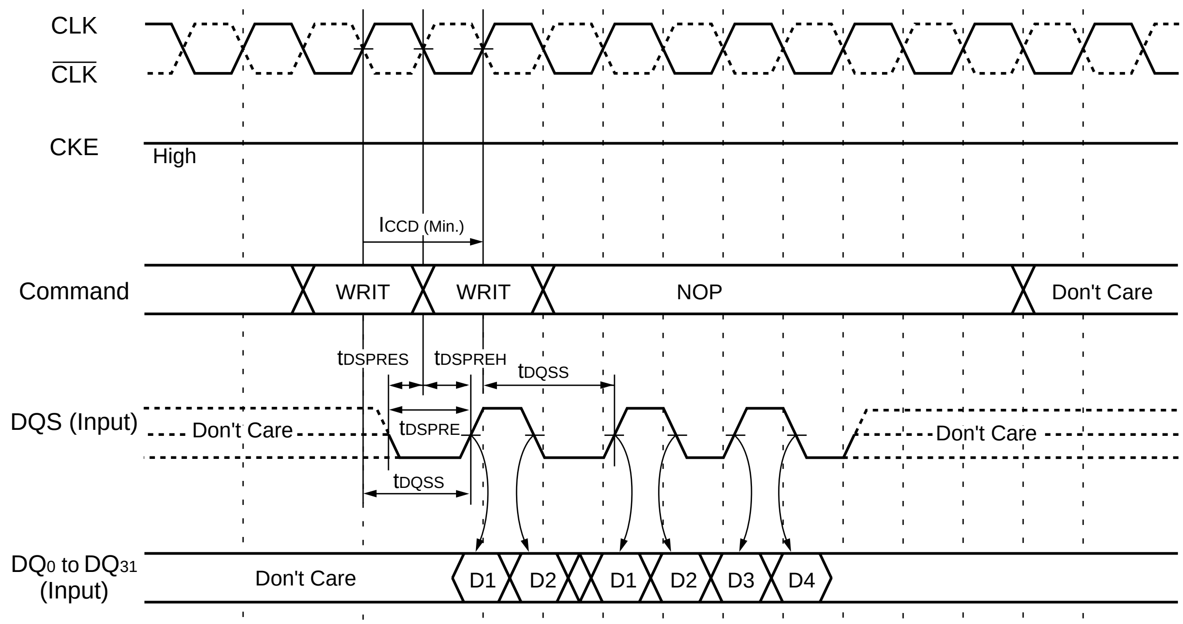


TIMING DIAGRAM - 3: READ (EXAMPLE @ BL = 4)



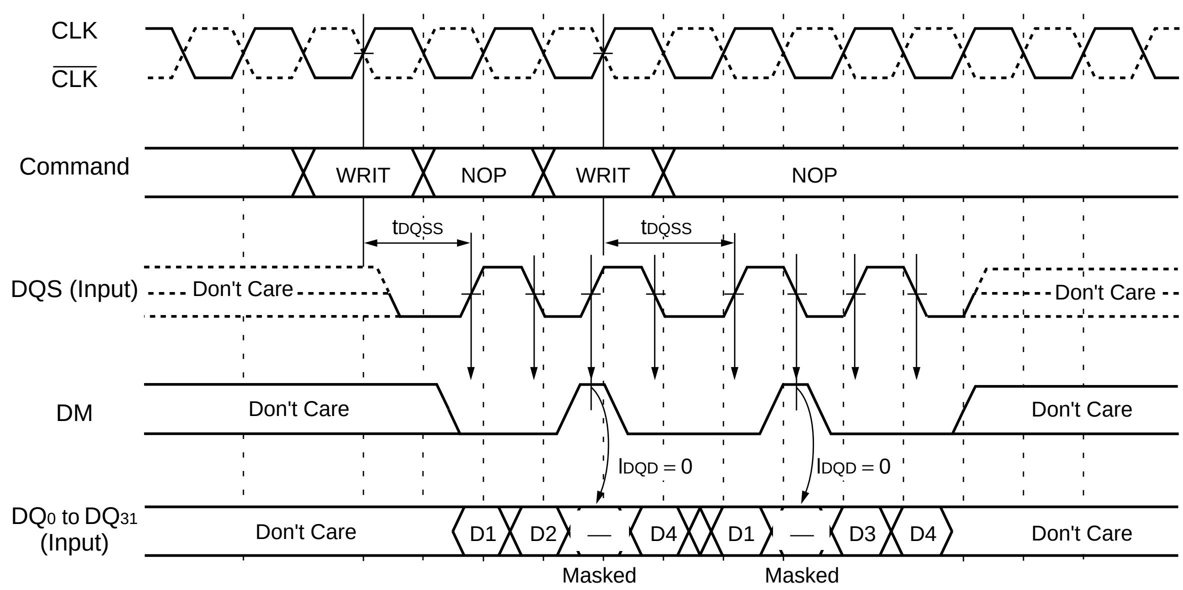
Note: CAS Latency is defined from Read command to first rising edge of DQS_0 to DQS_3 output.
Preamble is $1 \times t_{CK}$ length and starts driving Low level.

TIMING DIAGRAM - 4: WRITE (EXAMPLE @ BL = 4)



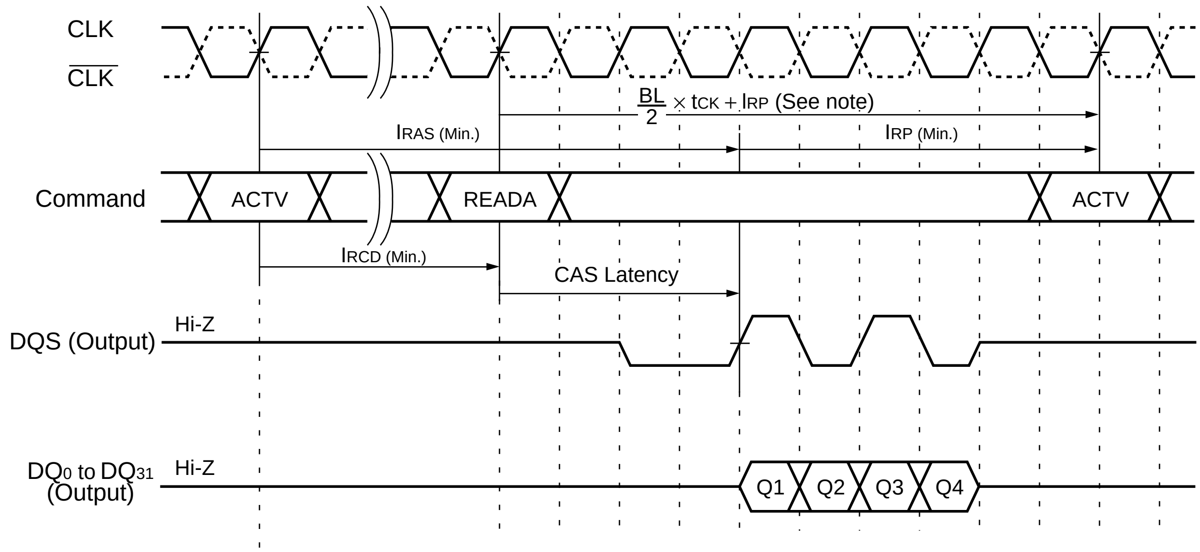
Note: DQS Setup Time, t_{DQSS}, must be within a range of 0.75*t_{CK} to 1.25*t_{CK} from write command Input.

TIMING DIAGRAM - 5: DM, WRITE DATA MASK (EXAMPLE @ BL = 4)



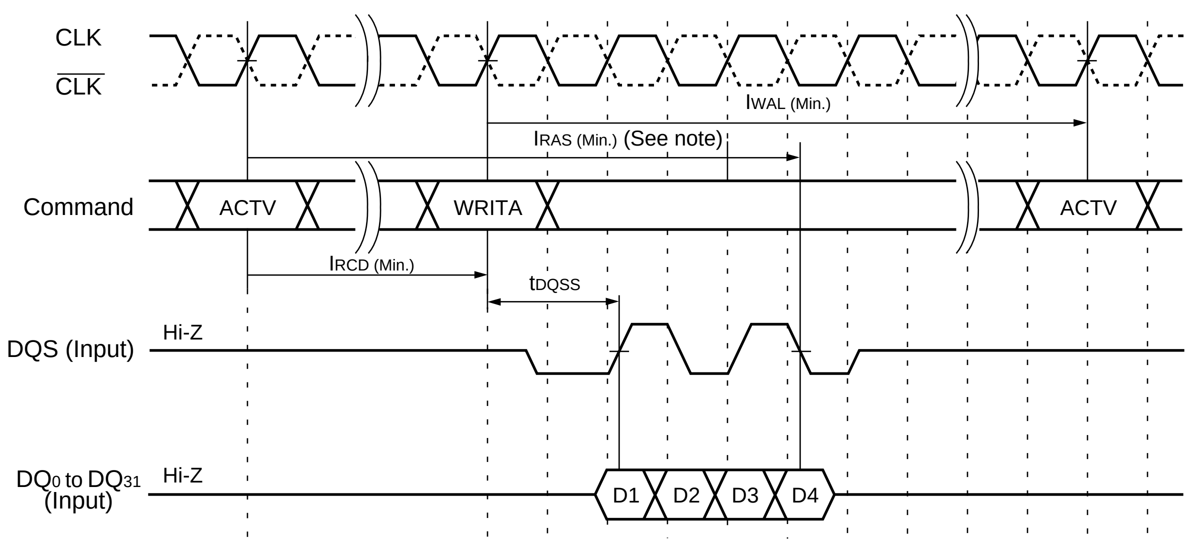
Note: DM are latched by DQS Input together with Data Input after write command.

TIMING DIAGRAM - 6: READ WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4 Applied to same bank)



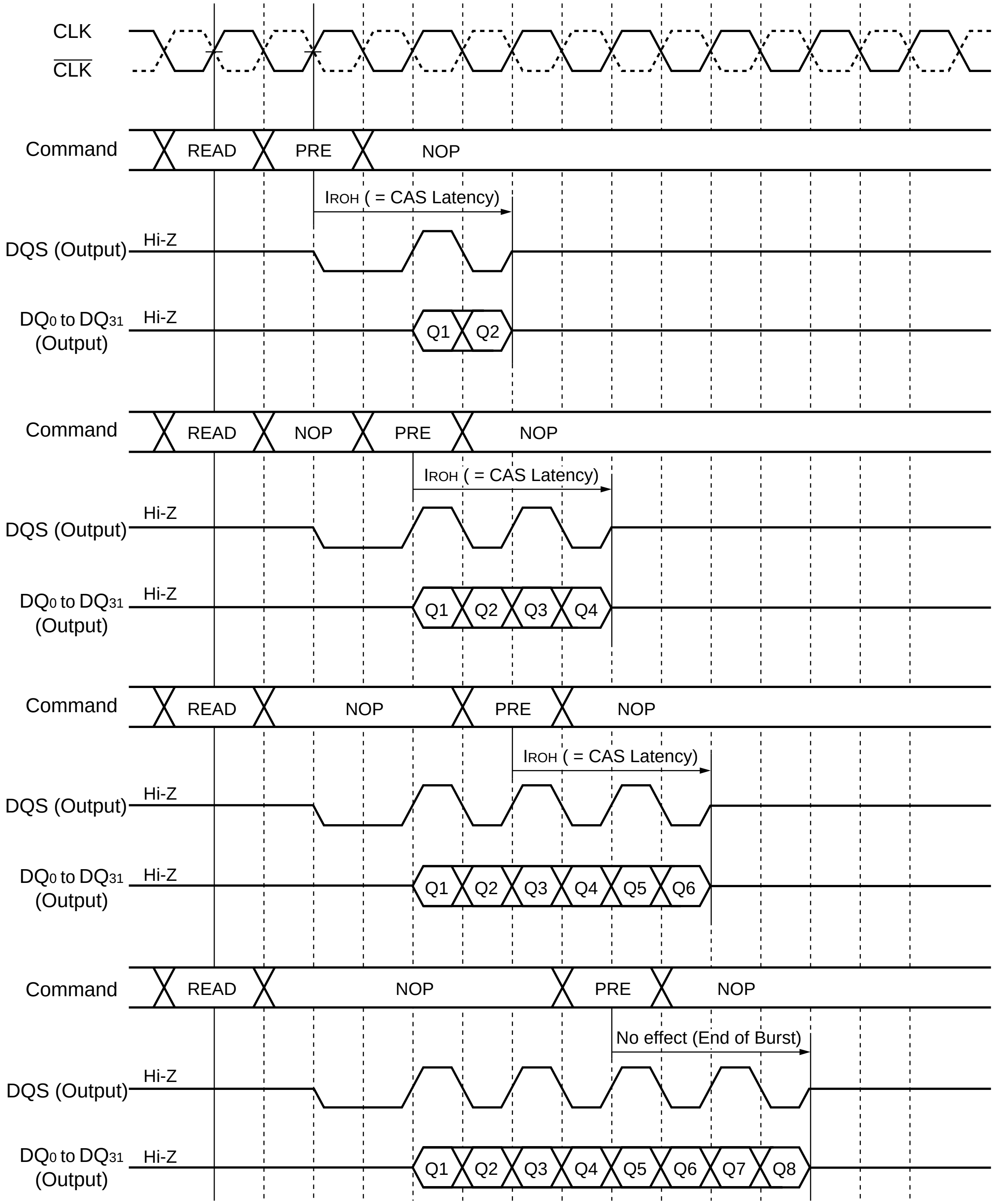
Note: Internal precharge operation at Read with Auto-precharge command (READA) is started BL/2 clock later from READA command.
If BL=2, the READA command should not be issued no earlier than 1 clock (BL/2 = 1) before l_{RAS} (Min.).
If BL=4, the READA command should not be issued no earlier than 2 clock (BL/2=2) before l_{RAS} (Min.).

TIMING DIAGRAM - 7: WRITE WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4 Applied to same bank)



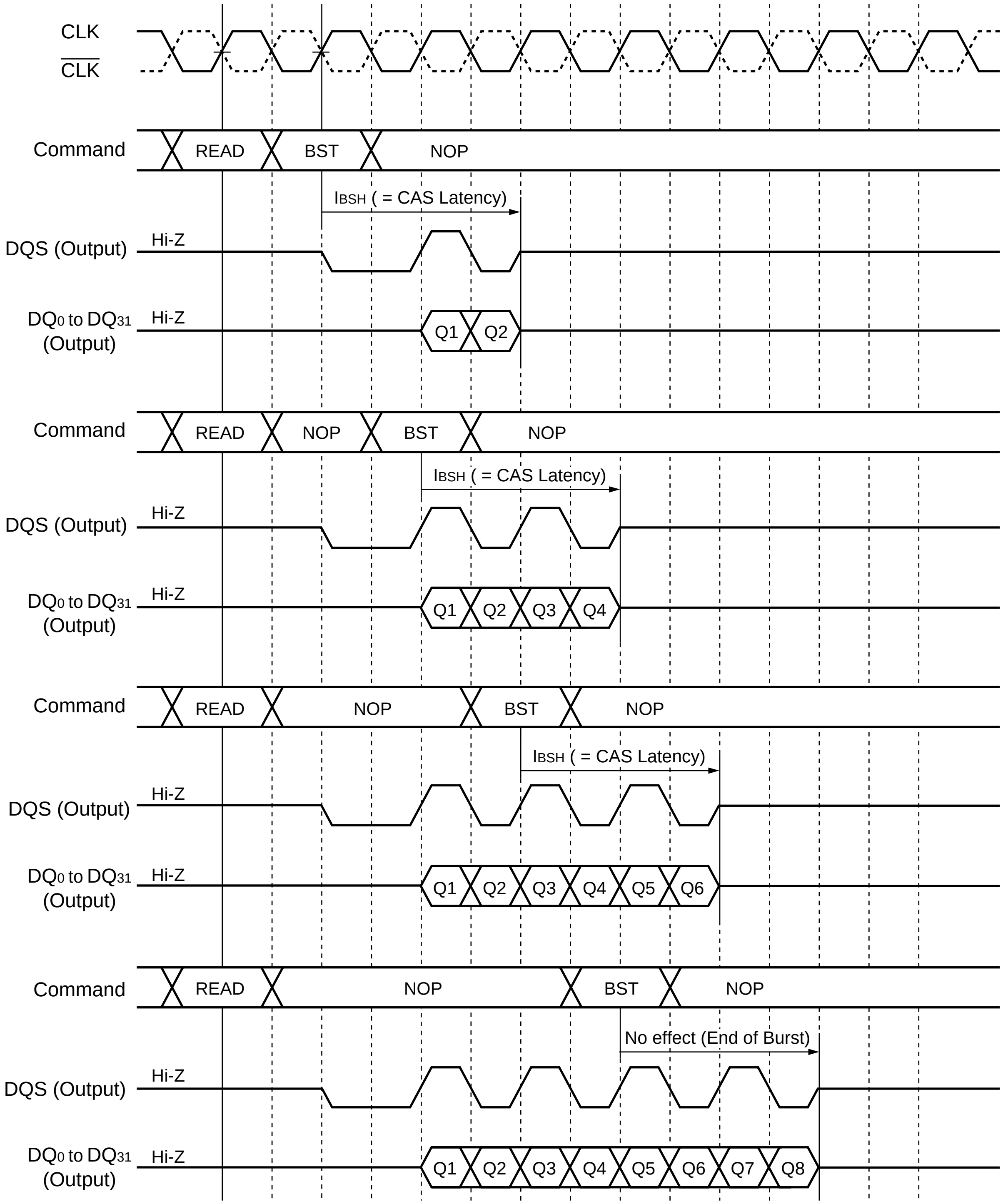
Note: Write with Auto-precharge command (WRITA) must be issued after l_{RCD} is satisfied and be considered to meet l_{RAS} requirement applied to end of burst length (BL) regardless of where it is masked or not.

**TIMING DIAGRAM - 8: READ INTERRUPTED BY PRECHARGE
(EXAMPLE @ CL = 2, BL = 8)**



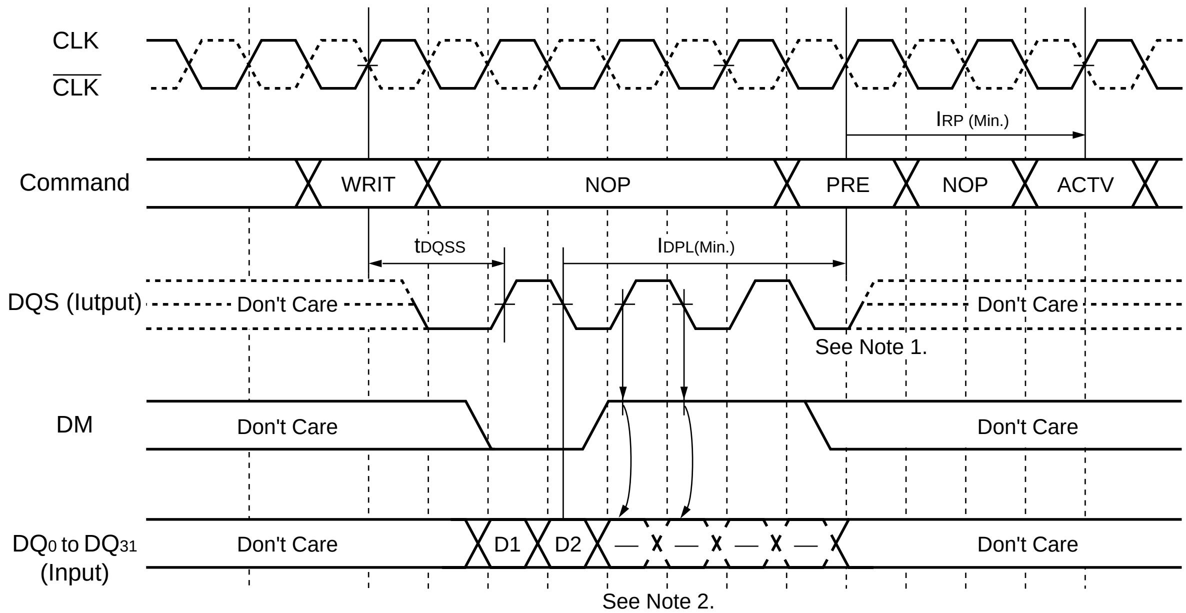
Note: I_{ROH} is the same as CAS Latency (CL). In case of CL =3, the I_{ROH} is 3 clock.

TIMING DIAGRAM - 9: READ INTERRUPTED BY BURST STOP (EXAMPLE @ CL = 2, BL = 8)



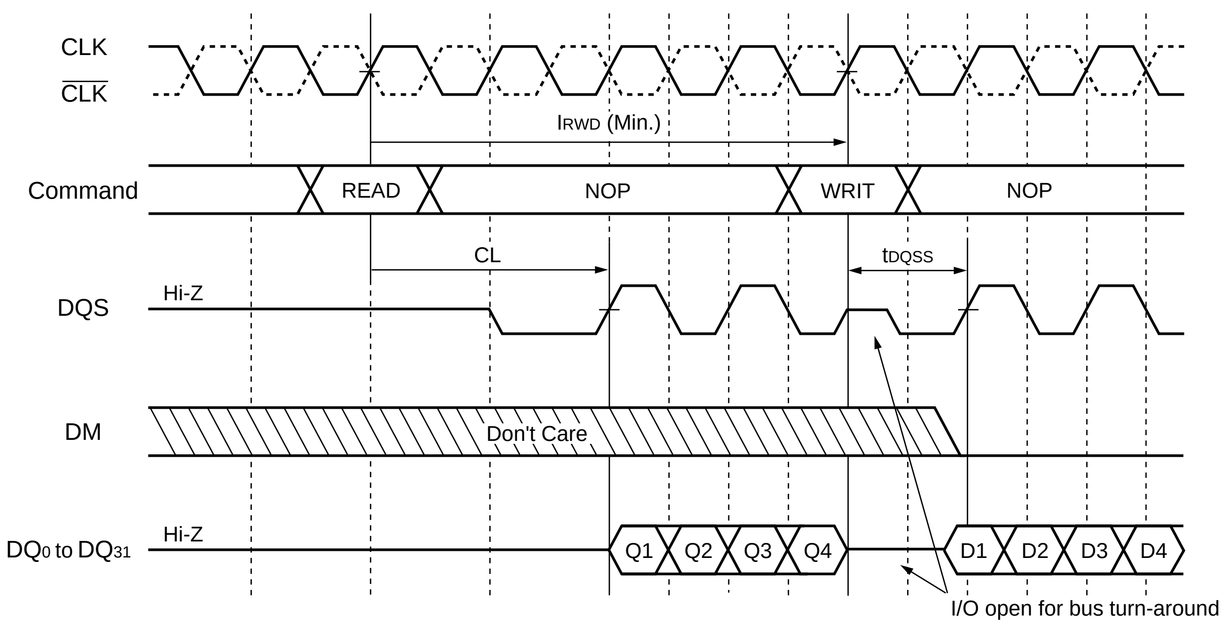
Note: I_{BSH} is the same as CAS Latency (CL). In case of CL =3, the I_{BSH} is 3 clock.

TIMING DIAGRAM - 10: WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 8)



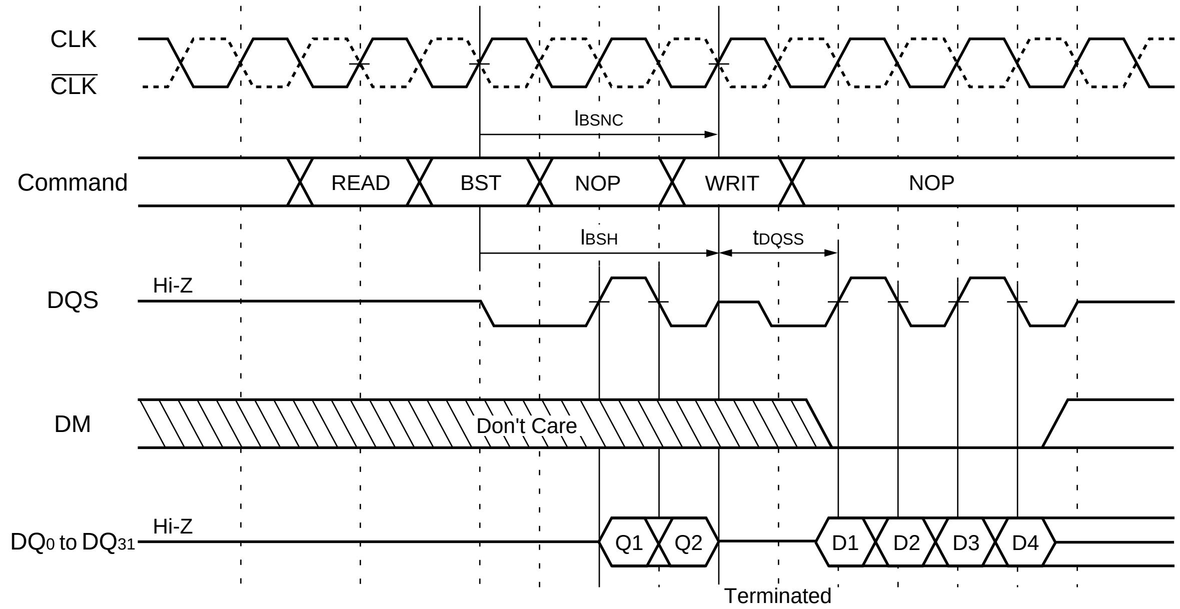
Note: 1. DQS Input are not required from when Precharge command is issued.
2. This pair of write data must be masked prior to Precharge command.

TIMING DIAGRAM - 11: READ TO WRITE (EXAMPLE @ CL = 2, BL = 4)



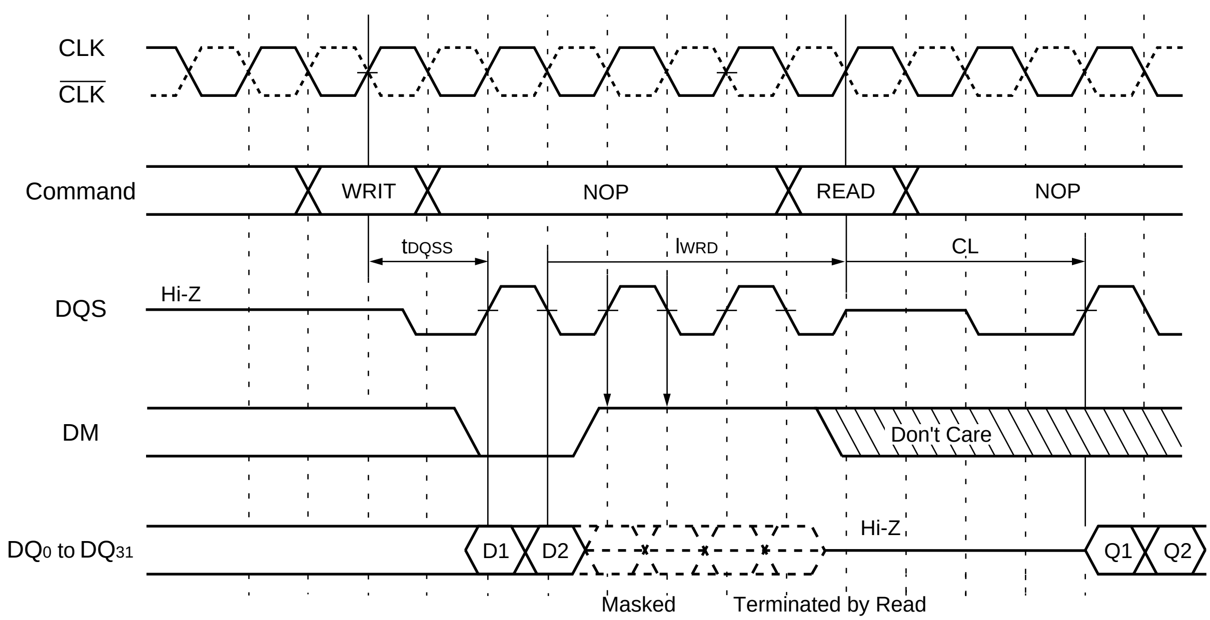
Note: l_{RWD} defines a minimum delay from Read to Write command input applied to the same bank.

TIMING DIAGRAM - 12: READ TO WRITE (EXAMPLE @ CL = 2, BL = 4)



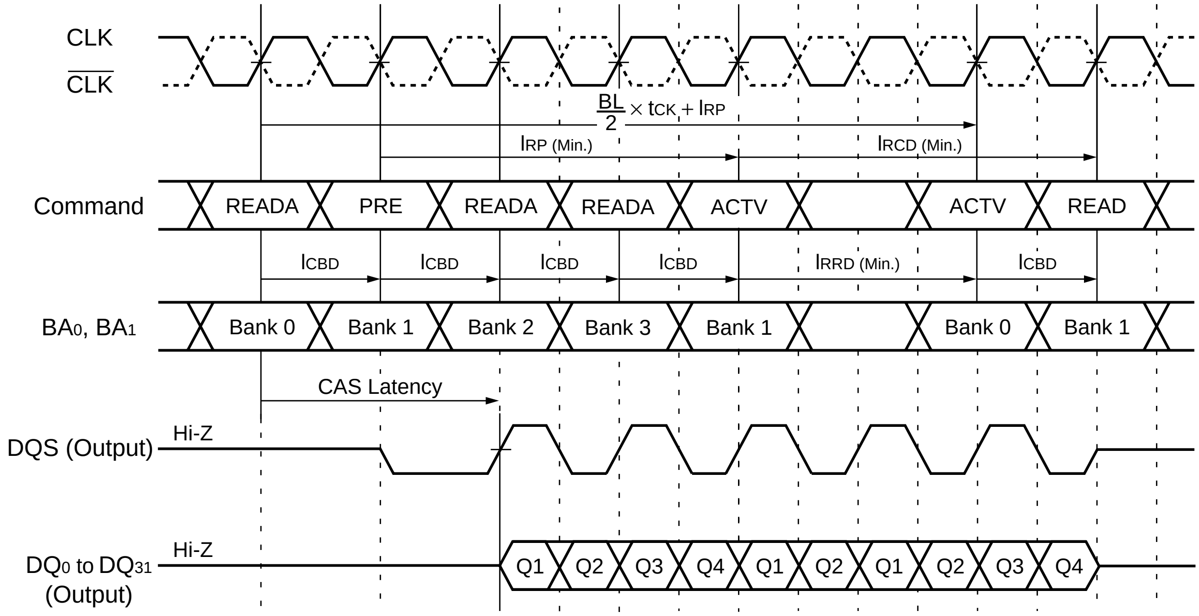
Note: DM are latched by DQS Input after Write command together with data Input.

TIMING DIAGRAM - 13: WRITE TO READ (EXAMPLE @ CL = 2, BL = 8)



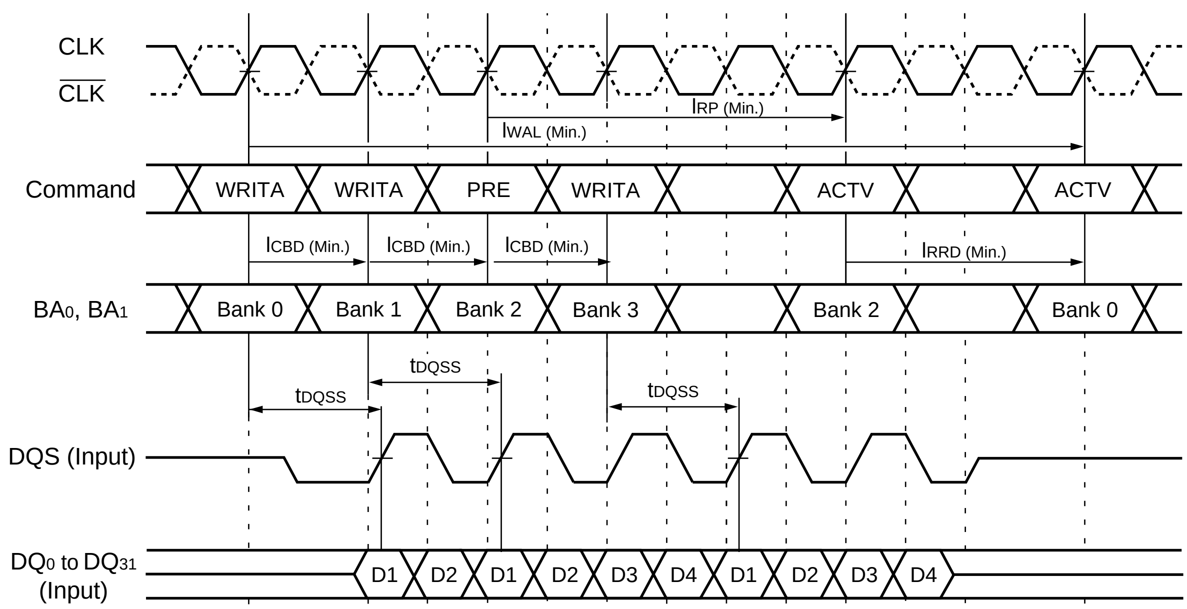
Note: Read command must be issued after l_{WRD} is satisfied and proceeding pair of data must be masked.

TIMING DIAGRAM - 14: READ WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2, BL = 4, Multiple Bank Operation)



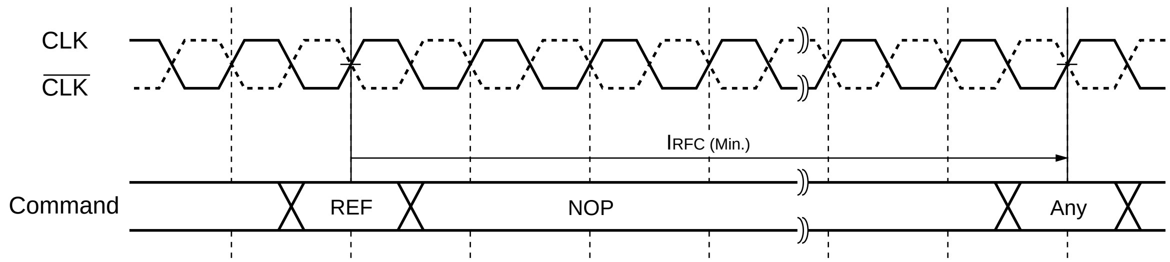
Note: Back to back Read with Auto-precharge (READA) command to the different bank in active state is possible. However, any new command to the same bank applied READA command can only be issued after (BL/2) × t_{CK}+l_{RP}.

TIMING DIAGRAM - 15: WRITE WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2, BL = 4, Multiple Bank Operation)

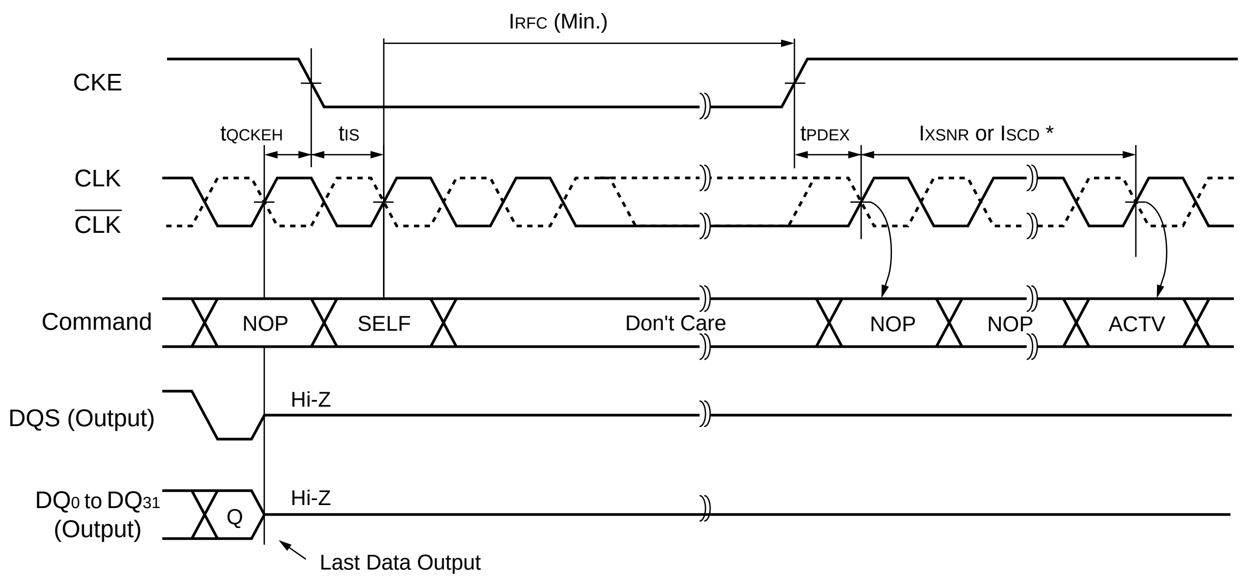


Note: Back to back Write with Auto-precharge (WRITA) command to the different bank in active state is possible. However, any new command to the same bank applied WRITA command can only be issued after l_{WAL}.

TIMING DIAGRAM - 16: AUTO-REFRESH ENTRY AND EXIT

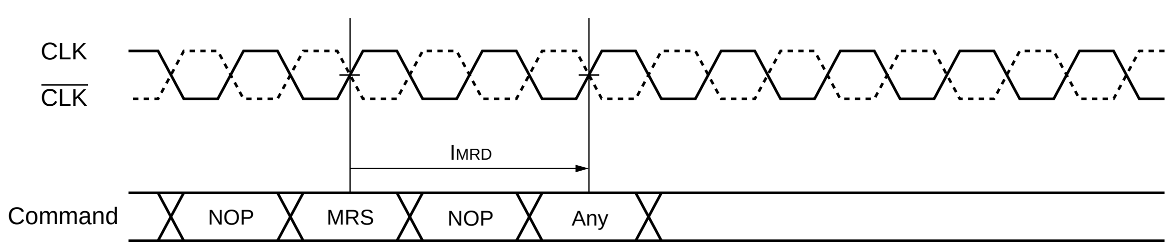


TIMING DIAGRAM - 17: SELF-REFRESH ENTRY AND EXIT



Note * :CKE must maintain High level and stable clock must be provided during the I_{SCD} period.
After Self-refresh exit, I_{XSNR} must be satisfied for at least specified period before any command (except for read) input.

TIMING DIAGRAM - 18: MODE REGISTER SET

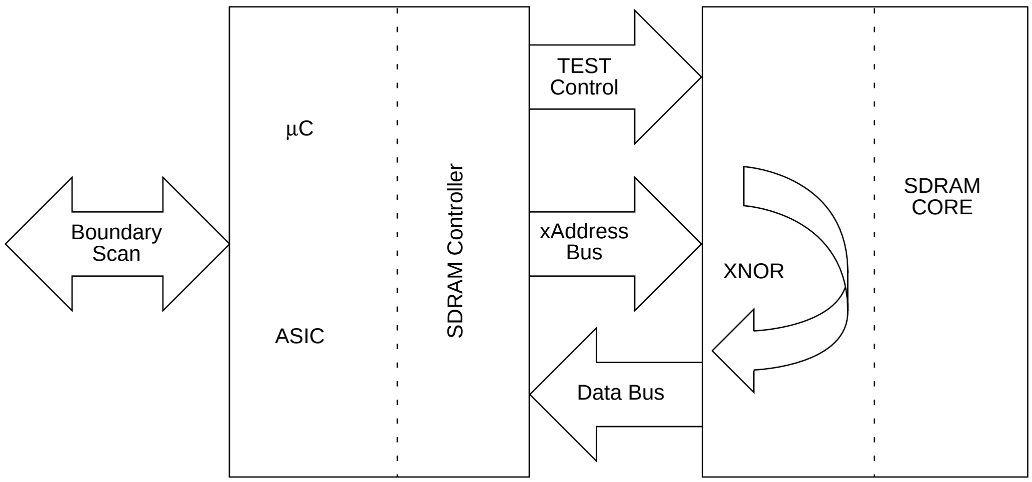


Note: MRS command must be issued after the last data is appeared on each DQ.

■ SCITT TEST MODE

ABOUT SCITT

SCITT (Static Component Interconnection Test Technology) is an XNOR circuit based test technology that is used for testing interconnection between SDRAM and SDRAM controller on the printed circuit boards. SCITT provides inexpensive board level test mode in combination with boundary-scan. The basic idea is simple, consider all output of SDRAM as output of XNOR circuit and each output pin has a unique mapping on the input of SDRAM. The ideal schematic block diagram is as shown below.



TEST Control : $\overline{CAS}$, $\overline{CS}$, CKE
xAddress Bus : A_0 to A_{10}, BA_0 to BA_2, $\overline{RAS}$, DM_0 to DM_3, CLK, $\overline{CLK}$, $\overline{WE}$
Data Bus : DQ_0 to DQ_{31}, DQS_0 to DQS_3

It is static and provides easy test pattern that result in a high diagnostic resolution for detecting all open/short faults.

SCITT TEST SEQUENCE

The followings are the SCITT test sequence. SCITT Test can be executed after power-on and prior to Precharge command in"■ FUNCTION DESCRIPTION POWER-UP INITIALIZATION". Once Precharge command is issued to SDRAM, it never get back to SCITT Test Mode during regular operation unless reset power supply for the purpose of a fail-safe way in get in and out of test mode.

1. Maintain all input signals (except CLK,$\overline{\text{CLK}}$) to be Low state (or at least CKE to be Low) and maintain CLK and $\overline{\text{CLK}}$ to be complementary state.
2. Apply V_{DD} voltage to all V_{DD} pins before or at the same time as V_{DDQ} pins.
3. Apply V_{DD} voltage to all V_{DDQ} pins before or at the same time as V_{REF} and V_{TT}.
4. Apply V_{REF} and V_{TT} (V_{TT} is applied to the system).
5. Maintain stable power for a minimum of 100μs.
6. Enter SCITT test mode.
7. Execute SCITT test.
8. Exit from SCITT mode.

It is required to follow Power On Sequence to execute read or write operation.

9. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200μs.
10. After the minimum of 200μs stable power and clock, apply NOP condition and take CKE to be High state.
11. Issue Precharge All Banks (PALL) command or Precharge Single Bank (PRE) command to every banks.
12. Issue EMRS to enable DLL, DE = Low.
13. Issue Mode Register Set command (MRS) to reset DLL, DR = High. An additional clock input for I_{PCD}*1 period is required to lock the DLL.
14. Apply minimum of two Auto-refresh command (REF).*2
15. Program the mode register by Mode Register Set command (MRS) with DR = Low.*2

The 6,7,8 steps define the SCITT mode available. It is possible to skip these steps if necessary (Refer to "■ FUNCTION DESCRIPTION POWER-UP INITIALIZATION").

Notes: *1. The I_{PCD} depends on operating clock period. The I_{PCD} is counted from "DLL Reset" at step-13 to any command input at step-15.

*2. The Mode Register Set command (MRS) can be issued before two Auto-refresh cycle.

COMMAND TRUTH TABLE Note *1

	Control			Input						Output	
	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	A_0 to A_{10}, BA_0 to BA_2	DM_0 to DM_3	CLK	$\overline{\text{CLK}}$	DQ_0 to DQ_{31}	DQS_0 to DQS_3
SCITT mode entry	H→L *2	L	L	X	X	X	X	H	L	X	X
								L	H		
SCITT mode exit	L→H *3	H *5	L *5	X	X	X	X	X	X	X	X
SCITT mode output enable *4	L	L	H	V	V	V	V	V	V	V	V

Notes: *1. L = Logic Low, H = Logic High, V = Valid, X = either L or H
*2. The SCITT mode entry command assumes the first $\overline{\text{CAS}}$ falling edge with $\overline{\text{CS}}$ = CKE = L and CLK,$\overline{\text{CLK}}$ signals are complementary after power on.
*3. The SCITT mode exit command assumes the first $\overline{\text{CAS}}$ rising edge after the test mode entry.
*4. Refer the test code table.
*5. $\overline{\text{CS}}$ = H or CKE = L is necessary to disable outputs in SCITT mode exit.

TEST CODE TABLE

DQ_0 to DQ_{31} and DQS_0 to DQS_3 output data is static and is determined by following logic during the SCITT mode operation.

$DQ_0 = \overline{RAS}$ xnor A_0
$DQ_1 = \overline{RAS}$ xnor A_1
$DQ_2 = \overline{RAS}$ xnor A_2
$DQ_3 = \overline{RAS}$ xnor A_3
$DQ_4 = \overline{RAS}$ xnor A_4
$DQ_5 = \overline{RAS}$ xnor A_5
$DQ_6 = \overline{RAS}$ xnor A_6
$DQ_7 = \overline{RAS}$ xnor A_7
$DQ_8 = \overline{RAS}$ xnor A_8
$DQ_9 = \overline{RAS}$ xnor A_9
$DQ_{10} = \overline{RAS}$ xnor A_{10}
$DQ_{11} = \overline{RAS}$ xnor BA_1
$DQ_{12} = \overline{RAS}$ xnor BA_0
$DQ_{13} = \overline{RAS}$ xnor BA_2
$DQ_{14} = \overline{RAS}$ xnor DM_0
$DQ_{15} = \overline{RAS}$ xnor DM_1
$DQ_{16} = \overline{RAS}$ xnor DM_2
$DQ_{17} = \overline{RAS}$ xnor DM_3
$DQ_{18} = \overline{RAS}$ xnor CLK
$DQ_{19} = \overline{RAS}$ xnor $\overline{CLK}$
$DQ_{20} = \overline{RAS}$ xnor $\overline{WE}$
$DQ_{21} = A_0$ xnor A_1
$DQ_{22} = A_0$ xnor A_2
$DQ_{23} = A_0$ xnor A_3
$DQ_{24} = A_0$ xnor A_4
$DQ_{25} = A_0$ xnor A_5
$DQ_{26} = A_0$ xnor A_6
$DQ_{27} = A_0$ xnor A_7
$DQ_{28} = A_0$ xnor A_8
$DQ_{29} = A_0$ xnor A_9
$DQ_{30} = A_0$ xnor A_{10}
$DQ_{31} = A_0$ xnor BA_0
$DQS_0 = A_0$ xnor BA_1
$DQS_1 = A_0$ xnor BA_2
$DQS_2 = A_0$ xnor DM_0
$DQS_3 = A_0$ xnor DM_1

- EXAMPLE OF TEST CODE TABLE

Input bus																						Output bus																																			
$\overline{RAS}$	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	BA_0	BA_1	BA_2	DM_0	DM_1	DM_2	DM_3	CLK	$\overline{CLK}$	$\overline{WE}$	DQ_0	DQ_1	DQ_2	DQ_3	DQ_4	DQ_5	DQ_6	DQ_7	DQ_8	DQ_9	DQ_{10}	DQ_{11}	DQ_{12}	DQ_{13}	DQ_{14}	DQ_{15}	DQ_{16}	DQ_{17}	DQ_{18}	DQ_{19}	DQ_{20}	DQ_{21}	DQ_{22}	DQ_{23}	DQ_{24}	DQ_{25}	DQ_{26}	DQ_{27}	DQ_{28}	DQ_{29}	DQ_{30}	DQ_{31}	DQS_0	DQS_1	DQS_2	DQS_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
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0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
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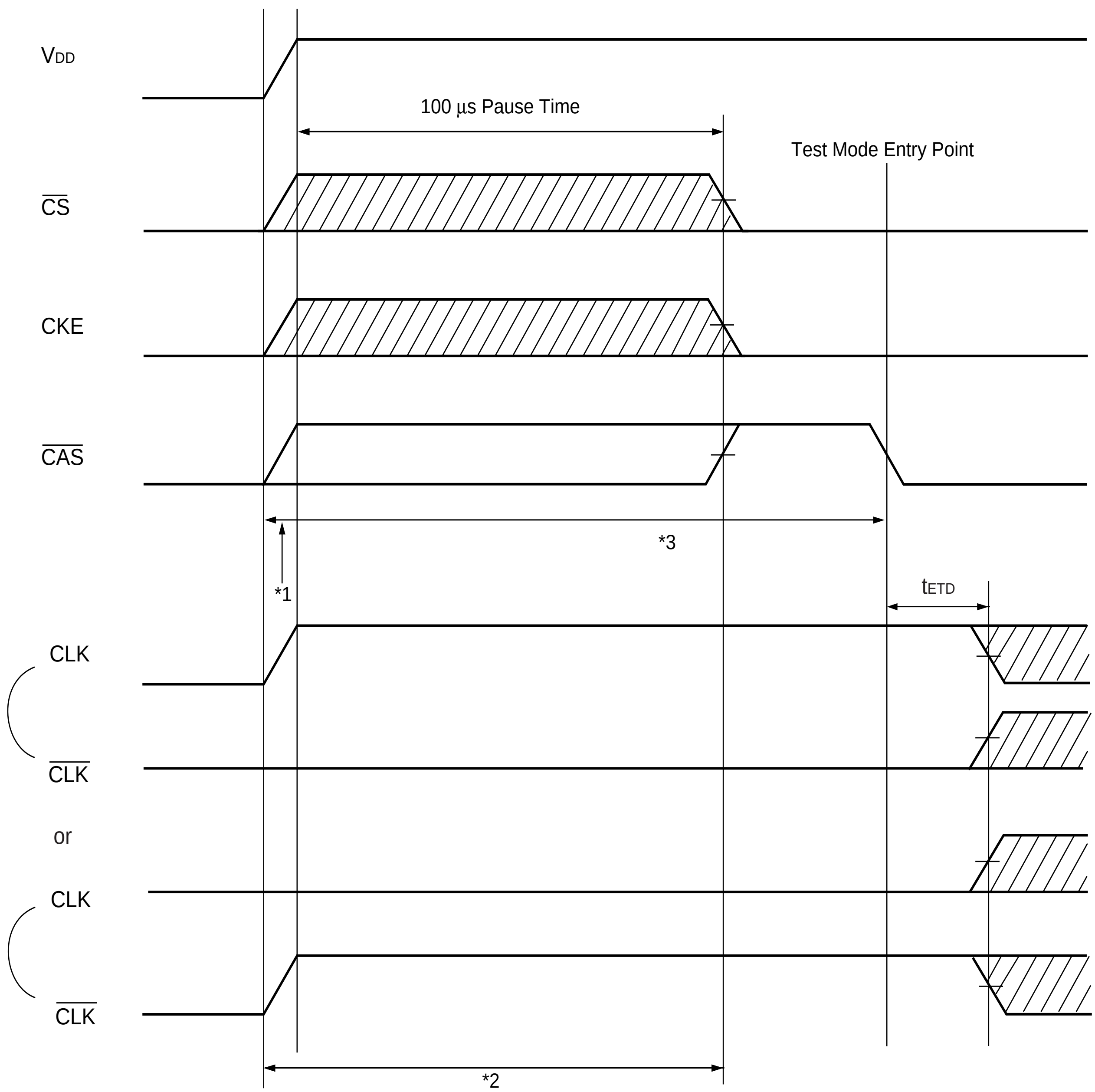
0 = input Low, 1 = input High, L = output Low, H = output High

AC SPECIFICATION

Parameter	Description	Min.	Max.	Units
t_{TS}	Test mode entry set up time	10	—	ns
t_{TH}	Test mode entry hold time	10	—	ns
t_{EPD}	Test mode exit to power on sequence delay time	10	—	ns
t_{TLZ}	$\overline{CS}$, CKE to output in Low-Z time	0	—	ns
t_{THZ}	$\overline{CS}$, CKE to output in High-Z time	0	20	ns
t_{TCA}	Test mode access time from control signals (clock enable & chip select)	—	40	ns
t_{TIA}	Test mode Input access time	—	20	ns
t_{TOH}	Test mode Output Hold time	0	—	ns
t_{ETD}	Test mode entry to test delay time	10	—	ns
t_{TIH}	Test mode input hold time	30	—	ns

TIMING DIAGRAMS

TIMING DIAGRAM - 1: POWER-UP TIMING DIAGRAM

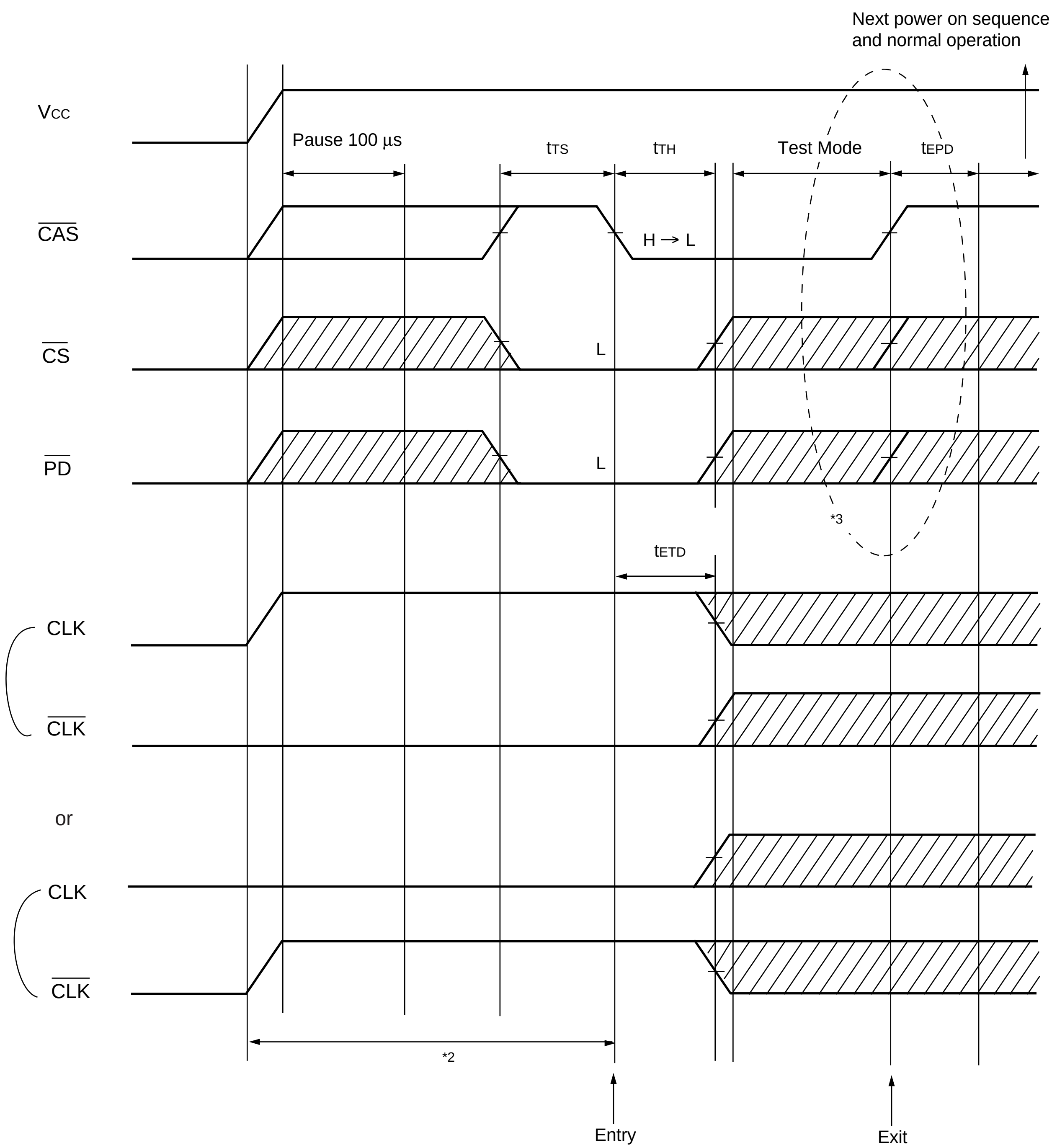


Notes: *1. $\overline{\text{CAS}}$ shall be staid either High or Low at power on.

*2 . All output buffers maintains in High-Z state regardless of the state of control signals except for $\overline{\text{CAS}}$ as long as the above timing is maintained.

*3. $\overline{\text{CAS}}$ must not be brought from High to Low.

TIMING DIAGRAM - 2 : SCITT TEST ENTRY AND EXIT *1

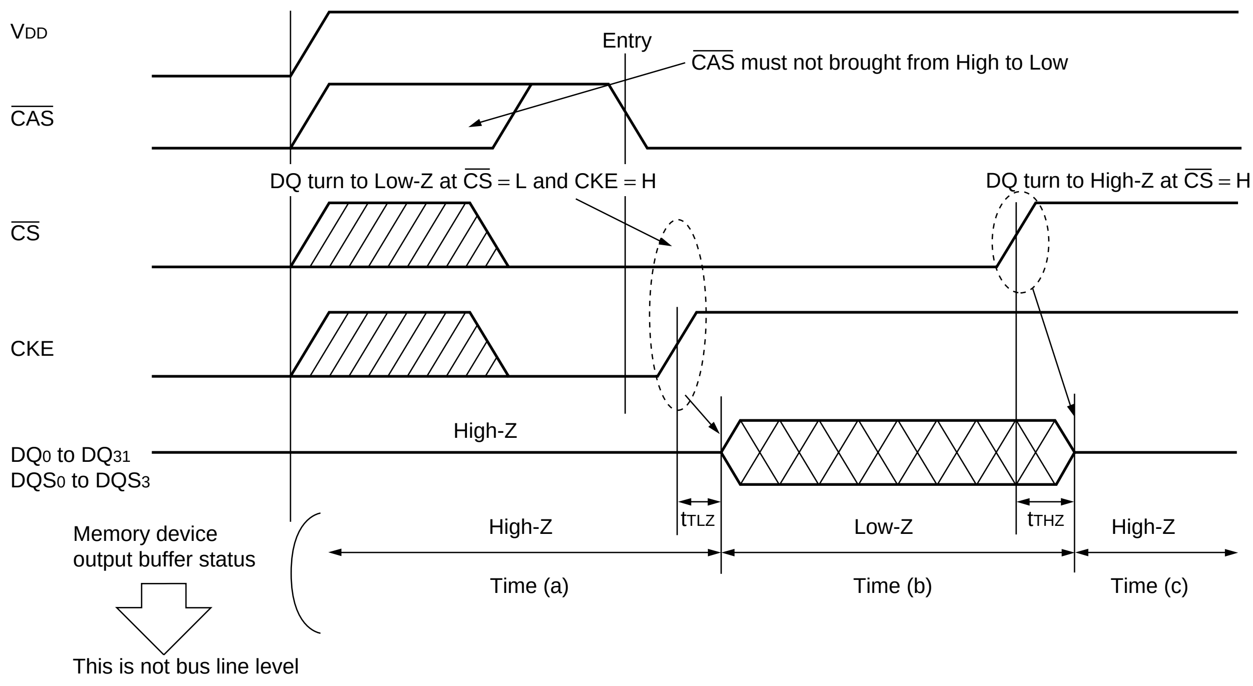


Notes: *1. If entry and exit operation have not been done correctly, $\overline{\text{CAS}}$, $\overline{\text{CS}}$, CKE pins will have some problems.

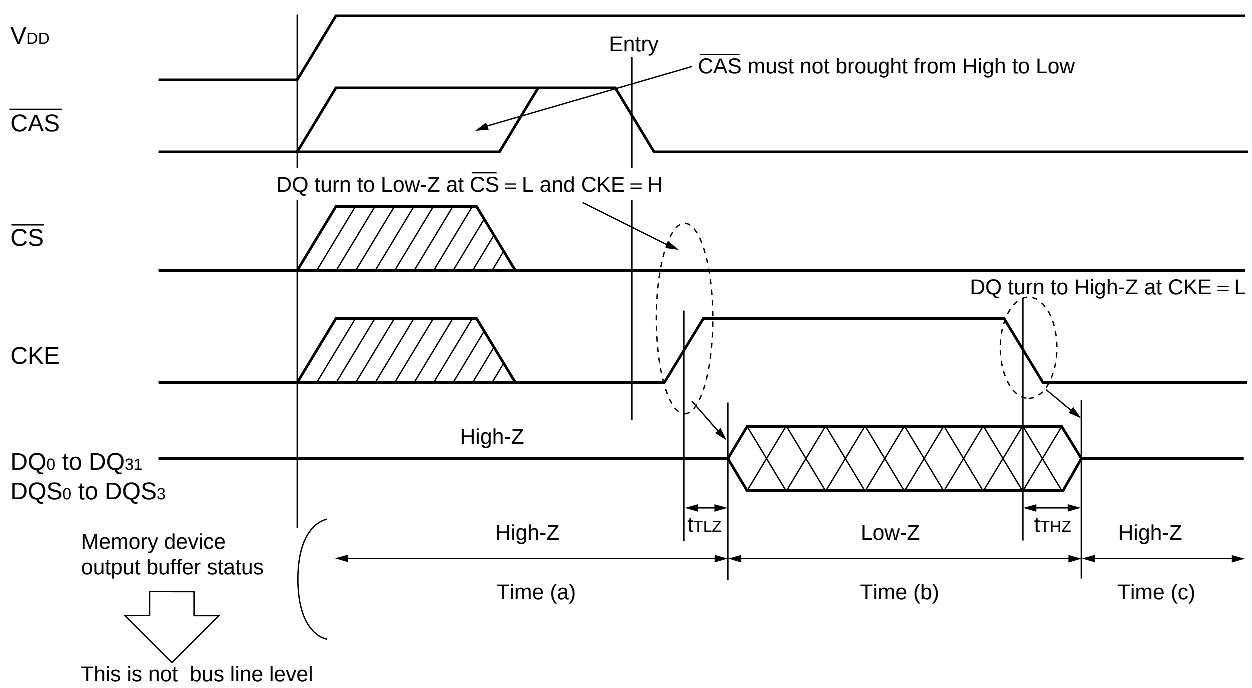
*2. PRE or PALL commands must not be asserted. Test mode is disable by those commands.

*3. Outputs must be disabled by $\overline{\text{CS}}$ = H or CKE = L before Exit.

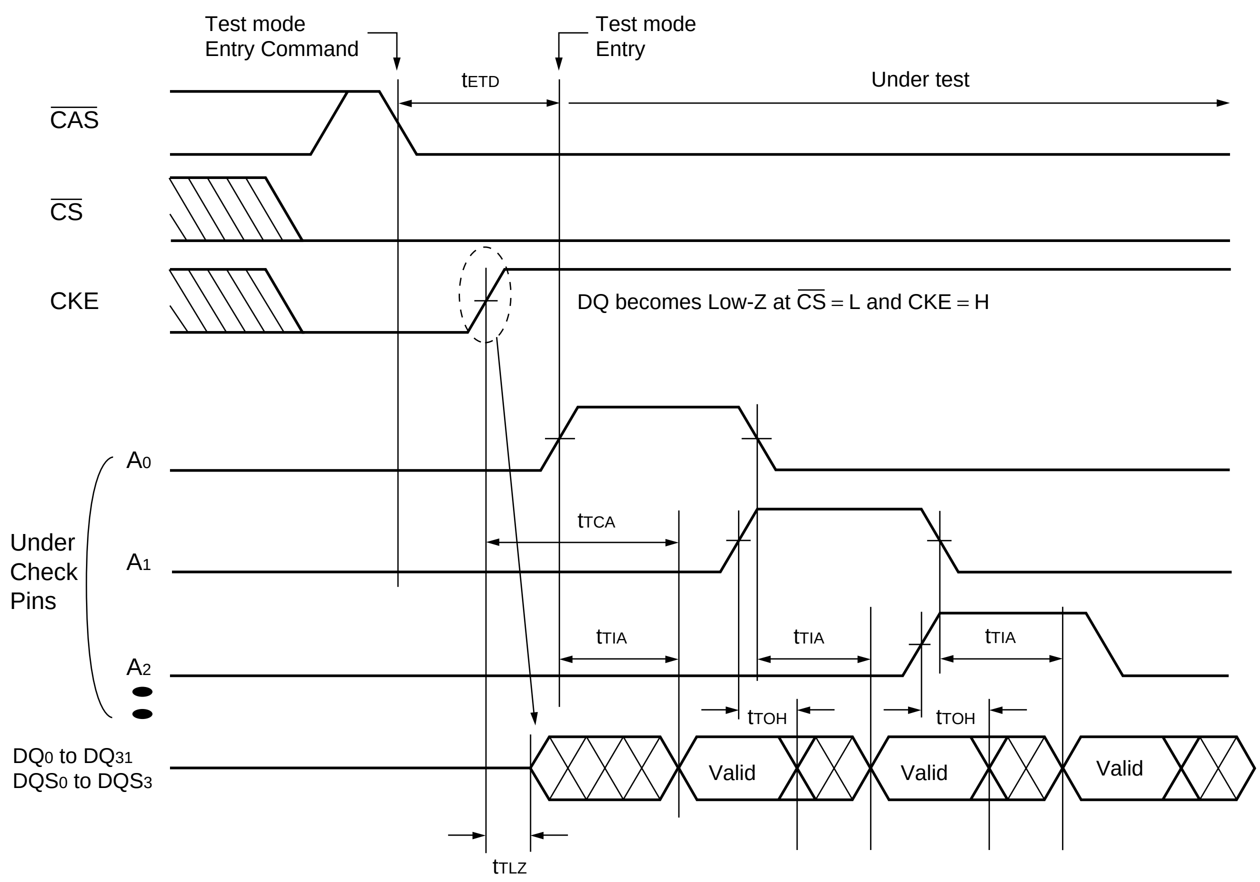
TIMING DIAGRAM - 3: OUTPUT CONTROL (1)



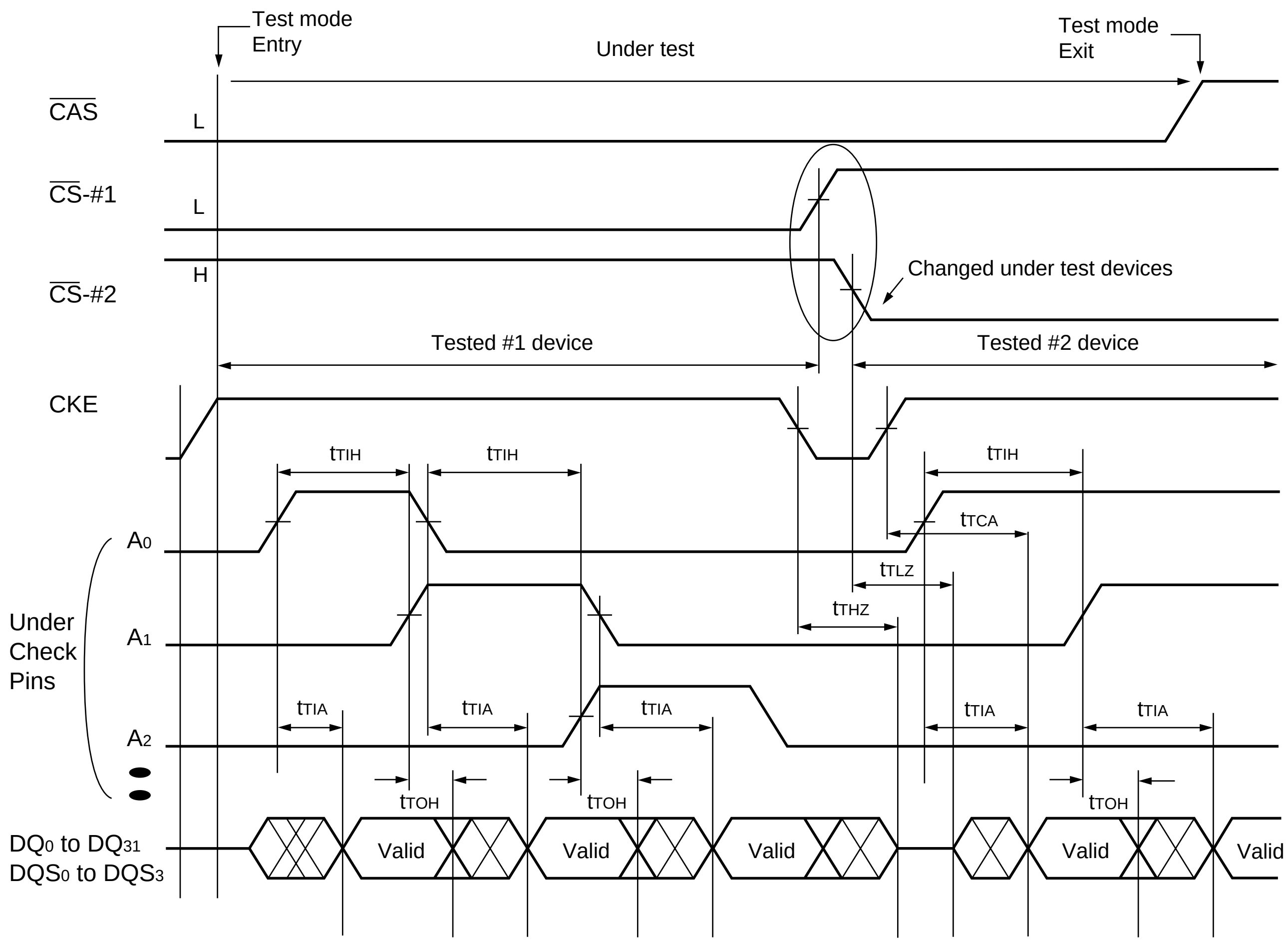
TIMING DIAGRAM - 4: OUTPUT CONTROL (2)



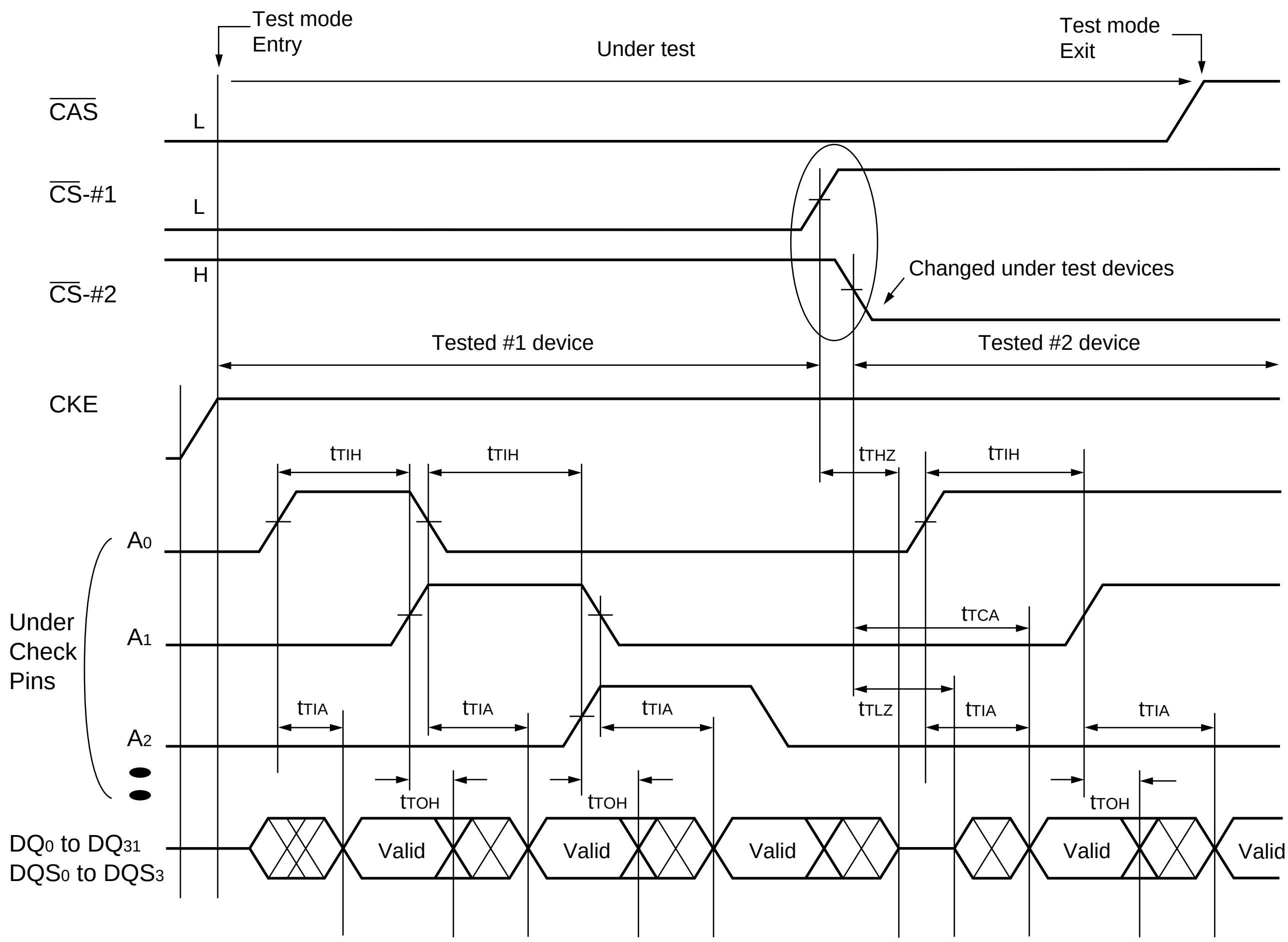
TIMING DIAGRAM - 5: TEST TIMING (1)



TIMING DIAGRAM - 6: TEST TIMING (2)



TIMING DIAGRAM - 7: TEST TIMING (3)



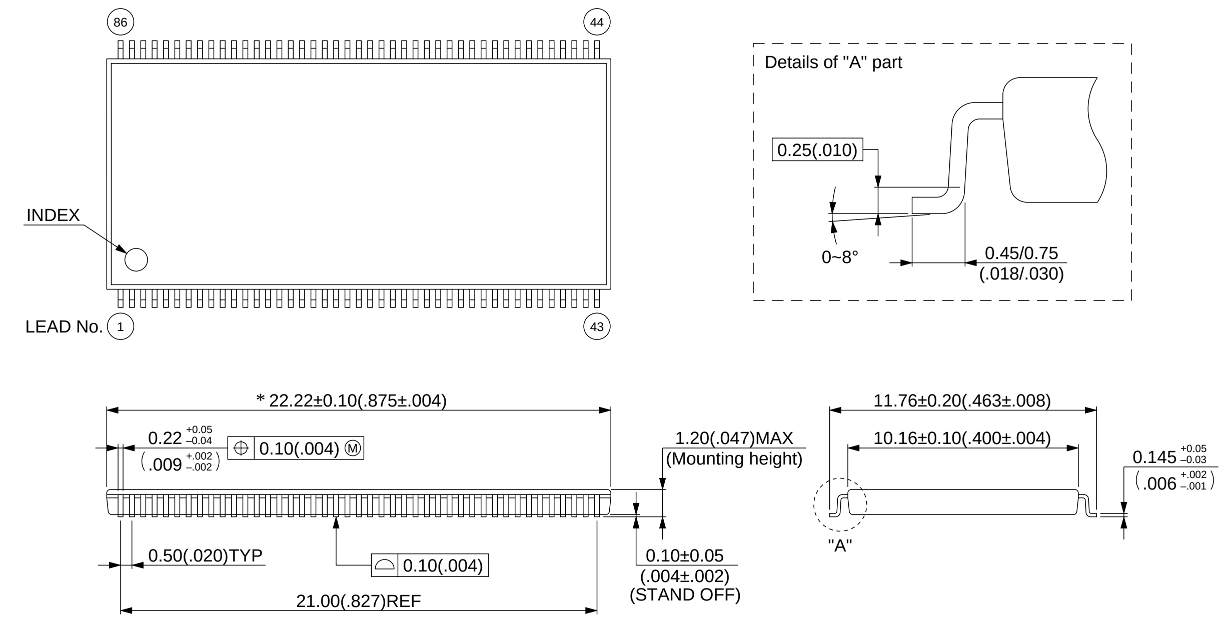
■ ORDERING INFORMATION

Part number	Package	Remarks
MB81P643287-50FN	86-pin plastic TSOP(II) (FPT-86P-M01)	—
MB81P643287-60FN		

■ PACKAGE DIMENSIONS

86-pin plastic TSOP (II)
(FPT-86P-M01)

*: Resin protrusion.(Each side: 0.15 (.006) Max.)



Dimensions in mm (inches).

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