

ASSP Communication Control

CMOS

FAST-20 SCSI Protocol Controller

MB86606A

■ DESCRIPTION

The MB86606A is an intelligent SCSI protocol controller (SPC) conforming to the ANSI (FAST-20) standard and integrating a PCI local bus interface function. The specification of SCSI controller block is based on the MB86605's one which is a Wide SCSI protocol controller, but the device functions/features to achieve the FAST-20 data transfer rate of maximum 40 Mbyte/sec at 16-bit FAST-20 SCSI, such as the size of internal data register FIFO, are larged on the MB86606A. As for the SCSI bus pins, a totem pole type single-ended driver/receiver is incorporated in the device so that it can drive the SCSI bus directly. Furthermore, the MB86606A is capable of connecting the external differential type driver/receiver.

The SCSI bus sequence is controlled by commands issued via the system interface. So, it supports sequential commands that perform the phase-to-phase sequences to reduce the overhead of system's sequence operations.

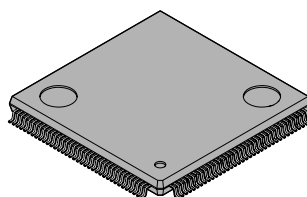
As another key feature to reduce the system overhead, the device has a 2 Kbytes user program memory to store the user program with the commands. Due to this, all the SCSI bus sequences including the data transfer can be performed automatically.

As the system interface block, it incorporates a 32-bit PCI local bus interface that easily realizes the SCSI interface on the motherboards of PCI bus based PCs and WSs, in addition to a 16-bit separate MPU and DMA buses. For the on-chip PCI bus interface, the MB86606A also incorporates a 32-bit DMA controller that is capable of supporting the scatter-gather function so that the data transfers can be controlled by both user program and the host system.

The device is fabricated by the advanced CMOS process and is housed in an 144-pin plastic Quad Flat Package (Suffix: -PMT2).

■ PACKAGE

144 pin plastic LQFP



(FPT-144P-M08)

■ FEATURES

SCSI Protocol Controller Block:

- Operable as initiator and target
- WIDE and FAST-20 data transfers
 - Synchronous transfer (max. 40 Mbytes/s: Up to 256 offset values can be set.)
 - Asynchronous transfer (max. 10 Mbytes/s)
- 512-byte FIFO register for data phase
- Two types (send-only and receive-only) of 32-byte data buffers for message, command, and status phases (MCS Buffers)
- On-chip totem pole type SCSI single-ended driver/receiver
- Supports external SCSI differential driver/receiver connectivity
- On-chip memory to store transfer parameters for each ID (up to 15 connected devices)
- On-chip 16-bit transfer block counter and 24-bit transfer byte counter
 - Maximum Transfer Byte : 1 Tbyte at fixed length data transfer
 - : 16 Mbyte at variable length data transfer
- Supports various control commands:
 - Sequential Commands : can perform phase-to-phase sequential operations (functions only when issuing from a system side.)
 - Discrete Commands : can perform any desired sequence to program in the user program memory
 - Data Transfer Commands : can program the transfer data length at the user program operation.
- On-chip direct control register for SCAM (SCSI Configured AutoMatically) Level-1 Protocol
- Supports Multi Selection/Reselection Responses
 - Selection and Reselection responses can be done to plural IDs.
- On-chip 2 Kbyte User Program Memory
 - Two Modes : 2 Kbyte × 1 bank and 1 Kbyte × 2 banks
 - (While 1 Kbyte × 2 banks are selected, host system can access another bank even if the user program is executing.)
 - Access to User program : Burst transfer via I/O access port
 - : Direct access to 2 Kbyte user program memory (only for PCI bus I/F mode)
- User Selectable Interrupt Report
 - Unnecessary interrupt reports can be disabled depending on user's applications to reduce a system ISR overhead.
- Two automatic receive modes
 - Initiator : can automatically receive information for new phase to which target switched
 - Target : can automatically receive attention condition generated by initiator
- Automatic selection/reselection
 - For command issues : automatically performs to receive MSG/CMD to the selection/reselection request from partner device
 - For user program operation : pauses the program currently executed and automatically jumps to the specified selection /reselection routine in response to the selection/reselection request from partner device.
- Operation Clock
 - System Clock: Max. 40 MHz
 - Internal Processor Operating Clock: Max. 20 MHz

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System Interface Block:

- Separate MPU and DMA buses called 16-bit Bus Mode
Directly connectable to 68-series or 80-series MPU
Two transfer modes (Program transfer and DMA transfer (slave mode))
- PCI Bus Interface Mode
Directly connectable to the 32-bit PCI local bus.
On-chip 32-bit DMAC for PCI bus master
Supports the PERR&SERR function
Supports the INTA# Interrupt Signals
Max. 64 bytes burst transfer
PCI system clock: Max. 33 MHz
- Data Bus Parity and Address Bus Parity (only for PCI bus interface mode) generation/check function

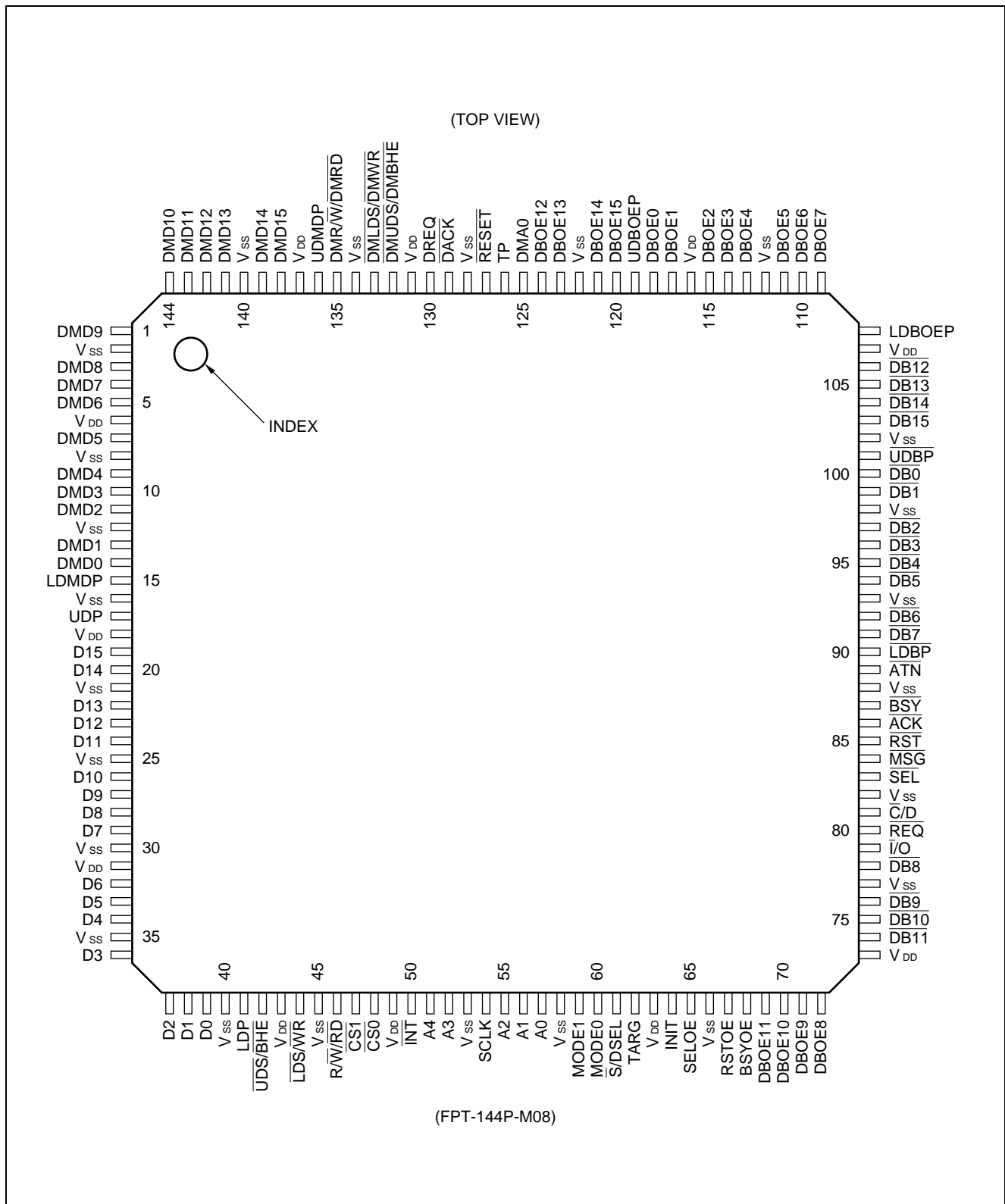
Others

- Compact 144-Pin Plastic Quad Flat Package (LQFP, Package Suffix: –PMT2)
- Pin compatible with MB86605
- Supply Voltage: $5V \pm 5\%$

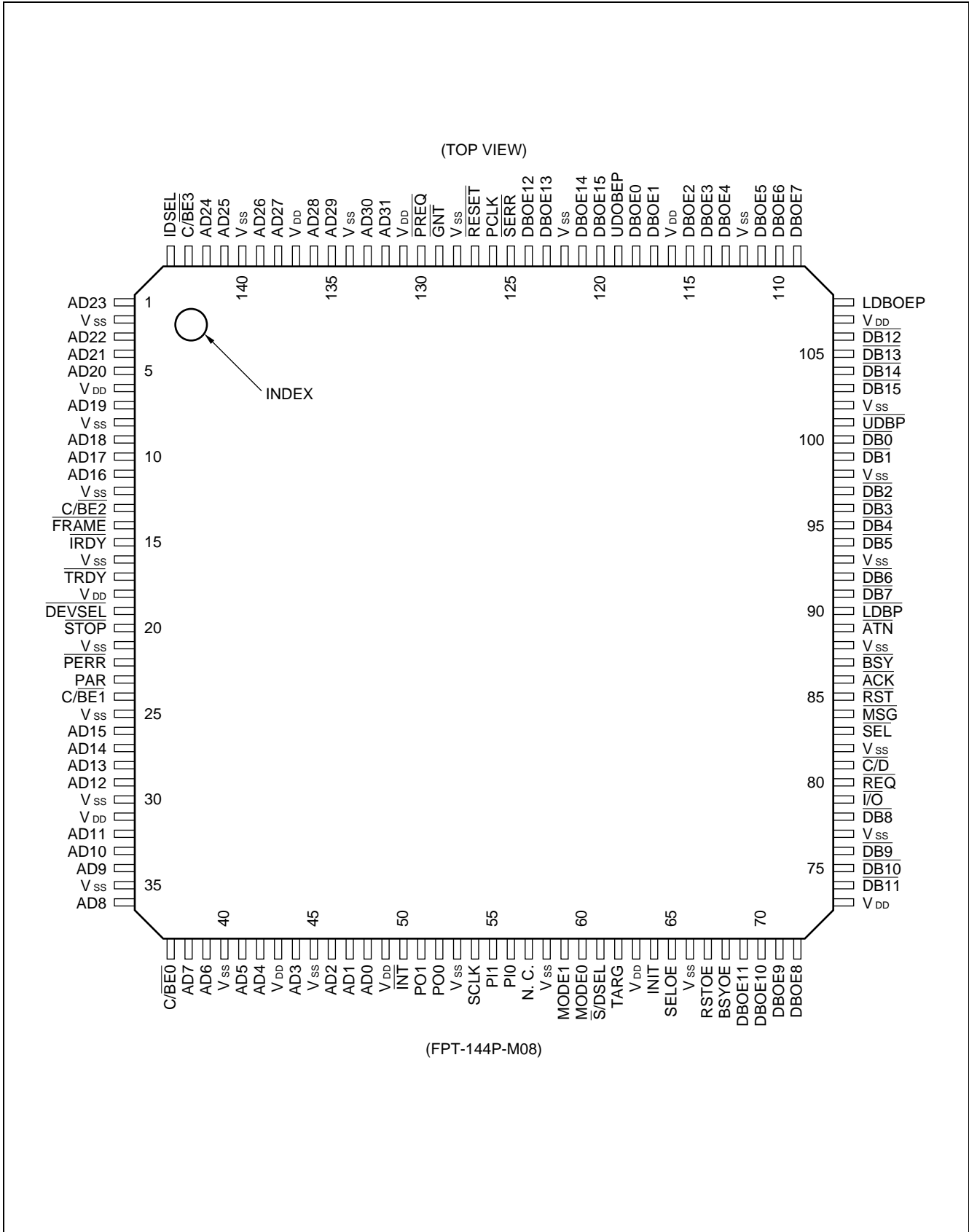
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■ PIN ASSIGNMENT

- 16-Bit Bus Mode



• PCI Bus Interface Mode



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■ PIN LIST

| Pin no. | 16-bit bus mode | | | | PCI bus I/F mode | | Pin no. | 16-bit bus mode | | | | PCI bus I/F mode | |
|---------|-----------------|-----------------|-----------------|----------|------------------|-----------------------------|---------|------------------------------|--------------------------|-----------------|-------------------------|-----------------------------|----------|
| | Mode 0 (68 I/F) | | Mode 1 (80 I/F) | | Mode 3 (PCI I/F) | | | Mode 0 (68 I/F) | | Mode 1 (80 I/F) | | Mode 3 (PCI I/F) | |
| | I/O | Pin name | I/O | Pin name | I/O | Pin name | | I/O | Pin name | I/O | Pin name | I/O | Pin name |
| 1 | I/O | DMD9 | | | I/O | AD23 | 31 | — | V _{DD} | | | | |
| 2 | — | V _{SS} | | | | | 32 | I/O | D6 | | I/O | AD11 | |
| 3 | I/O | DMD8 | | | I/O | AD22 | 33 | I/O | D5 | | I/O | AD10 | |
| 4 | I/O | DMD7 | | | I/O | AD21 | 34 | I/O | D4 | | I/O | AD9 | |
| 5 | I/O | DMD6 | | | I/O | AD20 | 35 | — | V _{SS} | | | | |
| 6 | — | V _{DD} | | | | | 36 | I/O | D3 | | I/O | AD8 | |
| 7 | I/O | DMD5 | | | I/O | AD19 | 37 | I/O | D2 | | I/O | C/ $\overline{\text{BE}}_0$ | |
| 8 | — | V _{SS} | | | | | 38 | I/O | D1 | | I/O | AD7 | |
| 9 | I/O | DMD4 | | | I/O | AD18 | 39 | I/O | D0 | | I/O | AD6 | |
| 10 | I/O | DMD3 | | | I/O | AD17 | 40 | — | V _{SS} | | | | |
| 11 | I/O | DMD2 | | | I/O | AD16 | 41 | I/O | LDP | | I/O | AD5 | |
| 12 | — | V _{SS} | | | | | 42 | I | $\overline{\text{UDS}}$ | I | $\overline{\text{BHE}}$ | I/O | AD4 |
| 13 | I/O | DMD1 | | | I/O | C/ $\overline{\text{BE}}_2$ | 43 | — | V _{DD} | | | | |
| 14 | I/O | DMD0 | | | I/O | $\overline{\text{FRAME}}$ | 44 | I | $\overline{\text{LDS}}$ | I | $\overline{\text{WR}}$ | I/O | AD3 |
| 15 | I/O | LDMDP | | | I/O | $\overline{\text{IRDY}}$ | 45 | — | V _{SS} | | | | |
| 16 | — | V _{SS} | | | | | 46 | I | R/ $\overline{\text{W}}$ | I | $\overline{\text{RD}}$ | I/O | AD2 |
| 17 | I/O | UDP | | | I/O | $\overline{\text{TRDY}}$ | 47 | I | $\overline{\text{CS}}_1$ | | I/O | AD1 | |
| 18 | — | V _{DD} | | | | | 48 | I | $\overline{\text{CS}}_0$ | | I/O | AD0 | |
| 19 | I/O | D15 | | | I/O | $\overline{\text{DEVSEL}}$ | 49 | — | V _{DD} | | | | |
| 20 | I/O | D14 | | | I/O | $\overline{\text{STOP}}$ | 50 | $\frac{\text{O}}{\text{OD}}$ | $\overline{\text{INT}}$ | | | | |
| 21 | — | V _{SS} | | | | | 51 | I | A4 | | O | PO1 | |
| 22 | I/O | D13 | | | I/O | $\overline{\text{PERR}}$ | 52 | I | A3 | | O | PO0 | |
| 23 | I/O | D12 | | | I/O | PAR | 53 | — | V _{SS} | | | | |
| 24 | I/O | D11 | | | I/O | C/ $\overline{\text{BE}}_1$ | 54 | I | SCLK | | | | |
| 25 | — | V _{SS} | | | | | 55 | IU | A2 | | IU | PI1 | |
| 26 | I/O | D10 | | | I/O | AD15 | 56 | IU | A1 | | IU | PI0 | |
| 27 | I/O | D9 | | | I/O | AD14 | 57 | IU | A0 | | IU | N.C. | |
| 28 | I/O | D8 | | | I/O | AD13 | 58 | — | V _{SS} | | | | |
| 29 | I/O | D7 | | | I/O | AD12 | 59 | I | MODE1 | | | | |
| 30 | — | V _{SS} | | | | | 60 | I | MODE2 | | | | |

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| Pin no. | 16-bit bus mode | | | | PCI bus I/F mode | | Pin no. | 16-bit bus mode | | | | PCI bus I/F mode | |
|---------|-----------------|---------------------|-----------------|----------|------------------|----------|---------|-----------------|-------------------|-----------------|----------|------------------|----------|
| | Mode 0 (68 I/F) | | Mode 1 (80 I/F) | | Mode 3 (PCI I/F) | | | Mode 0 (68 I/F) | | Mode 1 (80 I/F) | | Mode 3 (PCI I/F) | |
| | I/O | Pin name | I/O | Pin name | I/O | Pin name | | I/O | Pin name | I/O | Pin name | I/O | Pin name |
| 61 | I | $\overline{S}/DSEL$ | | | | | 91 | I/O | $\overline{DB7}$ | | | | |
| 62 | O | TARG | | | | | 92 | I/O | $\overline{DB6}$ | | | | |
| 63 | — | V _{DD} | | | | | 93 | — | V _{SS} | | | | |
| 64 | O | INIT | | | | | 94 | I/O | $\overline{DB5}$ | | | | |
| 65 | O | SELOE | | | | | 95 | I/O | $\overline{DB4}$ | | | | |
| 66 | — | V _{SS} | | | | | 96 | I/O | $\overline{DB3}$ | | | | |
| 67 | O | RSTOE | | | | | 97 | I/O | $\overline{DB2}$ | | | | |
| 68 | O | BSYOE | | | | | 98 | — | V _{SS} | | | | |
| 69 | O | DBOE11 | | | | | 99 | I/O | $\overline{DB1}$ | | | | |
| 70 | O | DBOE10 | | | | | 100 | I/O | $\overline{DB0}$ | | | | |
| 71 | O | DBOE9 | | | | | 101 | I/O | \overline{UDBP} | | | | |
| 72 | O | DBOE8 | | | | | 102 | — | V _{SS} | | | | |
| 73 | — | V _{DD} | | | | | 103 | I/O | $\overline{DB15}$ | | | | |
| 74 | I/O | $\overline{DB11}$ | | | | | 104 | I/O | $\overline{DB14}$ | | | | |
| 75 | I/O | $\overline{DB10}$ | | | | | 105 | I/O | $\overline{DB13}$ | | | | |
| 76 | I/O | DB9 | | | | | 106 | I/O | $\overline{DB12}$ | | | | |
| 77 | — | V _{SS} | | | | | 107 | — | V _{DD} | | | | |
| 78 | I/O | $\overline{DB8}$ | | | | | 108 | O | LDBOEP | | | | |
| 79 | I/O | $\overline{I/O}$ | | | | | 109 | O | DBOE7 | | | | |
| 80 | I/O | \overline{REQ} | | | | | 110 | O | DBOE6 | | | | |
| 81 | I/O | $\overline{C/D}$ | | | | | 111 | O | DBOE5 | | | | |
| 82 | — | V _{SS} | | | | | 112 | — | V _{SS} | | | | |
| 83 | I/O | \overline{SEL} | | | | | 113 | O | DBOE4 | | | | |
| 84 | I/O | \overline{MSG} | | | | | 114 | O | DBOE3 | | | | |
| 85 | I/O | \overline{RST} | | | | | 115 | O | DBOE2 | | | | |
| 86 | I/O | \overline{ACK} | | | | | 116 | — | V _{DD} | | | | |
| 87 | I/O | \overline{BSY} | | | | | 117 | O | DBOE1 | | | | |
| 88 | — | V _{SS} | | | | | 118 | O | DBOE0 | | | | |
| 89 | I/O | \overline{ATN} | | | | | 119 | O | UDBOEP | | | | |
| 90 | I/O | \overline{LDBP} | | | | | 120 | O | DBOE15 | | | | |

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| Pin no. | 16-bit bus mode | | | | PCI bus I/F mode | | Pin no. | 16-bit bus mode | | | | PCI bus I/F mode | |
|---------|-----------------|---------------------------|-----------------|---------------------------|--------------------------|----------|---------|-----------------|---------------------------|-----------------|--------------------------|---------------------------|----------|
| | Mode 0 (68 I/F) | | Mode 1 (80 I/F) | | Mode 3 (PCI I/F) | | | Mode 0 (68 I/F) | | Mode 1 (80 I/F) | | Mode 3 (PCI I/F) | |
| | I/O | Pin name | I/O | Pin name | I/O | Pin name | | I/O | Pin name | I/O | Pin name | I/O | Pin name |
| 121 | O | DBOE14 | | | | | 133 | I | $\overline{\text{DMLDS}}$ | I | $\overline{\text{DMWR}}$ | I/O | AD30 |
| 122 | — | Vss | | | | | 134 | — | Vss | | | | |
| 123 | O | DBOE13 | | | | | 135 | I | $\overline{\text{DMR/W}}$ | I | $\overline{\text{DMRD}}$ | I/O | AD29 |
| 124 | O | DBOE12 | | | | | 136 | I/O | UDMDP | | I/O | AD28 | |
| 125 | I | DMA0 | | OD | $\overline{\text{SERR}}$ | | 137 | — | VDD | | | | |
| 126 | I | TP | | I | PCLK | | 138 | I/O | DMD15 | | I/O | AD27 | |
| 127 | I | $\overline{\text{RESET}}$ | | | | | 139 | I/O | DMD14 | | I/O | AD26 | |
| 128 | — | Vss | | | | | 140 | — | Vss | | | | |
| 129 | I | $\overline{\text{DACK}}$ | | I | $\overline{\text{GNT}}$ | | 141 | I/O | DMD13 | | I/O | AD25 | |
| 130 | O | DREQ | | O | $\overline{\text{PREQ}}$ | | 142 | I/O | DMD12 | | I/O | AD24 | |
| 131 | — | VDD | | | | | 143 | I/O | DMD11 | | I/O | $\overline{\text{C/BE3}}$ | |
| 132 | I | $\overline{\text{DMUDS}}$ | I | $\overline{\text{DMBHE}}$ | I/O | AD31 | 144 | I/O | DMD10 | | I | IDSEL | |

I : Input pin

O : Output pin

I/O : Input/Output pin

IU : Input pin with pull-up resistor

OD : Open-drain output pin

■ PIN DESCRIPTION

1. SCSI Interface

| Pin no. | Pin name | I/O | Function |
|---|---|-----|--|
| 84, 81 89, 79 | $\overline{\text{MSG}}, \overline{\text{C/D}}$ $\overline{\text{ATN}}, \text{I/O}$ | I/O | These are the SCSI control signal input and output pins. They can be connected directly to a single-ended SCSI connector. Either open-drain or totem pole output can be selected. |
| 80, 86 | $\overline{\text{REQ}}, \overline{\text{ACK}}$ | I/O | These are the SCSI control signal input and output pins. They can be connected directly to a single-ended SCSI connector. The output buffer is the totem pole type. |
| 68 65 67 | BSYOE SELOE RSTOE | O | These are used for output control of SCSI control signals. They should be used as control signals for the external differential driver/receiver circuit. |
| 87 83 85 | $\overline{\text{BSY}}$ $\overline{\text{SEL}}$ $\overline{\text{RST}}$ | I/O | These are the SCSI control signal input and output pins. They can be connected directly to a single-ended SCSI connector. The output buffer is the open-drain type. |
| 120, 121, 123, 124, 69 to 72 119 109 to 111, 113 to 115, 117, 118 108 | DBOE15 to DBOE8 UDBOEP DBOE7 to DBOE0 LDBOEP | O | These are used for output control of SCSI data bus signals. They should be used as control signals for the external differential driver/receiver circuit. |
| 103 to 106, 74 to 76, 78 101 91, 92, 94 to 97, 99, 100 90 | $\overline{\text{DB15}}$ to $\overline{\text{DB8}}$ UDBP $\overline{\text{DB7}}$ to $\overline{\text{DB0}}$ LDBP | I/O | These are used to input and output SCSI data bus signals. They can be connected directly to a single-ended SCSI connector. Either open-drain or totem pole output buffer can be selected. |
| 64 62 | INIT TARG | O | These are used to output signals indicating the chip operating status. They should be used as control signals for the external differential driver/receiver circuit. |
| 61 | $\overline{\text{S}}/\text{DESL}$ | I | This is used to input signal for selecting the chip operation mode. Single-ended: Input 0 Differential-ended: Input 1 While 0 is input to this pin, all the SCSI control signals, data bus output control signals, INIT, and TARG signals are fixed with L level. |
| 54 | SCLK | I | This pin is used for a system clock input for SCSI protocol controller block. (Max. 40 MHz) |

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2. 16-Bit Bus Mode-MPU Interface

| Pin no. | Pin name | I/O | Function |
|----------------------------------|---------------------------------------|-----|--|
| 48 | $\overline{CS0}$ | I | This is used to input signals for the MPU to select the SPC as the I/O device. |
| 47 | $\overline{CS1}$ | I | This is used to input select signals (external circuit select signals) for the MPU to input and output the DMA data bus data via the SPC. |
| 19, 20, 22 to 24, 26 to 28 17 | D15 to D8 UDP | I/O | Upper byte and parity of data bus When $\overline{CS0}$ input valid: I/O ports for internal registers in SPC When $\overline{CS1}$ input valid: I/O ports for DMA bus data |
| 29, 32 to 34, 36 to 39 41 | D7 to D0 LDP | I/O | Lower byte and parity of data bus When $\overline{CS0}$ input valid: I/O ports for internal registers in SPC When $\overline{CS1}$ input valid: I/O ports for DMA bus data |
| 51, 52, 55 to 57 | A4 to A0 | IU | These are used to input addresses for selecting the Internal registers. |
| 46 | \overline{RD} (R/\overline{W}) | I | In 80-series mode: This is used to input the read strobe signal for reading data from the SPC to the MPU. In 68-series mode: This is used to input the R/\overline{W} control signal for reading and writing data from the MPU to the SPC. |
| 44 | \overline{WR} (\overline{LDS}) | I | In 80-series mode: This is used to input the write strobe signal for writing data from the MPU to the SPC. In 68-series mode: This is used to input the \overline{LDS} signal output by the MPU when the lower byte of the data bus is valid. |
| 42 | \overline{BHE} (\overline{UDS}) | I | In 80-series mode: This is used to input the \overline{BHE} signal output by the MPU when the upper byte of the data bus is valid. In 68-series mode: This is used to input the \overline{UDS} signal output by the MPU when the upper byte of the data bus is valid. |

3. 16-Bit Bus Mode – DMA Interface

| Pin no. | Pin name | I/O | Function |
|-----------------------------------|---|-----|--|
| 130 | DREQ | O | This is used to output DMA transfer request signals to the DMAC. DMA data transfer between the SPC and memory is requested. |
| 129 | $\overline{\text{DACK}}$ | I | This is used to input DMA-enabling signals from the DMAC. When the DMA enabling signal is active, DMA reading and writing are executed. |
| 138, 139, 141 to 144, 1, 3 136 | DMD15 to 8 UDMDP | I/O | Upper byte and parity of DMA data bus When CS1 input valid: The MPU data bus is directly connected. When 80-series mode: The 2nd data is input/output. When 68-series mode: The 1st data is input/output. |
| 4, 5, 7, 9 to 11, 13, 14 15 | DMD7 to 0 LDMDP | I/O | Lower byte and parity of DMA data bus When CS1 input valid: The MPU data bus is directly connected. When 80-series mode: The 1st data is input/output. When 68-series mode: The 2nd data is input/output. |
| 135 | $\overline{\text{DMRD}}$ (DMR/ $\overline{\text{W}}$) | I | In 80-series mode: This is used to input the $\overline{\text{IORD}}$ or $\overline{\text{RD}}$ signal for outputting data from the SPC to the DMA bus. In 68-series mode: This is used to input the $\overline{\text{R/W}}$ control signal for outputting and inputting data from the DMAC to the SPC. |
| 133 | $\overline{\text{DMWR}}$ ($\overline{\text{DMLDS}}$) | I | In 80-series mode: This is used to input the $\overline{\text{IOWR}}$ or $\overline{\text{WR}}$ signal for inputting data from the DMA bus to the SPC. In 68-series mode: This is used to input the $\overline{\text{LDS}}$ signal output by the DMAC when the lower byte of the DMA data bus is valid. |
| 132 | $\overline{\text{DMBHE}}$ ($\overline{\text{DMUDS}}$) | I | In 80-series mode: This is used to input the $\overline{\text{BHE}}$ signal output by the DMAC when the upper byte of the DMA data bus is valid. In 68-series mode: This is used to input the $\overline{\text{UDS}}$ signal output by the DMAC when the upper byte of the DMA data bus is valid. |
| 125 | DMA0 | I | This is used to input the address data A0 signal output by the DMAC in the 80-series mode. In 68-series mode: Connect to power supply pin (V _{DD}). |
| 126 | TP (Transfer permission) | I | This is used to input DMA-transfer-enabling signals. When the TP signal is active, the SPC performs the DMA transfer. When this signal becomes inactive during DMA transfer, the transfer stops temporarily at the block boundary. |

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4. PCI Bus Interface Mode

| Pin no. | Pin name | I/O | Function |
|---|--|-----|---|
| 130 | $\overline{\text{PREQ}}$ | O | This pin is used to request the bus arbiter for use of the bus. |
| 129 | $\overline{\text{GNT}}$ | I | This is the response signal input pin to the $\overline{\text{REQ}}$ signal from the bus arbiter. |
| 132, 133, 135, 136, 138, 139, 141, 142, 1, 3 to 5, 7, 9 to 11, 26 to 29, 32 to 34, 36, 38, 39, 41, 42, 44, 46 to 48 | AD31 to AD0 | I/O | PCI 32-bit address and data multiplexed pins |
| 143, 13, 24, 37 | $\overline{\text{C/BE3}}$ to $\overline{\text{C/BE0}}$ | I/O | Bus command and Byte Enable signals multiplexed pins. |
| 23 | PAR | I/O | This is an even parity signal pin for the AD31 to AD0 and $\overline{\text{C/BE3}}$ to $\overline{\text{C/BE0}}$ signals. This PAR signal becomes valid after one clock. |
| 14 | $\overline{\text{FRAME}}$ | I/O | This is a frame signal pin that indicates data are transferring on the bus. |
| 17 | $\overline{\text{TRDY}}$ | I/O | Data Ready signal of Target side. |
| 15 | $\overline{\text{IRDY}}$ | I/O | Data Ready signal of Initiator (Bus master) side. |
| 20 | $\overline{\text{STOP}}$ | I/O | This is a stop request signal to stop the data transfer from target to master. |
| 19 | $\overline{\text{DEVSEL}}$ | I/O | Device select pin. While the device is a target, this pin outputs the select signal that indicates the self device is selected. While the device is a master this pin functions as an input pin to indicate that a device on the bus is selected. |
| 144 | IDSEL | I | This is a chip select signal that indicates the configuration access. |
| 126 | PCLK | I | PCI bus clock input pin. The maximum clock frequency is 33 MHz. |
| 22 | $\overline{\text{PERR}}$ | I/O | Data parity error input and output pin. |
| 125 | $\overline{\text{SERR}}$ | OD | Address parity error output pin. |

5. Other Signals

| Pin No. | Pin name | I/O | Function | | | | | | | | | | | | | | | |
|--|---------------------------|----------------------------------|---|-------|-------|----------------|---|---|----------------------------------|---|---|----------------------------------|---|---|----------|---|---|------------------------|
| 127 | $\overline{\text{RESET}}$ | O | This pin is used to input system reset signals. | | | | | | | | | | | | | | | |
| 59, 60 | MODE1, MODE0 | I | <p>These pins are used for setting the device operation mode as listed in the table below.</p> <table border="1"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>Operation Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>16-bit bus mode (68 series mode)</td> </tr> <tr> <td>0</td> <td>1</td> <td>16-bit bus mode (80 series mode)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>1</td> <td>PCI bus interface mode</td> </tr> </tbody> </table> | MODE1 | MODE0 | Operation Mode | 0 | 0 | 16-bit bus mode (68 series mode) | 0 | 1 | 16-bit bus mode (80 series mode) | 1 | 0 | Reserved | 1 | 1 | PCI bus interface mode |
| MODE1 | MODE0 | Operation Mode | | | | | | | | | | | | | | | | |
| 0 | 0 | 16-bit bus mode (68 series mode) | | | | | | | | | | | | | | | | |
| 0 | 1 | 16-bit bus mode (80 series mode) | | | | | | | | | | | | | | | | |
| 1 | 0 | Reserved | | | | | | | | | | | | | | | | |
| 1 | 1 | PCI bus interface mode | | | | | | | | | | | | | | | | |
| 50 | $\overline{\text{INT}}$ | O/ OD | Interrupt output pin. Either totem pole or open-drain output buffer can be selected. This pin has an internal pull-up resistor. | | | | | | | | | | | | | | | |
| 6, 18, 31, 43, 49, 63, 73, 107, 116, 131, 137 | V _{DD} | — | Power supply pin | | | | | | | | | | | | | | | |
| 2, 8, 12, 16, 21, 25, 30, 35, 40, 45, 53, 58, 66, 77, 82, 88, 93, 98, 102, 112, 122, 128, 134, 140 | V _{SS} | — | Ground pin | | | | | | | | | | | | | | | |
| 51, 52 | PO1, PO0 | O | General purpose output ports that can control the external active SCSI bus terminator etc. Initial signal level on each pin is "L". Those pins are available only for PCI bus interface mode. | | | | | | | | | | | | | | | |
| 55, 56 | PI1, PI0 | IU | General purpose input ports. Available only for PCI bus interface mode. | | | | | | | | | | | | | | | |
| 57 | N.C. | — | No connection and unused pins. These pins exist on the only PCI bus mode. These are internally pulled-up, and do not connect to the pins. | | | | | | | | | | | | | | | |

I : Input pin

O : Output pin

I/O : Input and Output pin

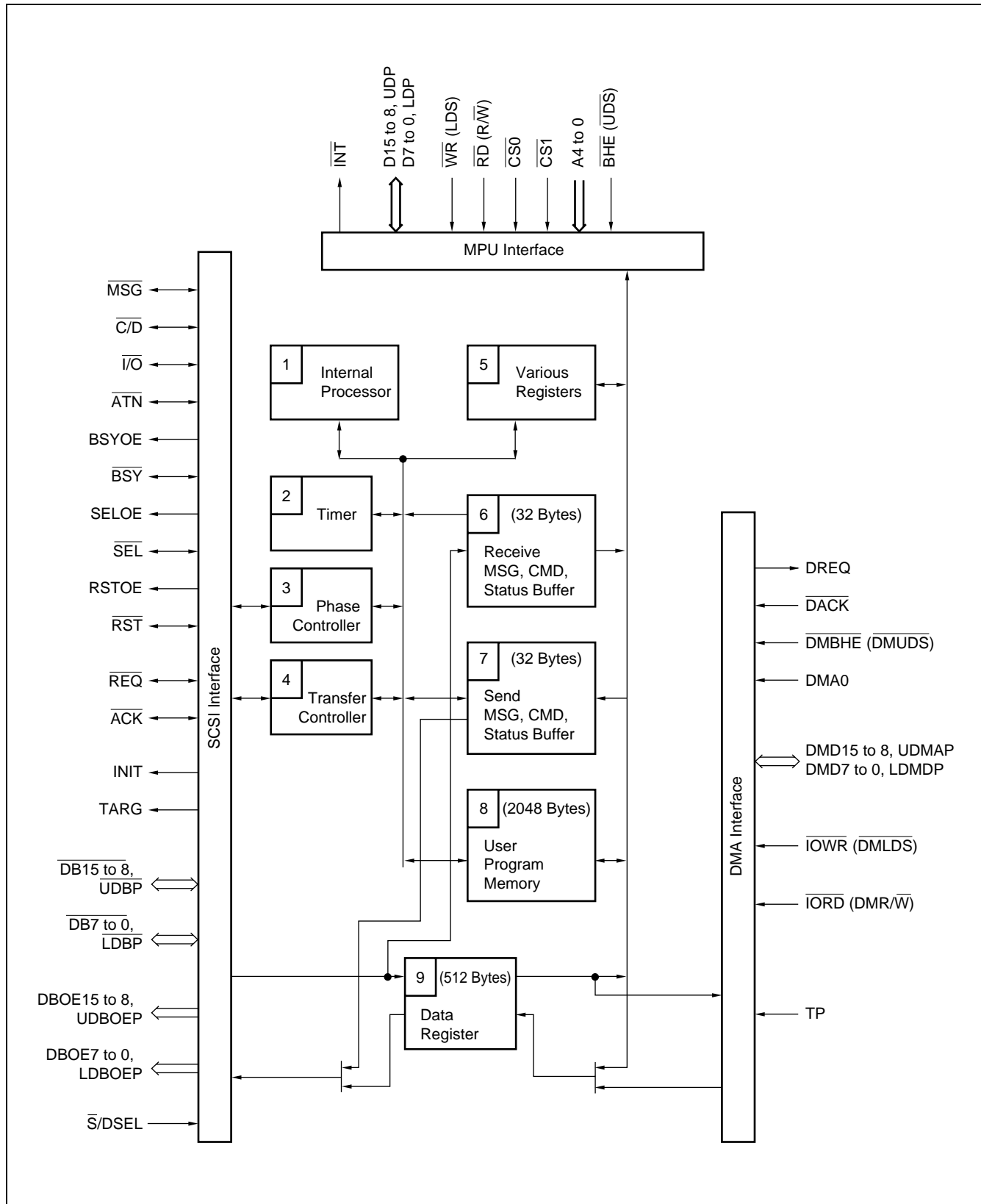
OD : Open-drain output pin

IU : Input pin with pull-up resistor

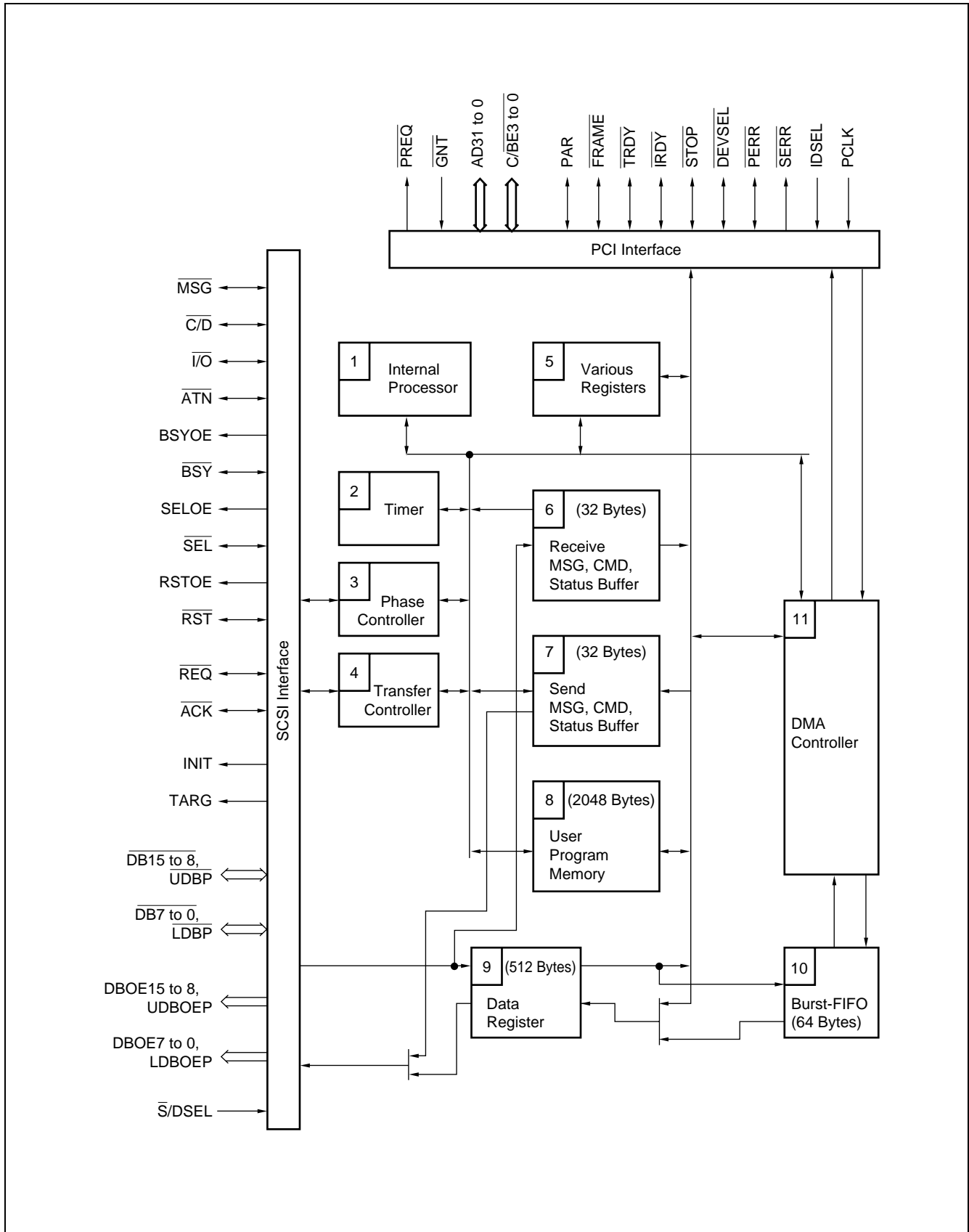
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■ BLOCK DIAGRAM

1. 16-Bit Bus Mode



2. PCI Bus Interface Mode



■ BLOCK FUNCTIONS

1. Internal Processor

This processor provides the sequence control between each phase.

2. Timer

This timer manages the time specified by SCSI and the following time:

- REQ/ACK assertion time for data at asynchronous transfer
- Selection/reselection retry time
- Selection/reselection timeout time
- REQ/ACK timeout time during transfer
 - Asynchronous transfer (target) : Time required for initiator to assert ACK signal after asserting REQ signal
 - Asynchronous transfer (initiator) : Time required for target to negate REQ signal after asserting ACK signal
 - Synchronous transfer (target only) : Time required for target to receive ACK signal for setting offset value to 0 from initiator after sending REQ signal

3. Phase Controller

This controller controls the arbitration, selection/reselection, data-in/out, command, status, and message-in/out phases executed on the SCSI bus.

4. Transfer Controller

This controller controls the information (data, command, status, message) transfer phases executed on the SCSI bus.

There are two types of transfer for executing the information transfer phases.

- Asynchronous transfer : Control by interlocking REQ and ACK signals
- Synchronous transfer : Control with maximum of 32-byte offset value in data-in/out phase

Depending on the data migration, there are the following two modes.

- Program transfer : Performed via MPU interface using data registers
- DMA transfer : Performed via DMA interface using DREQ and $\overline{\text{DACK}}$ pins

At synchronous transfer, the transfer parameters (transfer mode, minimum cycle period of REQ or ACK signal sent from SPC in synchronous transfer, and maximum value between REQ and ACK signals in synchronous transfer) can be saved for each ID and are automatically set when the data phase is started. The transfer byte count is determined by block length \times number of blocks.

5. Various Registers

• Command register

This register specifies each command with an 8-bit code.

When using the user program, specify "1" at the Bit 7. The lower 7 bits (Bit 6 to Bit 0) are invalid.

• Nexus status register

This register indicates the chip's operating condition, the nexused partner's ID, and data register status.

• SCSI control signal status register

This register indicates the status of SCSI control signals.

- **Interrupt status register**

This register indicates the interrupt status with an 8-bit code.

- **Command step register**

This register indicates the execution status of each command with an 8-bit step code. Error causes can be analyzed by referencing the interrupt status register and this register.

- **Group 6/7 command length setting register**

This register sets the group 6/7 command length not defined in the SCSI standard. Setting this register determines the group 6/7 command length.

6. Receive MSG, CMD, Status Buffer (Receive MCS Buffer)

This is a 32-byte receive-only information buffer that holds the information for the message, command, and status received from the SCSI bus.

7. Send MSG, CMD, Status Buffer (Send MCS Buffer)

This is a 32-byte send-only information buffer that holds the information for the message, command, and status sent on the SCSI bus.

8. User Program Memory

This is a 2048-byte program memory that stores programmable commands. It can consist of 1024-byte × 2 banks or 2048-byte × 1 bank.

9. Data Register

This is a 512-byte FIFO data register that holds data in the data phase executed on the SCSI bus.

10. Burst FIFO

64-byte FIFO type data buffer to perform burst transfer during the PCI bus interface mode. The device has total 576-byte FIFO with Data Register and Burst FIFO in the PCI bus interface mode.

11. DMA Controller

This is a 32-bit DMA Controller that performs data transfer. This DMAC is a bus master during the PCI bus interface mode.

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■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|-------------------------------|------------------|----------------------|----------------------|------|
| | | Min. | Max. | |
| Supply voltage* | V _{DD} | V _{SS} -0.5 | 6.0 | V |
| Input voltage* | V _I | V _{SS} -0.5 | V _{DD} +0.5 | V |
| Output voltage* | V _O | V _{SS} -0.5 | V _{DD} +0.5 | V |
| Operating ambient temperature | T _{op} | -25 | +85 | °C |
| Storage temperature | T _{stg} | -40 | +125 | °C |

* : The voltages are based on V_{SS} (= 0V)

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|----------------------------|-------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| Supply voltage* | V _{DD} | 4.75 | 5.0 | 5.25 | V |
| SCSI clock input frequency | f _{SCSI} | 20.0 | — | 40.0 | MHz |
| PCI clock input frequency | f _{PCI} | — | — | 33.0 | MHz |
| Operating temperature | T _a | 0 | — | +70 | °C |

* : The voltages are based on V_{SS} (= 0V)

Note: The recommended operating conditions are the recommended values for assuring normal logic operation of the LSI. Requirements in electrical characteristics (DC and AC characteristics) are assured within the range of the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

($V_{DD} = +5 V \pm 5\%$, $V_{SS} = 0 V$, $T_a = 0$ to $+70^\circ C$)

| Parameter | | | | Symbol | Condition | Value | | Unit | |
|--------------------------------|-------------------------|--------------------|--|-----------|-----------------------------|-----------------------------|------|---------|---|
| | | | | | | Min. | Max. | | |
| Input voltage*1 | SCSI pins | | | V_{IH} | — | 1.9 | — | V | |
| | | | | V_{IL} | — | — | 1.0 | V | |
| | SCLK pins SDSEL pins | | | V_{IH} | — | 2.4 | — | V | |
| | | | | V_{IL} | — | — | 0.8 | V | |
| | Other pins | | | V_{IH} | — | 2.0 | — | V | |
| | | | | V_{IL} | — | — | 0.8 | V | |
| SCSI-pin input hysteresis*1 | | | | V_{HW} | — | 0.3 | — | V | |
| Output voltage*1 | SCSI pins | In single-end mode | $\overline{REQ}, \overline{ACK}$ | | V_{OH} | $I_{OH} = -7.0 \text{ mA}$ | 2.0 | 3.24 | V |
| | | | | | V_{OL} | $I_{OL} = +48.0 \text{ mA}$ | — | 0.5 | V |
| | | | $\overline{RST}, \overline{BSY}, \overline{SEL}$ | | V_{OL} | $I_{OL} = +48.0 \text{ mA}$ | — | 0.5 | V |
| | | Others | Non-3ST. | V_{OL} | $I_{OL} = +48.0 \text{ mA}$ | — | 0.5 | V | |
| | | | 3ST. | V_{OH} | $I_{OH} = -7.0 \text{ mA}$ | 2.0 | 3.24 | V | |
| | | | | V_{OL} | $I_{OL} = +48.0 \text{ mA}$ | — | 0.5 | V | |
| | In differential mode | | | | V_{OH} | $I_{OH} = -7.0 \text{ mA}$ | 2.0 | 3.24 | V |
| | | | | | V_{OL} | $I_{OL} = +3.2 \text{ mA}$ | — | 0.4 | V |
| | PCI bus interface pins | | | | V_{OH} | $I_{OH} = -2.0 \text{ mA}$ | 4.2 | — | V |
| | | | | | V_{OL} | $I_{OL} = +6.0 \text{ mA}$ | — | 0.55 | V |
| | Other pins | | | | V_{OH} | $I_{OH} = -2.0 \text{ mA}$ | 4.2 | — | V |
| | | | | | V_{OL} | $I_{OL} = +3.2 \text{ mA}$ | — | 0.4 | V |
| Input leakage current | | | | I_{LI} | $V_{IN} = 0$ to V_{DD} | -10 | +10 | μA | |
| Input/output leakage current*2 | | | | I_{LOZ} | $V_{IN} = 0$ to V_{DD} | -10 | +10 | μA | |
| Supply current | | | | I_{DD} | — | — | 150 | mA | |

3ST. : Three-state mode

*1 : SCSI pins are; \overline{UDBP} , $\overline{DB15}$ to $\overline{DB8}$, \overline{LDBP} , $\overline{DB7}$ to $\overline{DB0}$, \overline{BSY} , \overline{SEL} , \overline{RST} , \overline{ATN} , \overline{REQ} , \overline{ACK} , \overline{MSG} , $\overline{C/D}$ and $\overline{I/O}$. (Total 27 pins)

*2 : Leak current when the three-state output pin output and the bidirectional bus pin output are in a high impedance state.

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2. Input/Output Pin Capacitance

($V_{DD} = V_{IN} = 0\text{ V}$, $f = 1\text{ MHz}$, $T_a = +25^\circ\text{C}$)

| Parameter | Pin name | Symbol | Conditions | | Unit |
|------------------------------|------------------|-----------|------------|------|------|
| | | | Min. | Max. | |
| Input-pin capacitance | SCLK, PCLK (TP) | C_{IN} | — | 12 | pF |
| | Other input pins | | — | 8 | pF |
| Output-pin capacitance | | C_{OUT} | — | 10 | pF |
| Input/output-pin capacitance | Non-SCSI pins | $C_{I/O}$ | — | 10 | pF |
| | SCSI pins | | — | 25 | pF |

3. Load Conditions for Measurement of AC Characteristics

(1) Non-SCSI pins

($V_{DD} = +5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

16-bit bus mode

| Pin name | C_L |
|--|-------|
| INT, DREQ | 60 pF |
| D15 to D8, UDP, D7 to D0, LDP, DMD15 to DMD8, UDMDP, DMD7 to DMD0, LDMDP | 85 pF |

PCI bus interface mode

| Pin name | C_L |
|--------------|-------|
| PCI bus pins | 50 pF |

(2) SCSI pins

($V_{DD} = +5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

| | |
|------------------|------------------------|
| Load resistance | $R_{L1} = 110\ \Omega$ |
| | $R_{L2} = 165\ \Omega$ |
| Load capacitance | $C_L = 200\ \text{pF}$ |

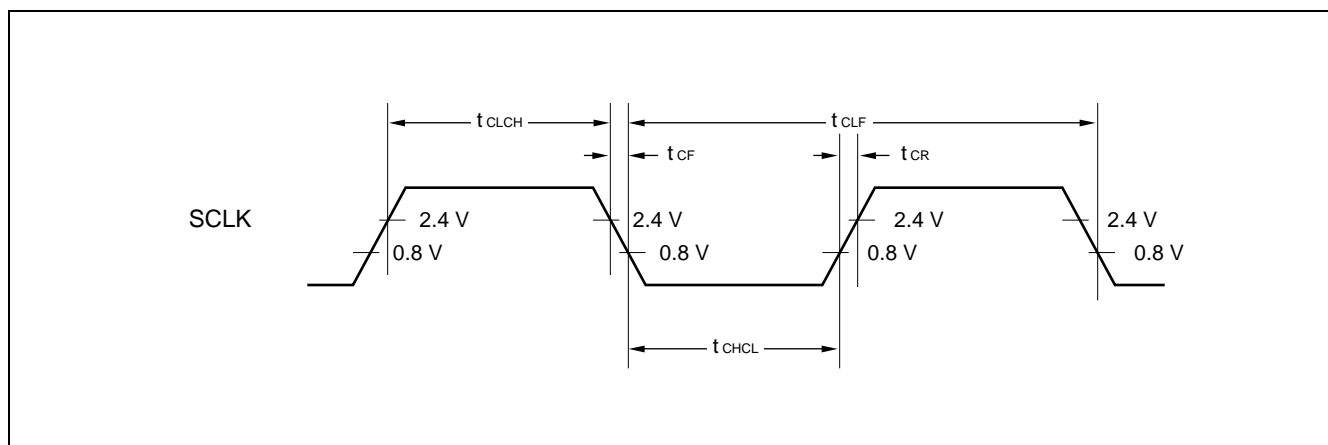
4. AC Characteristics

(1) System clock

- SCSI clock (SCLK pin)

| Parameter | Symbol | Value | | | Unit |
|--------------------------|-------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| Clock period | t _{CLF} | 25.0 | — | 50.0 | ns |
| Clock pulse width (Low) | t _{CLCH} | 10.0 | — | — | ns |
| Clock pulse width (High) | t _{CHCL} | 10.0 | — | — | ns |
| Clock pulse rise time | t _{CR} | — | — | 5.0 | ns |
| Clock pulse fall time | t _{CF} | — | — | 5.0 | ns |

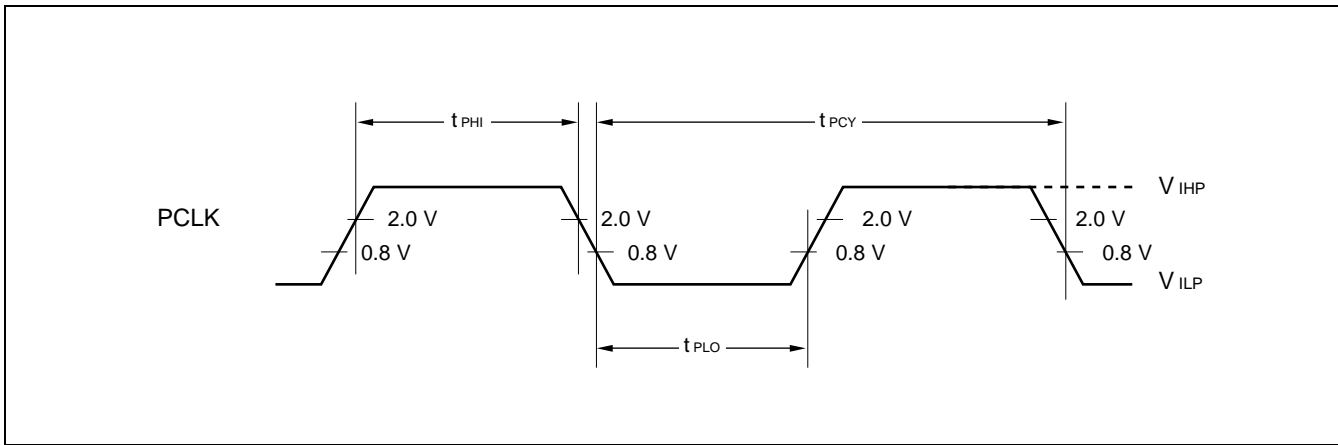
Note: When the internal operating clock frequency is the same as the input clock frequency, (when using the device in divide-by-1 mode), the clock pulse width for L and H levels must have minimum 20.0 ns or longer.
 (i.e. When the clock conversion register value is 0Bh (address: 10h in the initial setting registers) and input clock frequency = 20 MHz.)



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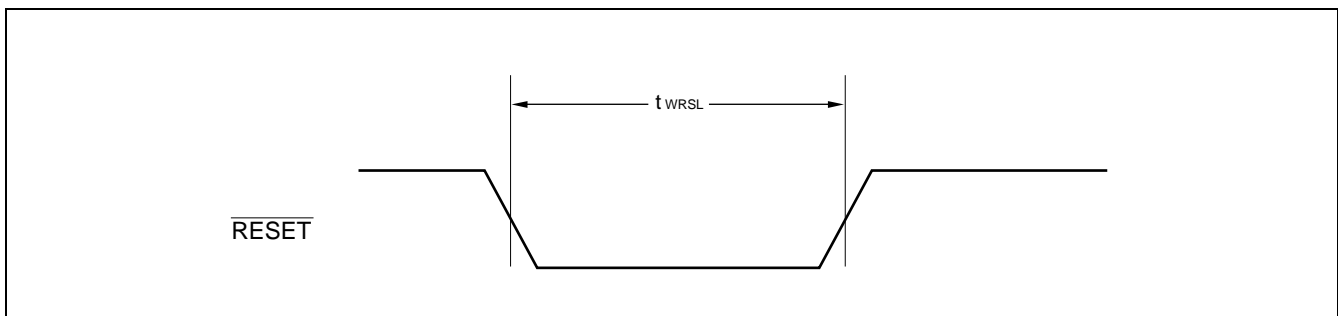
• PCI clock (PCLK pin)

| Parameter | Symbol | Value | | | Unit |
|--------------------------|---------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| Clock frequency | t_{PCY} | 30.0 | — | — | ns |
| Clock pulse width (Low) | t_{PLO} | 12.0 | — | — | ns |
| Clock pulse width (High) | t_{PHI} | 12.0 | — | — | ns |
| Clock slew rate | t_{PSR} | 1.0 | — | 4.0 | V/ns |
| Clock amplitude | $V_{IHP} - V_{ILP}$ | 2.0 | — | — | V |



(2) System reset

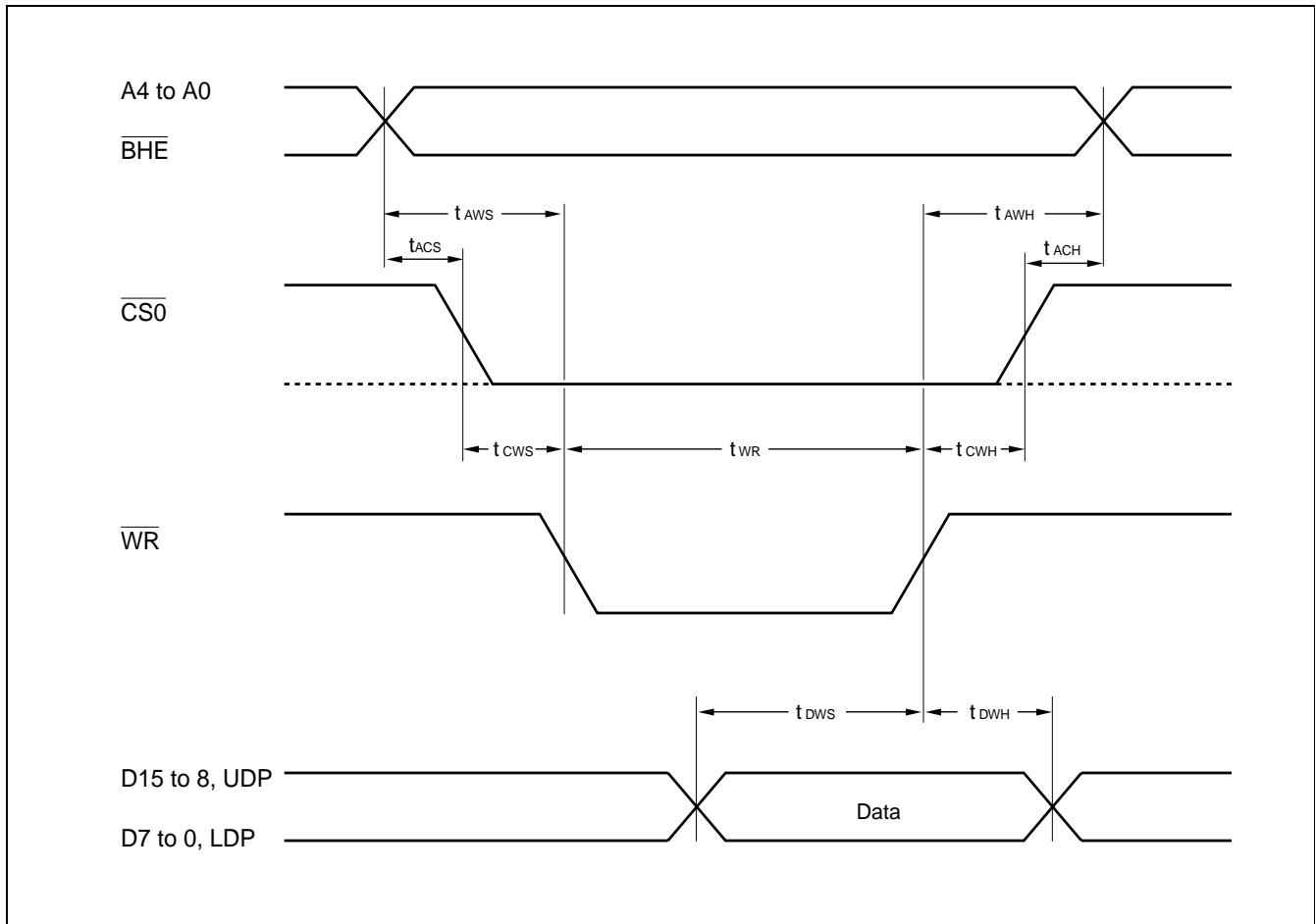
| Parameter | Symbol | Value | | | Unit |
|---|------------|-------------|------|------|------|
| | | Min. | Typ. | Max. | |
| Reset ($\overline{\text{RESET}}$) pulse "L" level pulse width | t_{WRSL} | $4 t_{CLF}$ | — | — | ns |



5. MPU Interface

(1) Register write timing for 80 series

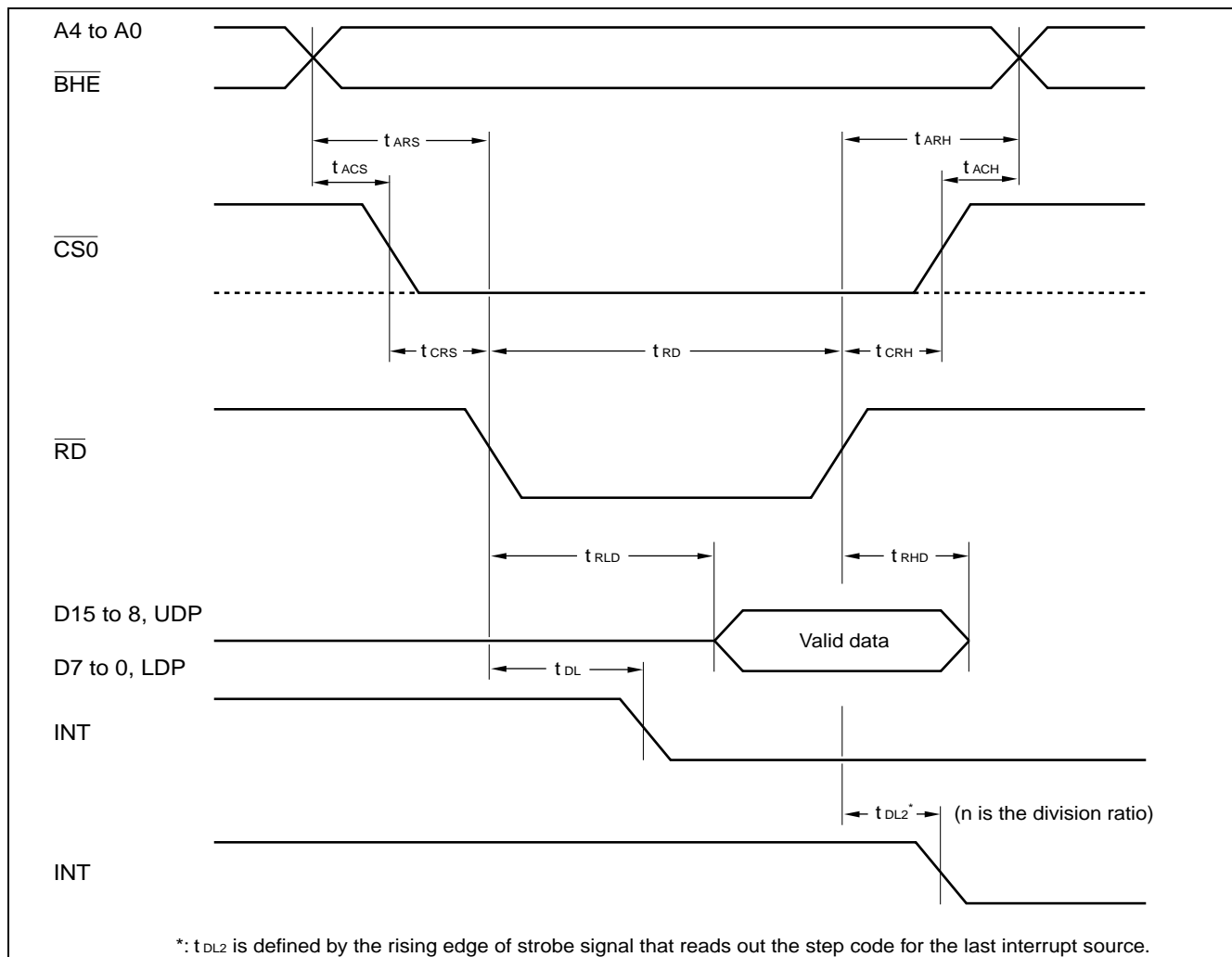
| Parameter | Symbol | Value | | Unit |
|--|------------------|-------|------|------|
| | | Min. | Max. | |
| Address (A4 to A0), $\overline{\text{BHE}}$ setup time (1) | t_{AWS} | 20 | — | ns |
| Address (A4 to A0) hold time (1) | t_{AWH} | 10 | — | ns |
| Address (A4 to A0), $\overline{\text{BHE}}$ setup time (2) | t_{ACS} | 10 | — | ns |
| Address (A4 to A0) hold time (2) | t_{ACH} | 5 | — | ns |
| $\overline{\text{CS0}}$ setup time | t_{CWS} | 10 | — | ns |
| $\overline{\text{CS0}}$ hold time | t_{CWH} | 5 | — | ns |
| Data set up time | t_{DWS} | 25 | — | ns |
| Data hold time | t_{DWH} | 10 | — | ns |
| $\overline{\text{WR}}$ "L" level pulse width | t_{WR} | 70 | — | ns |



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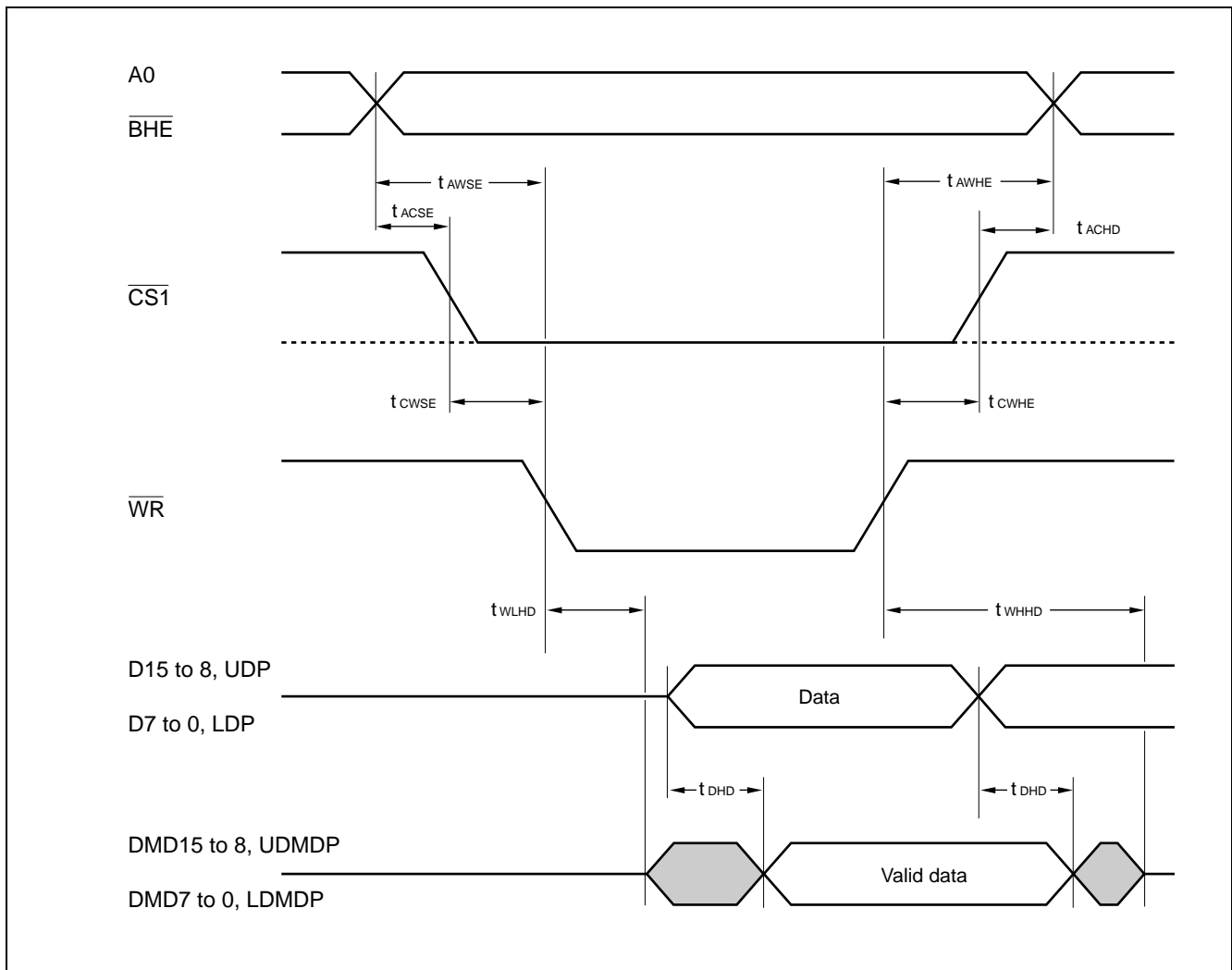
(2) Register read timing for 80 series

| Parameter | Symbol | Value | | Unit | |
|--|-------------------------|------------------|------|-------------------------------|----|
| | | Min. | Max. | | |
| Address (A4 to A0), $\overline{\text{BHE}}$ setup time (1) | t_{ARS} | 20 | — | ns | |
| Address (A4 to A0) hold time (1) | t_{ARH} | 10 | — | ns | |
| Address (A4 to A0), $\overline{\text{BHE}}$ setup time (2) | t_{ACS} | 10 | — | ns | |
| Address (A4 to A0) hold time (2) | t_{ACH} | 5 | — | ns | |
| $\overline{\text{CS0}}$ setup time | t_{CRS} | 10 | — | ns | |
| $\overline{\text{CS0}}$ hold time | t_{CRH} | 5 | — | ns | |
| $\overline{\text{RD}}$ set Low → data output defined time | t_{RLD} | — | 40 | ns | |
| $\overline{\text{RD}}$ set High → data output defined time | t_{RHD} | 5 | — | ns | |
| $\overline{\text{RD}}$ pulse duration at Low | t_{RD} | 70 | — | ns | |
| INT signal clear time | Interrupt non-hold mode | t_{DL} | — | 50 | ns |
| | Interrupt hold mode | t_{DL2} | — | $n \cdot t_{\text{CLF}} + 50$ | ns |



(3) Register write timing for 80 series (for external access)

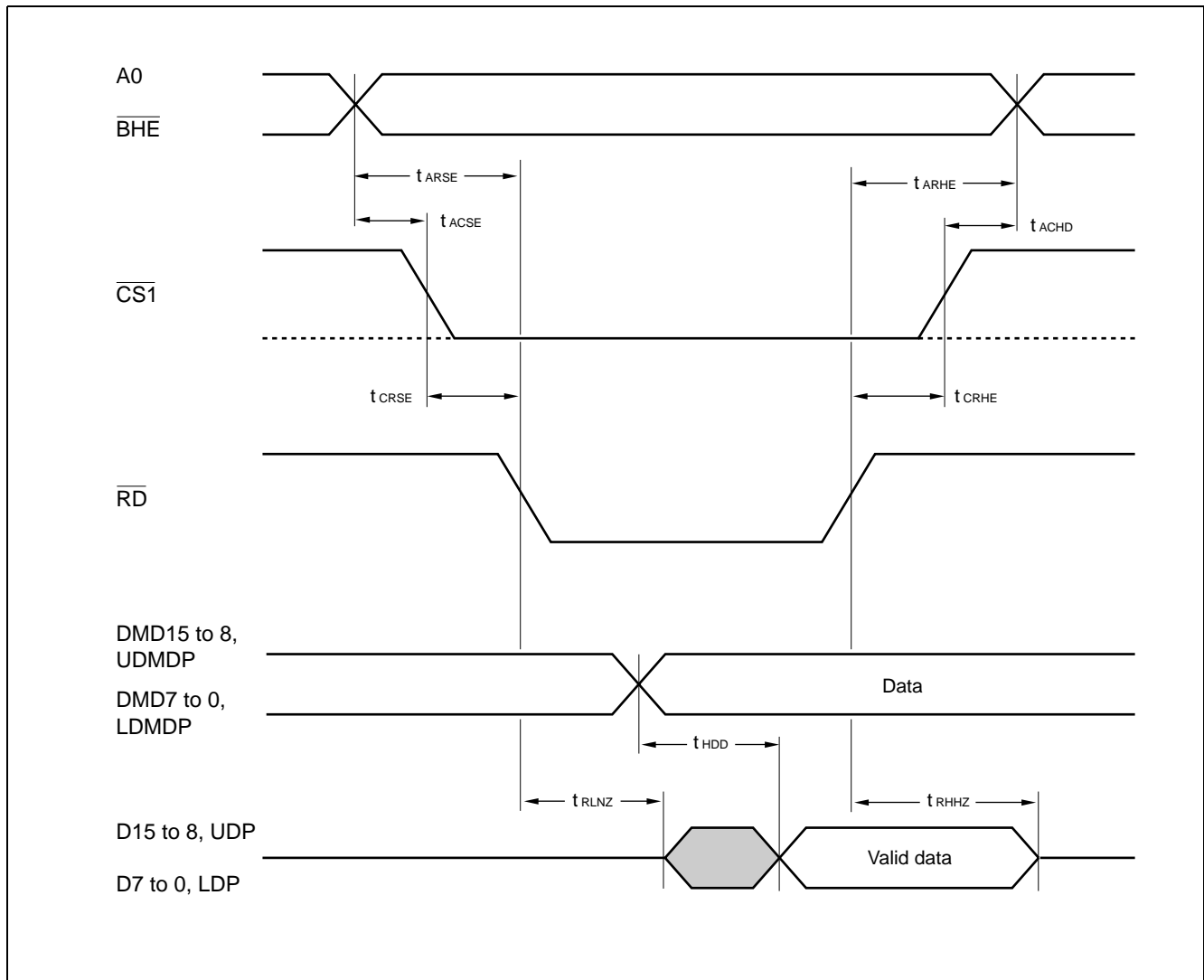
| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------|------|------|
| | | Min. | Max. | |
| Address (A0), $\overline{\text{BHE}}$ setup time (1) | t_{AWSE} | 20 | — | ns |
| Address (A0) hold time (1) | t_{AWHE} | 10 | — | ns |
| Address (A0), $\overline{\text{BHE}}$ setup time (2) | t_{ACSE} | 10 | — | ns |
| Address (A0) hold time (2) | t_{ACHD} | 5 | — | ns |
| $\overline{\text{CS1}}$ setup time | t_{CWSE} | 10 | — | ns |
| $\overline{\text{CS1}}$ hold time | t_{CWHE} | 5 | — | ns |
| $\overline{\text{WR}}$ set Low → DMA bus output delay time | t_{WLHD} | — | 40 | ns |
| $\overline{\text{WR}}$ set High → DMA bus output undefined time | t_{WHHD} | 5 | — | ns |
| MPU data bus → DMA bus output delay time | t_{DHD} | — | 20 | ns |



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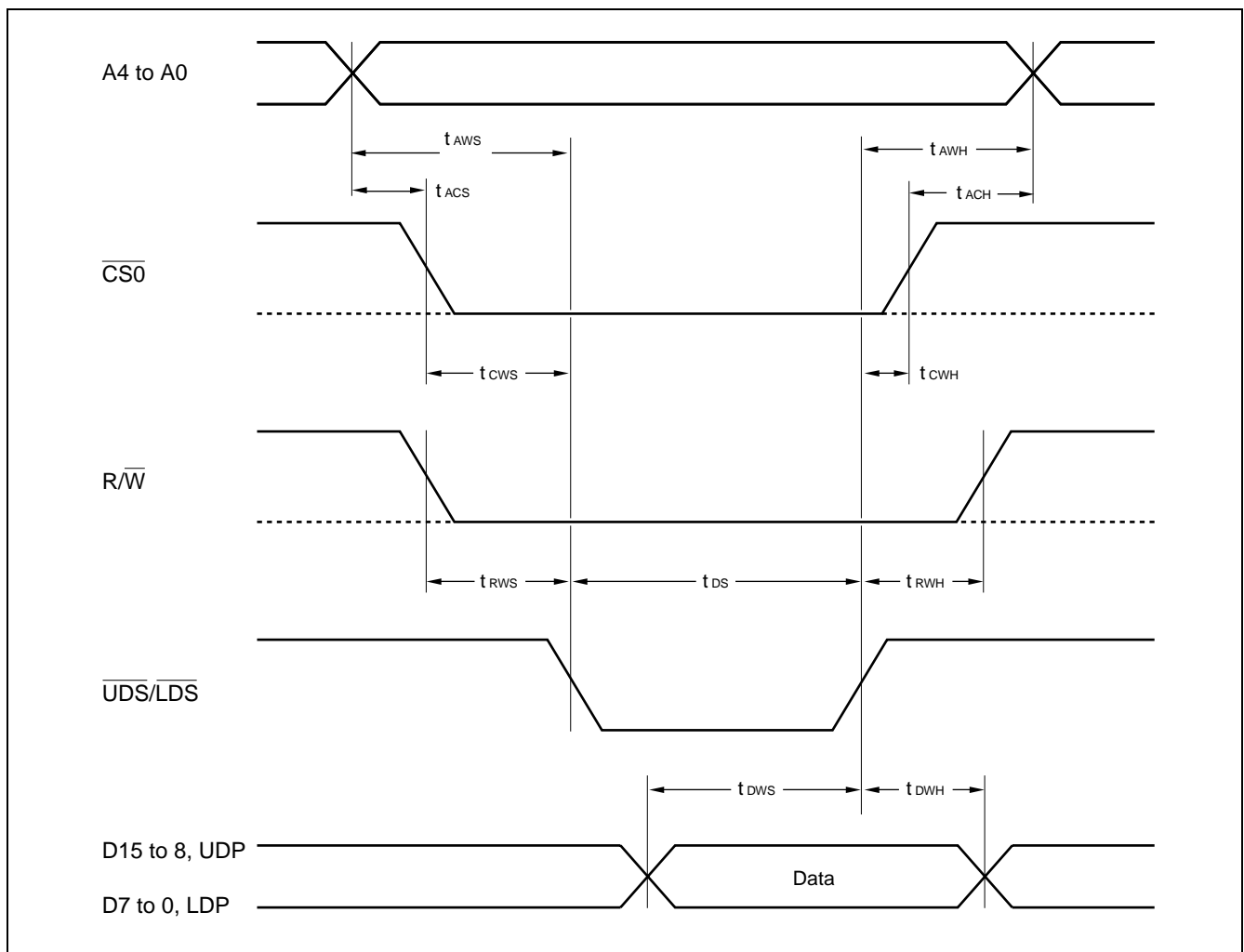
(4) Register read timing for 80 series (for external access)

| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------|------|------|
| | | Min. | Max. | |
| Address (A0), $\overline{\text{BHE}}$ setup time (1) | t_{ARSE} | 20 | — | ns |
| Address (A0), $\overline{\text{BHE}}$ hold time (1) | t_{ARHE} | 10 | — | ns |
| Address (A0), $\overline{\text{BHE}}$ setup time (2) | t_{ACSE} | 10 | — | ns |
| Address (A0), $\overline{\text{BHE}}$ hold time (2) | t_{ACHD} | 5 | — | ns |
| $\overline{\text{CS1}}$ setup time | t_{CRSE} | 10 | — | ns |
| $\overline{\text{CS1}}$ hold time | t_{CRHE} | 5 | — | ns |
| $\overline{\text{RD}}$ set Low → MPU bus output enable time | t_{RLNZ} | — | 40 | ns |
| $\overline{\text{RD}}$ set High → MPU bus output disable time | t_{RHHZ} | 5 | — | ns |
| DMA data bus → MPU bus output delay time | t_{HDD} | — | 20 | ns |



(5) Register write timing for 68 series

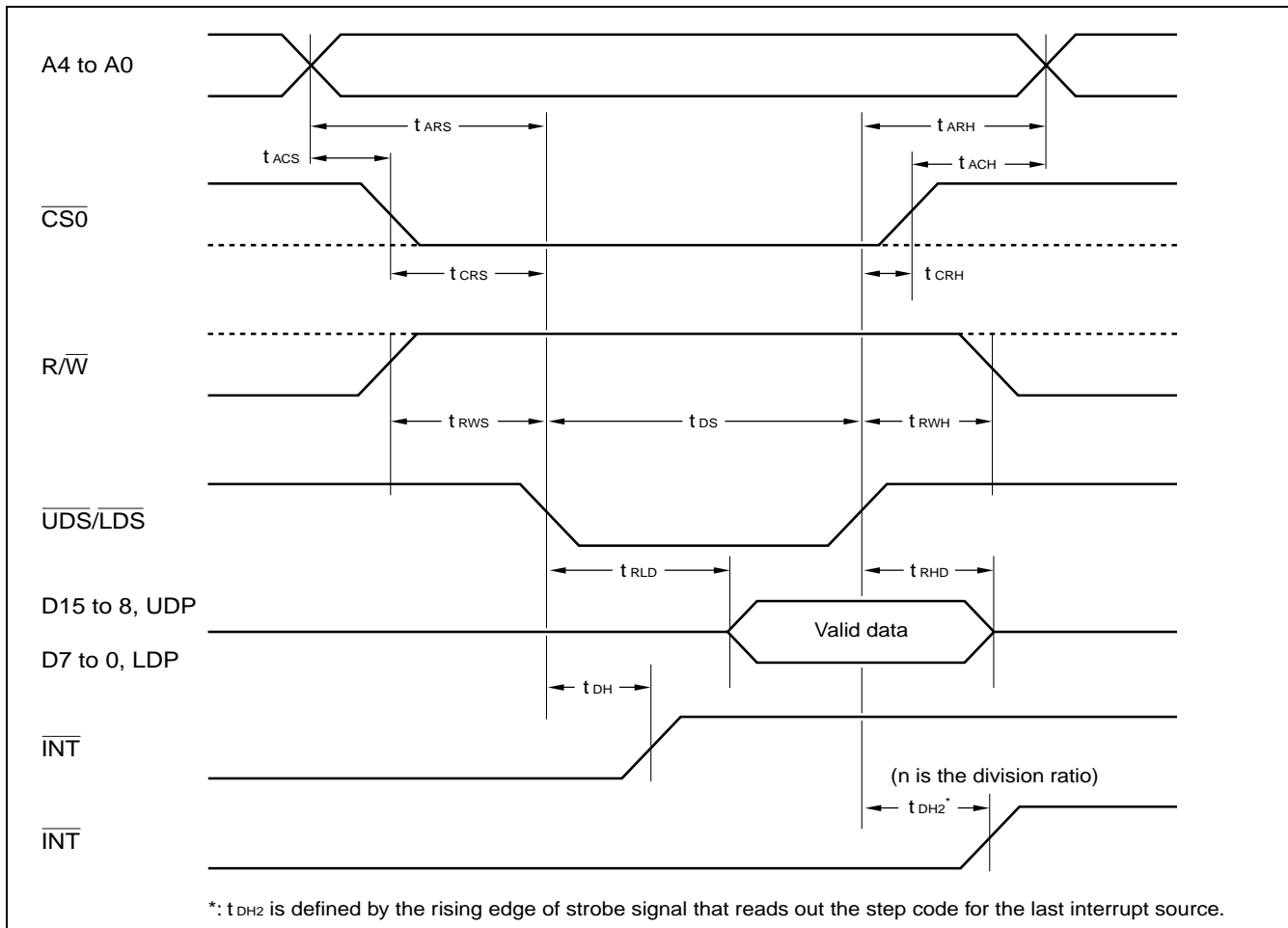
| Parameter | Symbol | Value | | Unit |
|---|-----------|-------|------|------|
| | | Min. | Max. | |
| Address (A4 to A0) setup time (1) | t_{AWS} | 20 | — | ns |
| Address (A4 to A0) hold time (1) | t_{AWH} | 10 | — | ns |
| Address (A4 to A0) setup time (2) | t_{ACS} | 10 | — | ns |
| Address (A4 to A0) hold time (2) | t_{ACH} | 5 | — | ns |
| $\overline{CS0}$ setup time | t_{CWS} | 10 | — | ns |
| $\overline{CS0}$ hold time | t_{CWH} | 5 | — | ns |
| Data setup time | t_{DWS} | 25 | — | ns |
| Data hold time | t_{DWH} | 10 | — | ns |
| $\overline{UDS}/\overline{LDS}$ "L" level pulse width | t_{DS} | 70 | — | ns |
| R/\overline{W} setup time | t_{RWS} | 10 | — | ns |
| R/\overline{W} hold time | t_{RWH} | 10 | — | ns |



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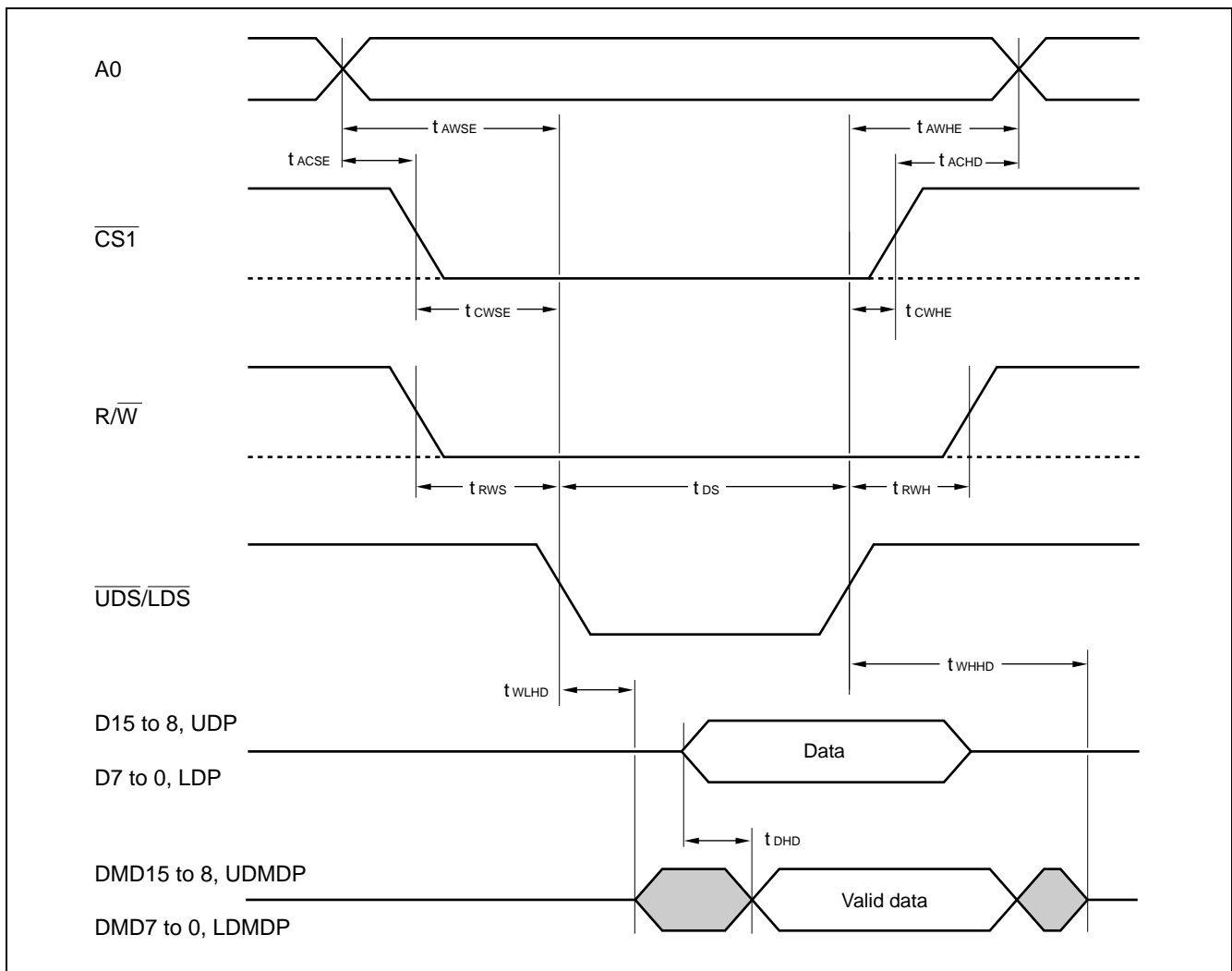
(6) Register read timing for 68 series

| Parameter | Symbol | Value | | Unit |
|---|-----------|-------|------------------------|------|
| | | Min. | Max. | |
| Address (A4 to A0) setup time (1) | t_{ARS} | 20 | — | ns |
| Address (A4 to A0) hold time (1) | t_{ARH} | 10 | — | ns |
| Address (A4 to A0) setup time (2) | t_{ACS} | 10 | — | ns |
| Address (A4 to A0) hold time (2) | t_{ACH} | 5 | — | ns |
| $\overline{CS0}$ setup time | t_{CRS} | 10 | — | ns |
| $\overline{CS0}$ hold time | t_{CRH} | 5 | — | ns |
| Data output defined time | t_{RLD} | — | 40 | ns |
| Data output disable time | t_{RHD} | 5 | — | ns |
| $\overline{UDS}/\overline{LDS}$ "L" level pulse width | t_{DS} | 70 | — | ns |
| R/\overline{W} setup time | t_{RWS} | 10 | — | ns |
| R/\overline{W} hold time | t_{RWH} | 10 | — | ns |
| \overline{INT} signal clear time | t_{DH} | — | 50 | ns |
| | t_{DH2} | — | $n \cdot t_{CLK} + 50$ | |



(7) Register write timing for 68 series (for external access)

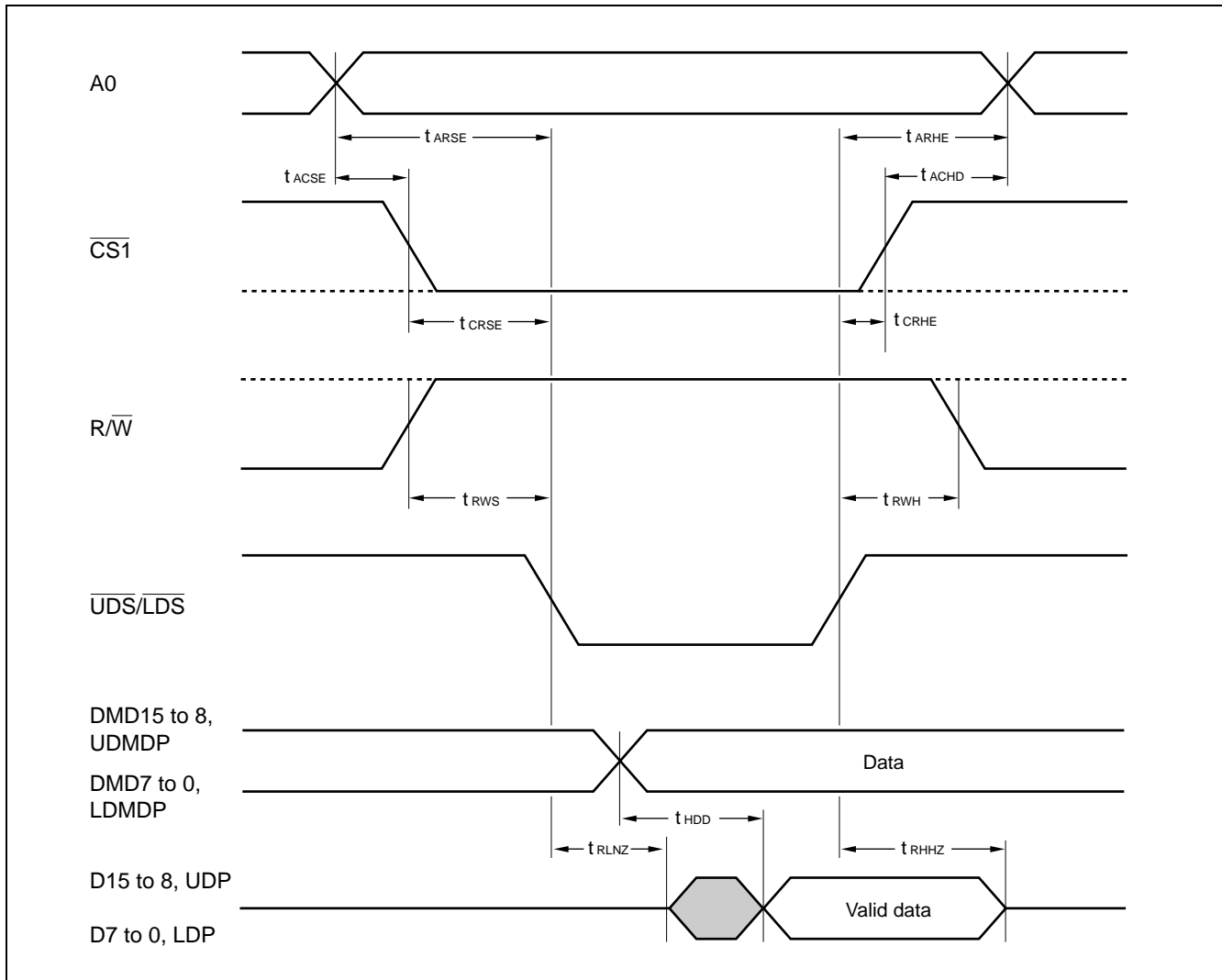
| Parameter | Symbol | Value | | Unit |
|--|------------|-------|------|------|
| | | Min. | Max. | |
| Address (A0) setup time (1) | t_{AWSE} | 20 | — | ns |
| Address (A0) hold time (1) | t_{AWHE} | 10 | — | ns |
| Address (A0) setup time (2) | t_{ACSE} | 10 | — | ns |
| Address (A0) hold time (2) | t_{ACHD} | 5 | — | ns |
| $\overline{CS1}$ setup time | t_{CWSE} | 10 | — | ns |
| $\overline{CS1}$ hold time | t_{CWHE} | 5 | — | ns |
| $\overline{UDS}/\overline{LDS}$ set Low → DMA bus output delay time | t_{WLHD} | — | 40 | ns |
| $\overline{UDS}/\overline{LDS}$ set High → DMA bus output undefined time | t_{WHHD} | 5 | — | ns |
| MPU data bus → DMA bus output delay time | t_{DHD} | — | 20 | ns |
| R/\overline{W} setup time | t_{RWS} | 10 | — | ns |
| R/\overline{W} hold time | t_{RWH} | 10 | — | ns |



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(8) Register read timing for 68 series (for external access)

| Parameter | Symbol | Value | | Unit |
|--|------------|-------|------|------|
| | | Min. | Max. | |
| Address (A0) setup time (1) | t_{ARSE} | 20 | — | ns |
| Address (A0) hold time (1) | t_{ARHE} | 10 | — | ns |
| Address (A0) setup time (2) | t_{ACSE} | 10 | — | ns |
| Address (A0) hold time (2) | t_{ACHD} | 5 | — | ns |
| $\overline{CS1}$ setup time | t_{CRSE} | 10 | — | ns |
| $\overline{CS1}$ hold time | t_{CRHE} | 5 | — | ns |
| $\overline{UDS/LDS}$ set Low → MPU data bus output enable time | t_{RLNZ} | — | 40 | ns |
| $\overline{UDS/LDS}$ set High → MPU data bus output disable time | t_{RHH} | 5 | — | ns |
| DMA bus → MPU data bus output delay time | t_{HDD} | — | 20 | ns |
| R/\overline{W} setup time | t_{RWS} | 10 | — | ns |
| R/\overline{W} hold time | t_{RWH} | 10 | — | ns |



6. DMA Interface

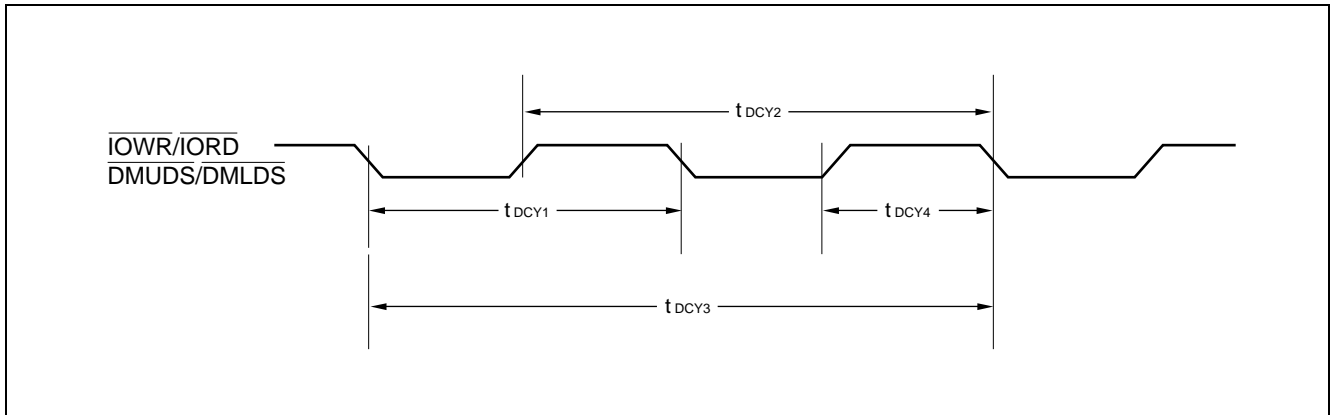
DMA access timing

The time regulations are not applicable in the following cases:

- During SCSI input and when data buffer EMPTY, or when one byte held
- During SCSI output and when data buffer FULL, or when 511 bytes held
- When parity error detected (target)
- When error stopping transfer occurs in SCSI interface

(1) Access cycle time (burst mode)

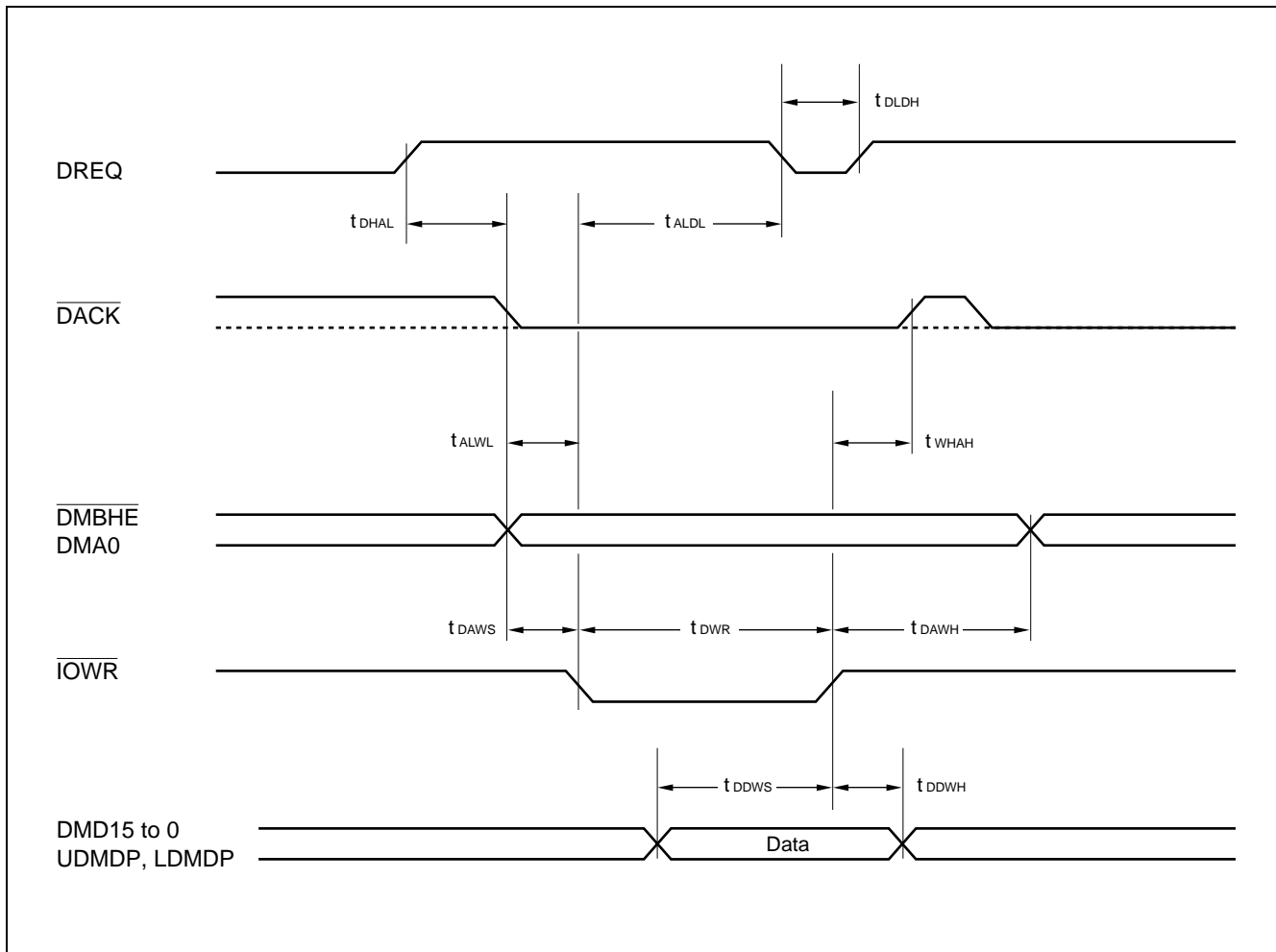
| Parameter | Symbol | Value | | Unit |
|--------------------|-------------------|--------------------|------|------|
| | | Min. | Max. | |
| Address cycle time | t _{DCY1} | 2 t _{CLF} | — | ns |
| | t _{DCY2} | 3 t _{CLF} | — | ns |
| | t _{DCY3} | 4 t _{CLF} | — | ns |
| | t _{DCY4} | 1 t _{CLF} | — | ns |



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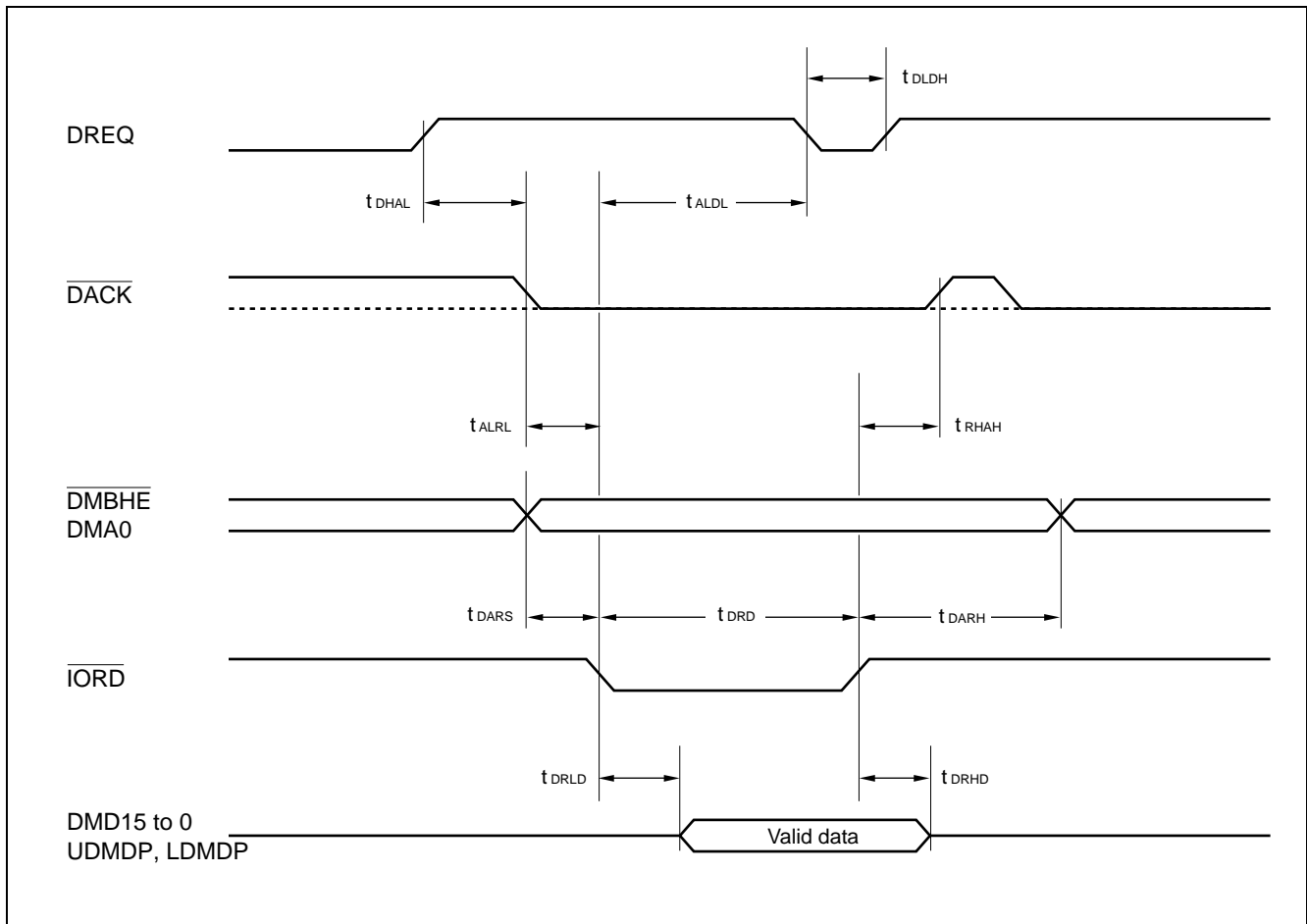
(2) Write timing (burst mode for 80 series)

| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------|------|------|
| | | Min. | Max. | |
| DREQ set High → $\overline{\text{DACK}}$ set Low | t_{DHAL} | 0 | — | ns |
| $\overline{\text{IOWR}}$ set Low → DREQ set Low | t_{ALDL} | — | 25 | ns |
| DREQ set Low → DREQ set High | t_{DLDH} | 0 | — | ns |
| $\overline{\text{DACK}}$ set Low → $\overline{\text{IOWR}}$ set Low | t_{ALWL} | 0 | — | ns |
| $\overline{\text{DMBHE}}$, DMA0 setup time | t_{DAWS} | 10 | — | ns |
| $\overline{\text{IOWR}}$ "L" level pulse width | t_{DWR} | 25 | — | ns |
| $\overline{\text{IOWR}}$ set High → $\overline{\text{DACK}}$ set High | t_{WHAH} | 0 | — | ns |
| $\overline{\text{DMBHE}}$, DMA0 hold time | t_{DAWH} | 10 | — | ns |
| Input data setup time | t_{DDWS} | 25 | — | ns |
| Input data hold time | t_{DDWH} | 5 | — | ns |



(3) Read timing (burst mode for 80 series)

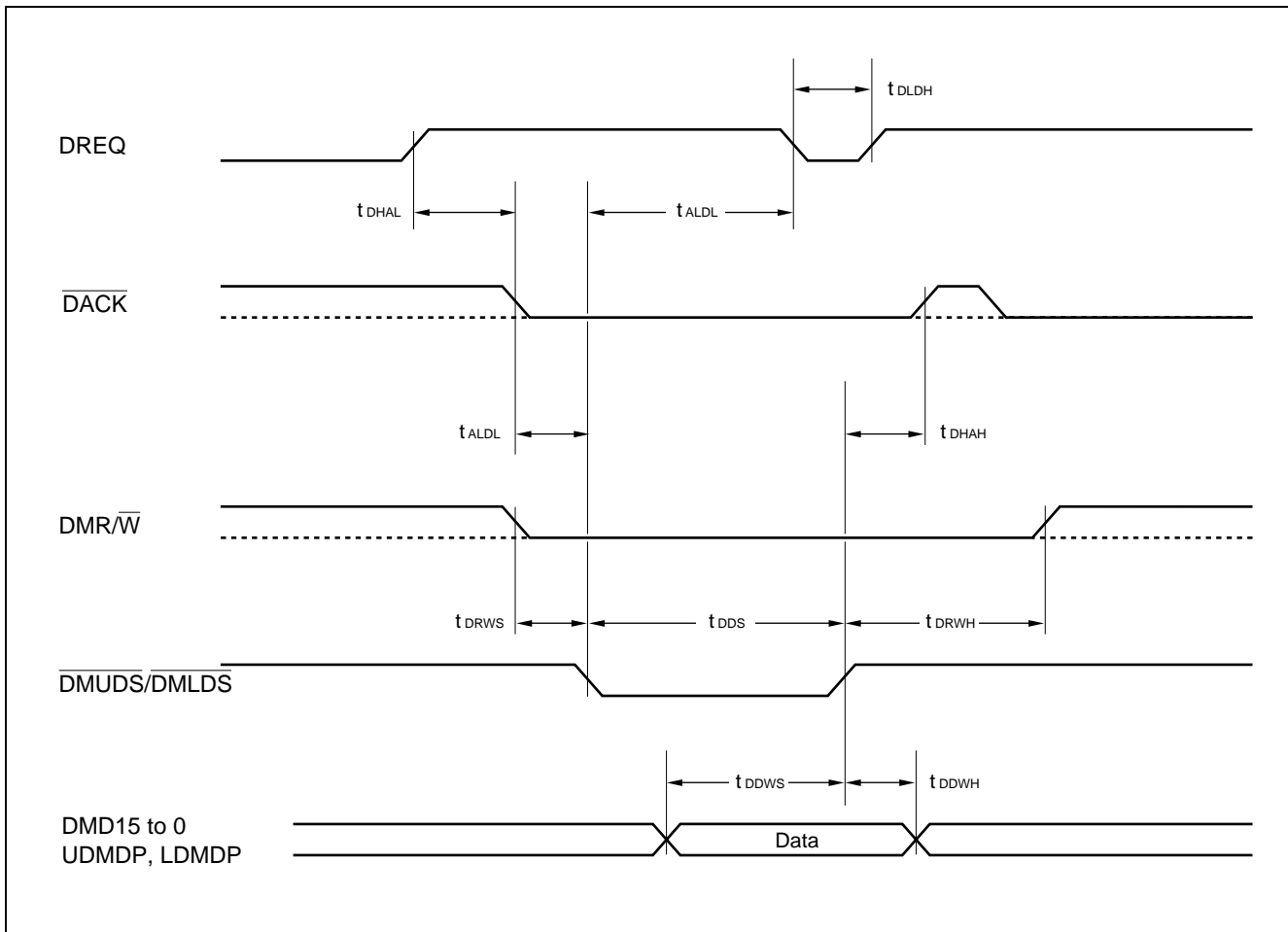
| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------|------|------|
| | | Min. | Max. | |
| DREQ set High → $\overline{\text{DACK}}$ set Low | t_{DHAL} | 0 | — | ns |
| $\overline{\text{IORD}}$ set Low → DREQ set Low | t_{ALDL} | — | 25 | ns |
| DREQ set Low → DREQ set High | t_{DLDH} | 0 | — | ns |
| $\overline{\text{DACK}}$ set Low → $\overline{\text{IORD}}$ set Low | t_{ALRL} | 0 | — | ns |
| $\overline{\text{DMBHE}}$, DMA0 setup time | t_{DARS} | 10 | — | ns |
| $\overline{\text{IORD}}$ "L" level pulse width | t_{DRD} | 25 | — | ns |
| $\overline{\text{IORD}}$ set High → $\overline{\text{DACK}}$ set High | t_{RHAH} | 0 | — | ns |
| $\overline{\text{DMBHE}}$, DMA0 hold time | t_{DARH} | 10 | — | ns |
| Data output defined time | t_{DRLD} | — | 25 | ns |
| Data output hold time | t_{DRHD} | 10 | — | ns |



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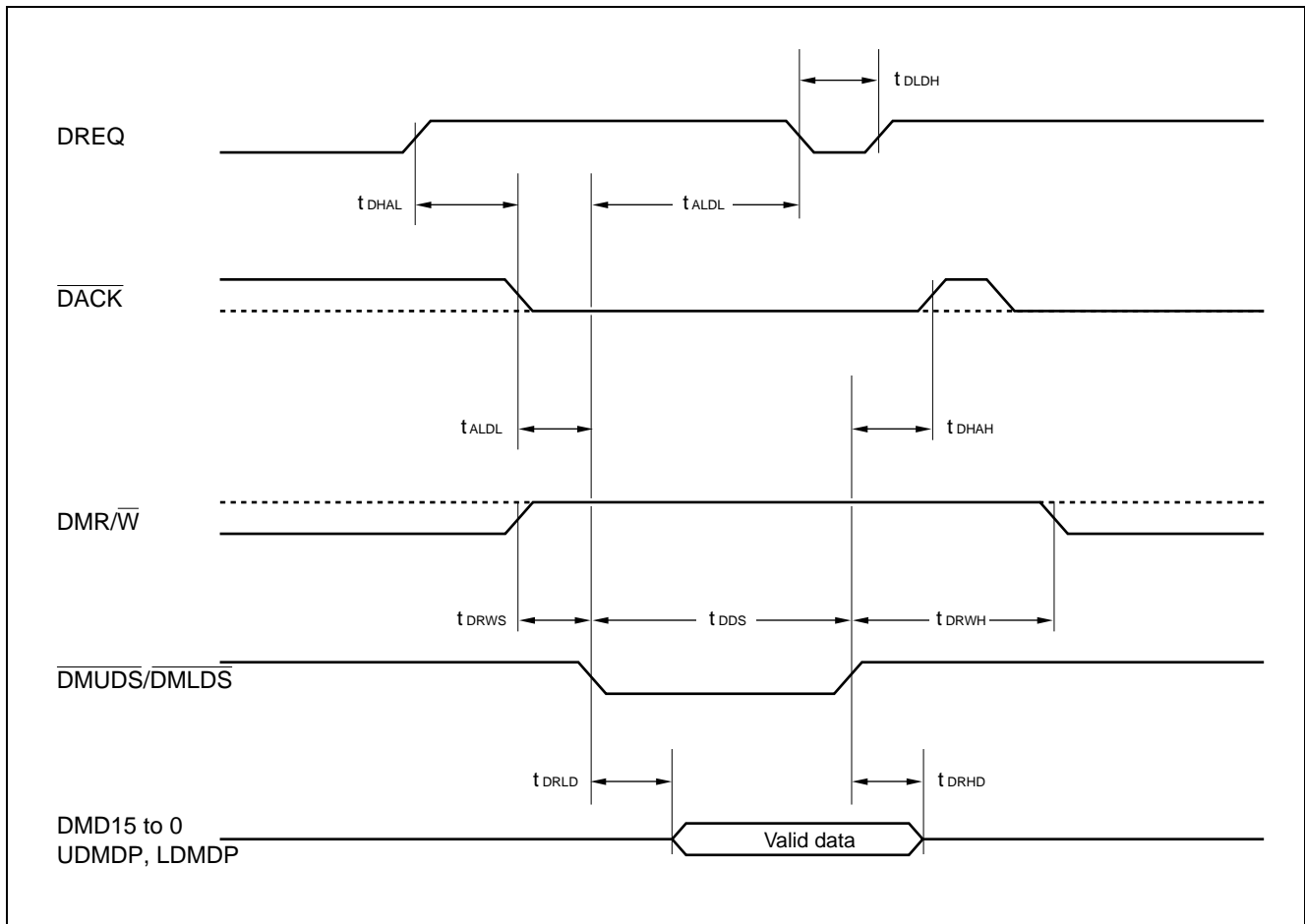
(4) Write timing (burst mode for 68 series)

| Parameter | Symbol | Value | | Unit |
|--|-------------------|-------|------|------|
| | | Min. | Max. | |
| DREQ set High → $\overline{\text{DACK}}$ set Low | t_{DHAL} | 0 | — | ns |
| $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low → DREQ set Low | t_{ALDL} | — | 25 | ns |
| DREQ set Low → DREQ set High | t_{DLDH} | 0 | — | ns |
| $\overline{\text{DACK}}$ set Low → $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low | t_{ALDL} | 5 | — | ns |
| $\text{R}/\overline{\text{W}}$ setup time | t_{DRWS} | 10 | — | ns |
| $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ "L" level pulse width | t_{DDS} | 25 | — | ns |
| $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set High → $\overline{\text{DACK}}$ set High | t_{DHAH} | 0 | — | ns |
| $\text{R}/\overline{\text{W}}$ hold time | t_{DRWH} | 10 | — | ns |
| Input data setup time | t_{DDWS} | 25 | — | ns |
| Input data hold time | t_{DDWH} | 5 | — | ns |



(5) Read timing (burst mode for 68 series)

| Parameter | Symbol | Value | | Unit |
|--|-------------------|-------|------|------|
| | | Min. | Max. | |
| DREQ set High → $\overline{\text{DACK}}$ set Low | t_{DHAL} | 0 | — | ns |
| $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low → DREQ set Low | t_{ALDL} | — | 25 | ns |
| DREQ set Low → DREQ set High | t_{LDLH} | 0 | — | ns |
| $\overline{\text{DACK}}$ set Low → $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low | t_{ALDL} | 5 | — | ns |
| $\text{R}/\overline{\text{W}}$ setup time | t_{DRWS} | 10 | — | ns |
| $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ "L" level pulse width | t_{DDS} | 25 | — | ns |
| $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set High → $\overline{\text{DACK}}$ set High | t_{DHAH} | 0 | — | ns |
| $\text{R}/\overline{\text{W}}$ hold time | t_{DRWH} | 10 | — | ns |
| Output data valid time | t_{DRLD} | — | 25 | ns |
| Output data hold time | t_{DRHD} | 10 | — | ns |



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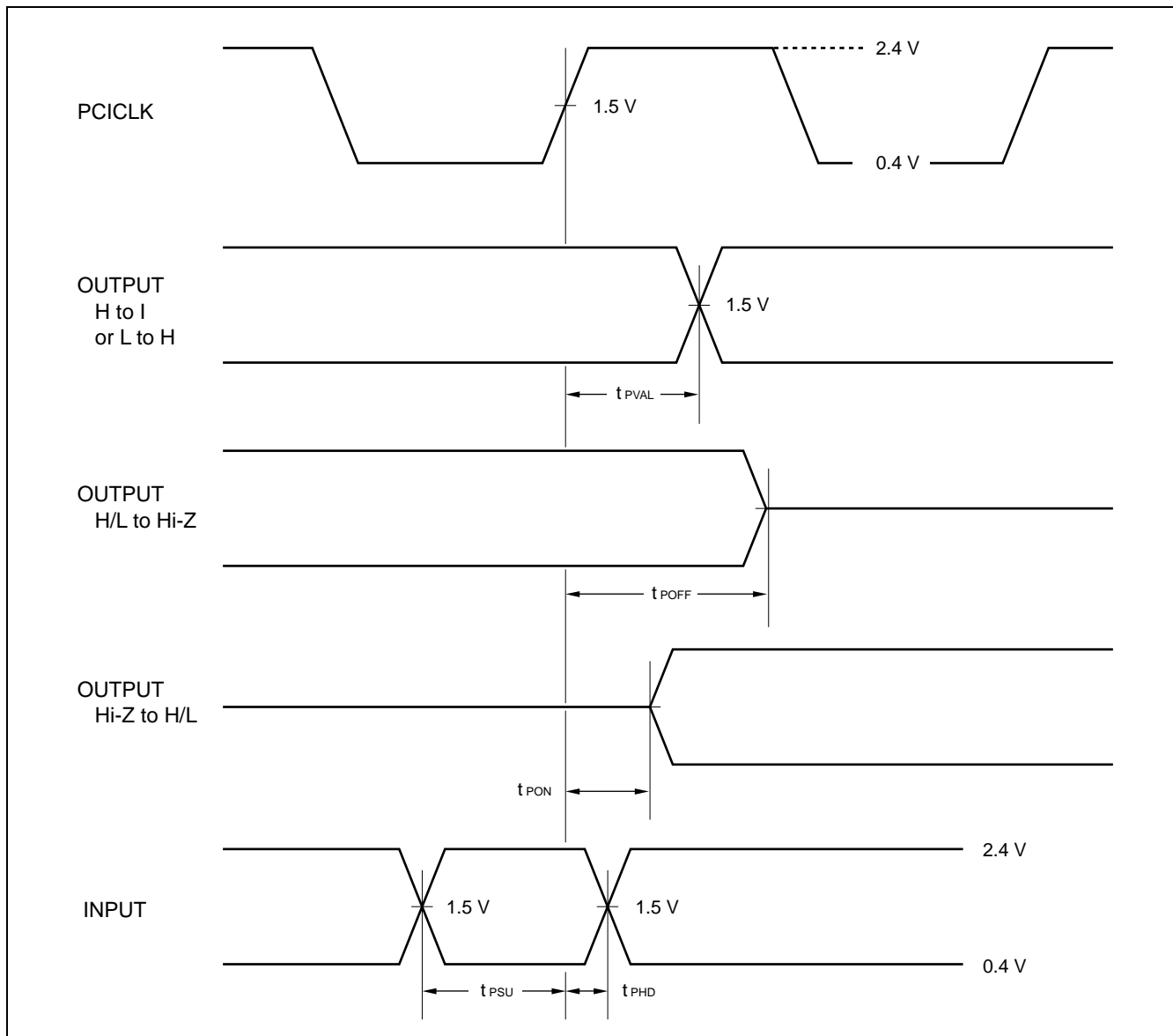
7. PCI Interface

(1) PCI interface signal timing

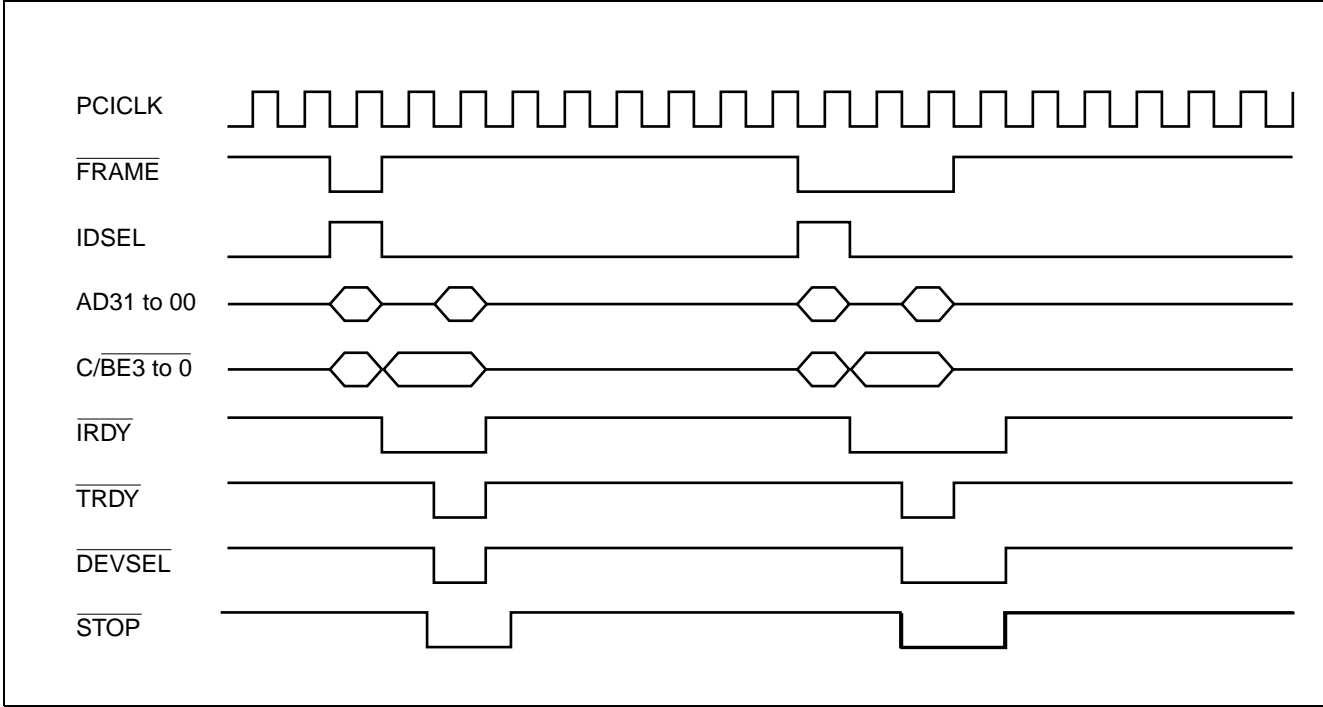
| Parameter | Symbol | Value | | Unit |
|--------------------------|--------|--------------------|---------------------|------|
| | | Min. | Max. | |
| Output signal valid time | tPVAL | 2 | 11/12* ¹ | ns |
| Output disable time | tPOFF | — | 28 | ns |
| Output enable time | tPON | 2 | — | ns |
| Input setup time | tPSU | 7/10* ² | — | ns |
| Input hold time | tPHD | 0 | — | ns |

*1: Applicable to $\overline{\text{PREQ}}$ pin

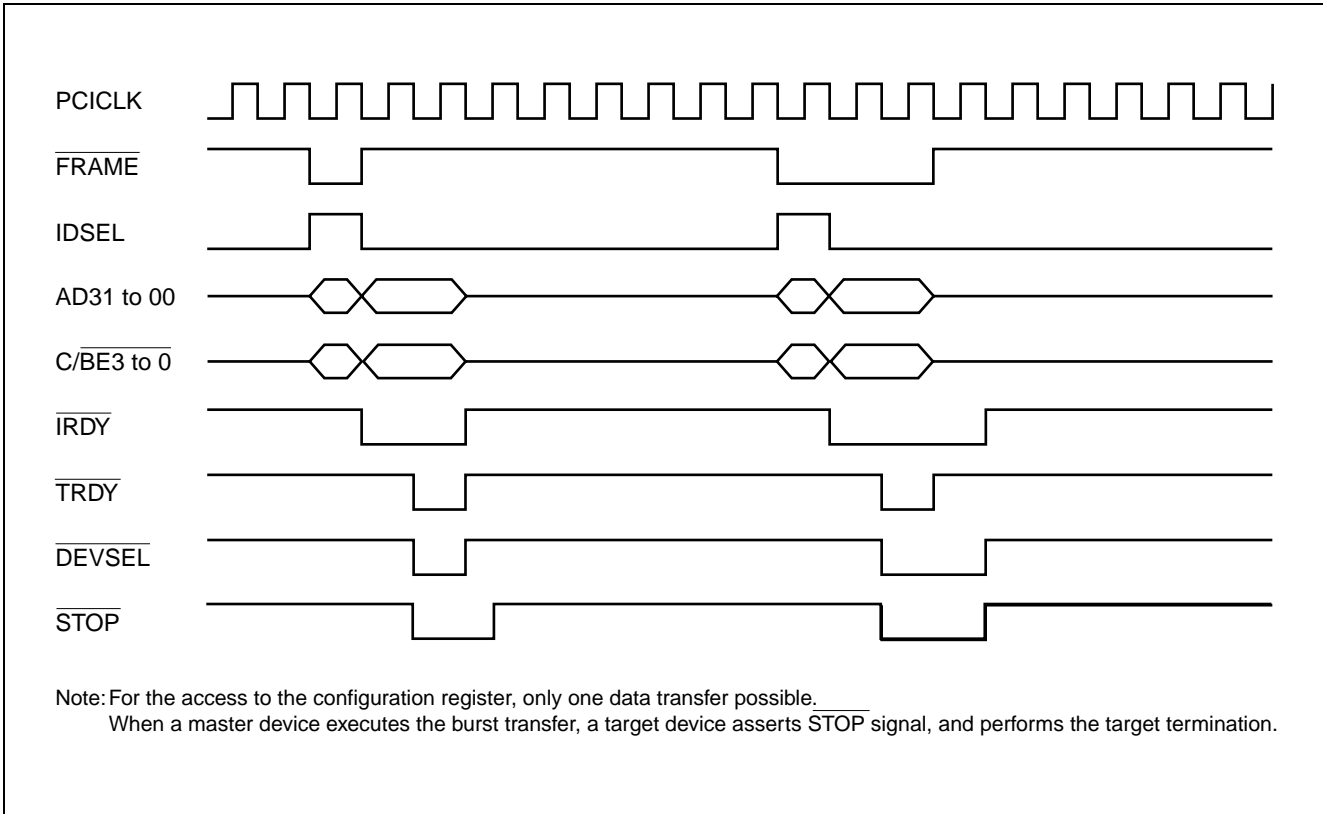
*2: Applicable to $\overline{\text{GNT}}$ pin



(2) Configuration register read timing



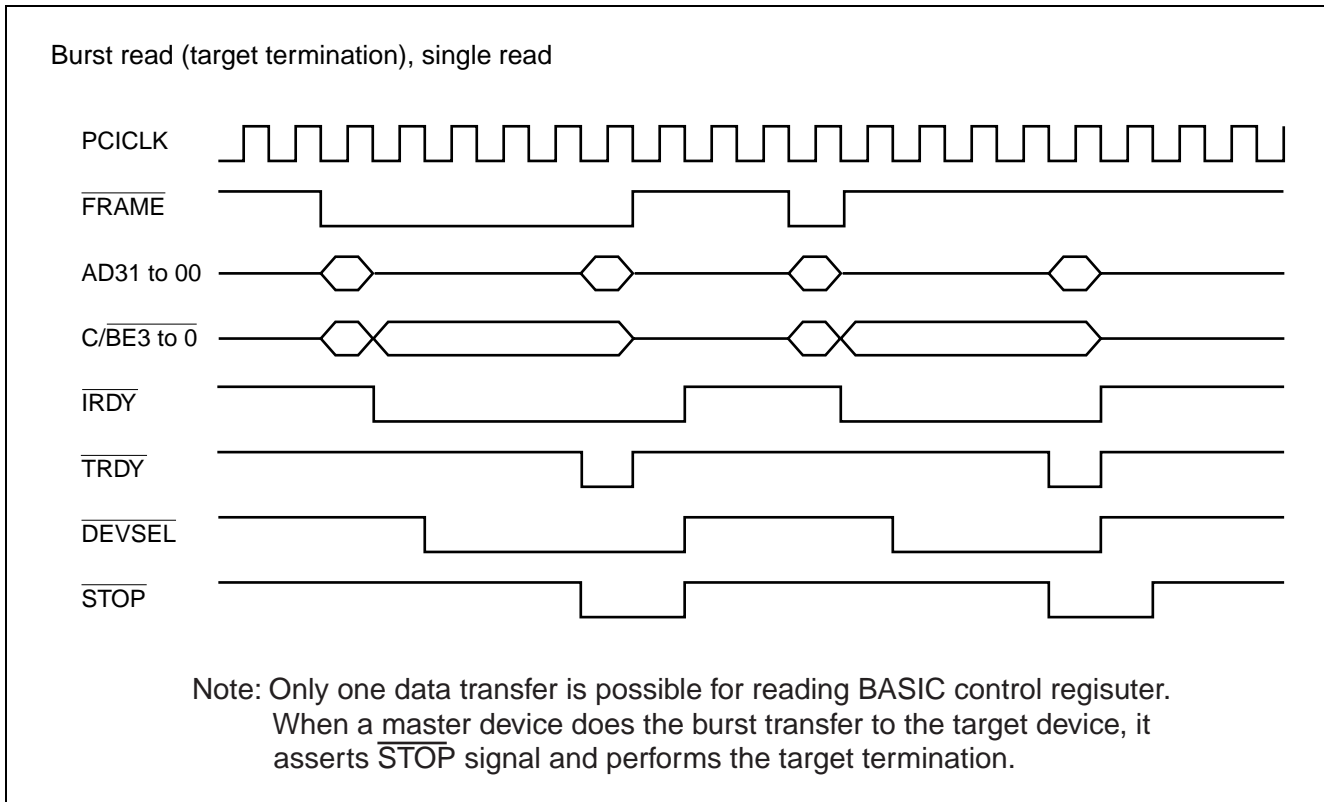
(3) Configuration register write timing



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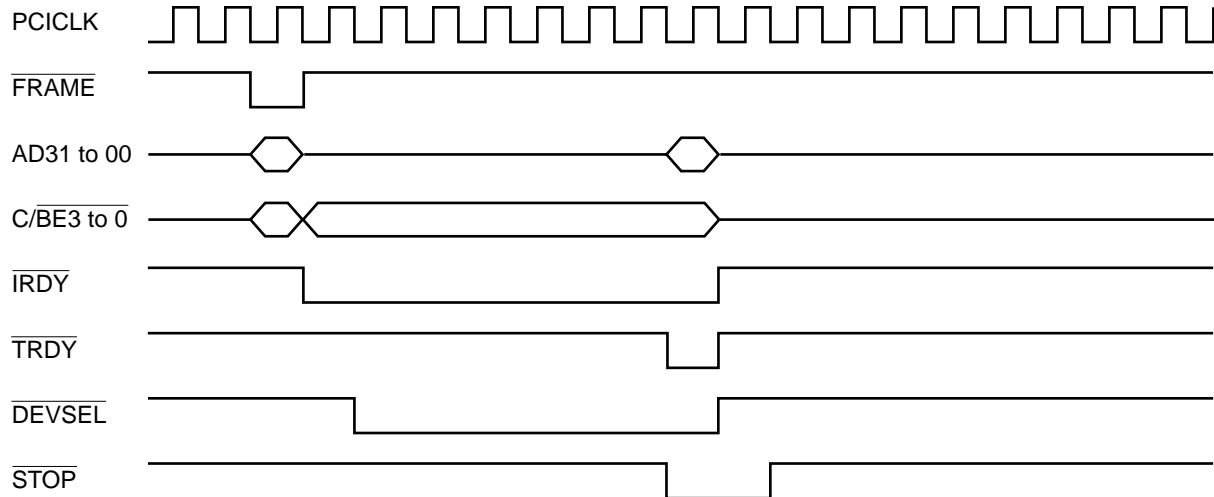
(4) BASIC control register read timing (target mode)

- Byte or word access

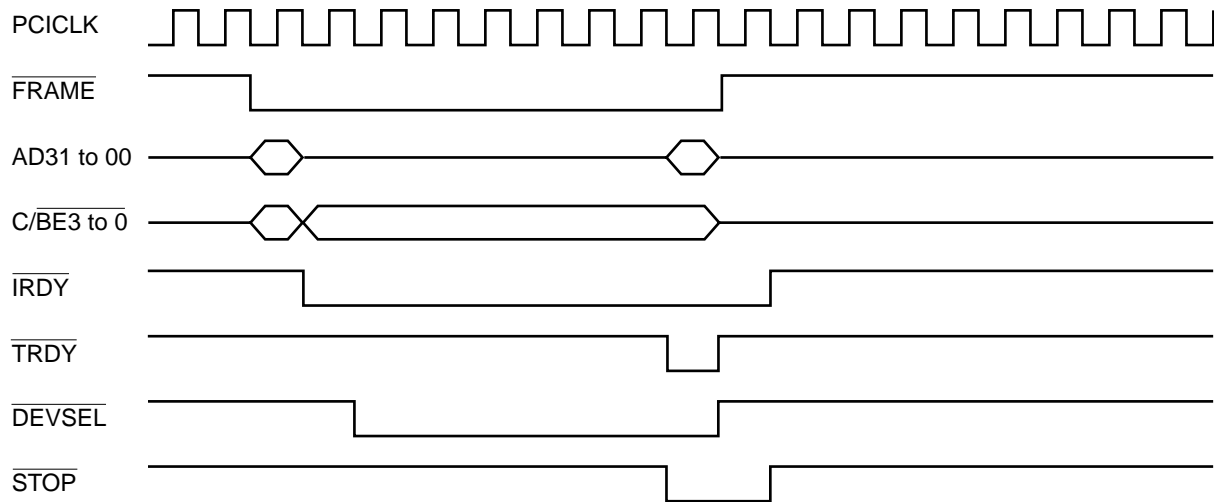


• Long-word access

Single read



Burst read (target termination)

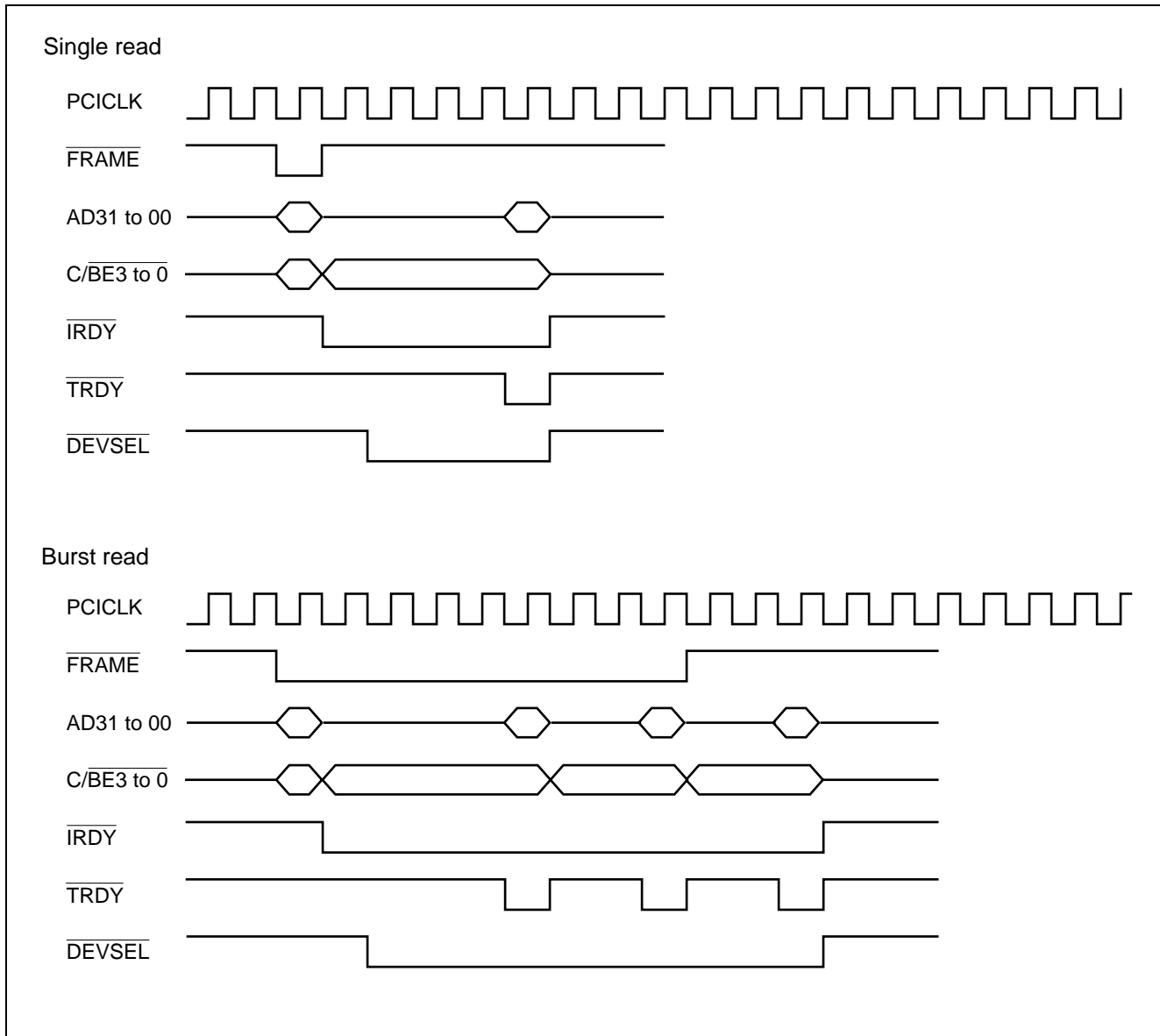


Note: For the read operation of BASIC control registers, only one data transfer possible.
 When a master device executes the burst transfer, a target device asserts STOP signal and performs the target termination.

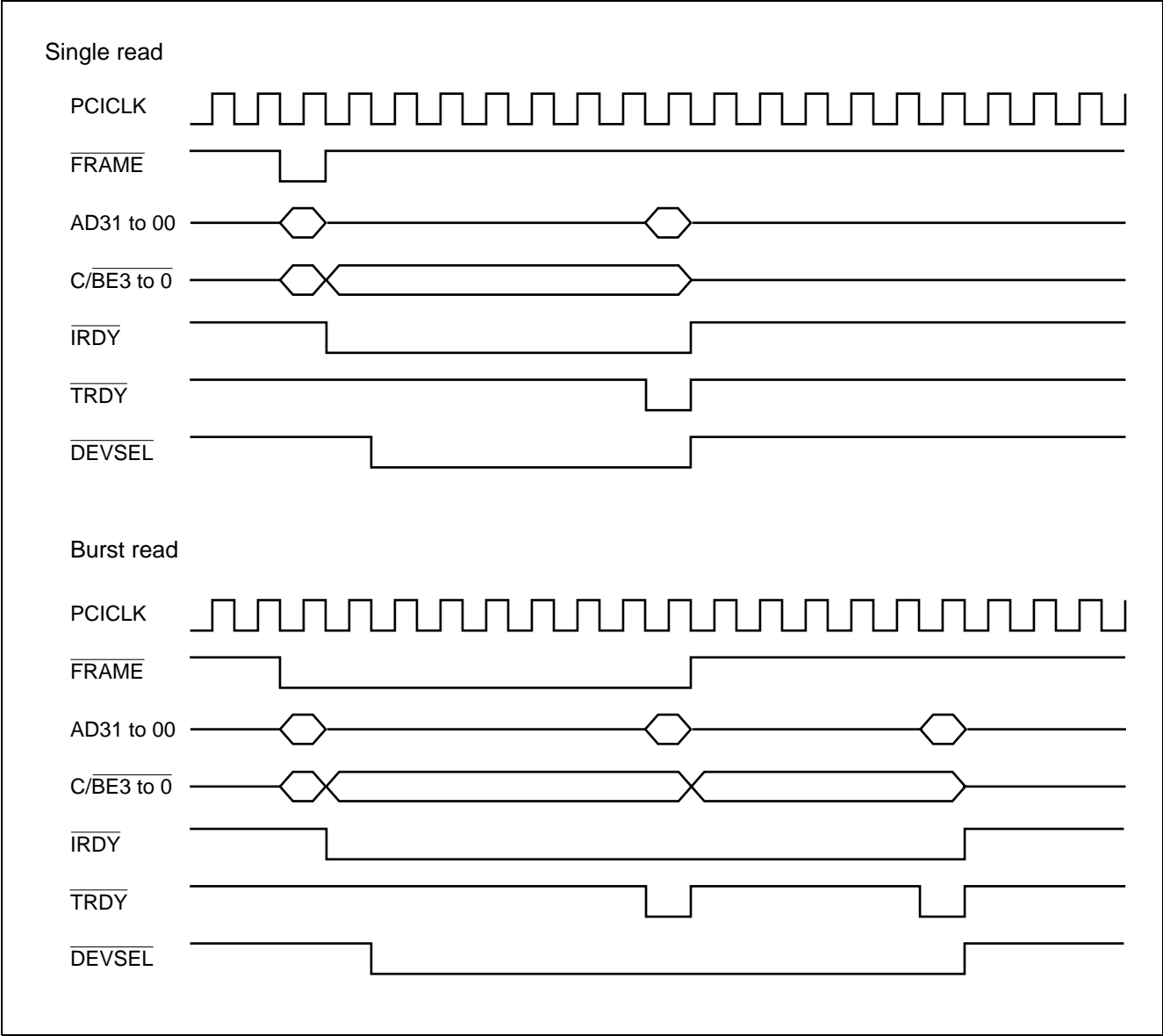
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(5) Target mode – I/O, memory read timing (except BASIC control registers)

- Byte, word access



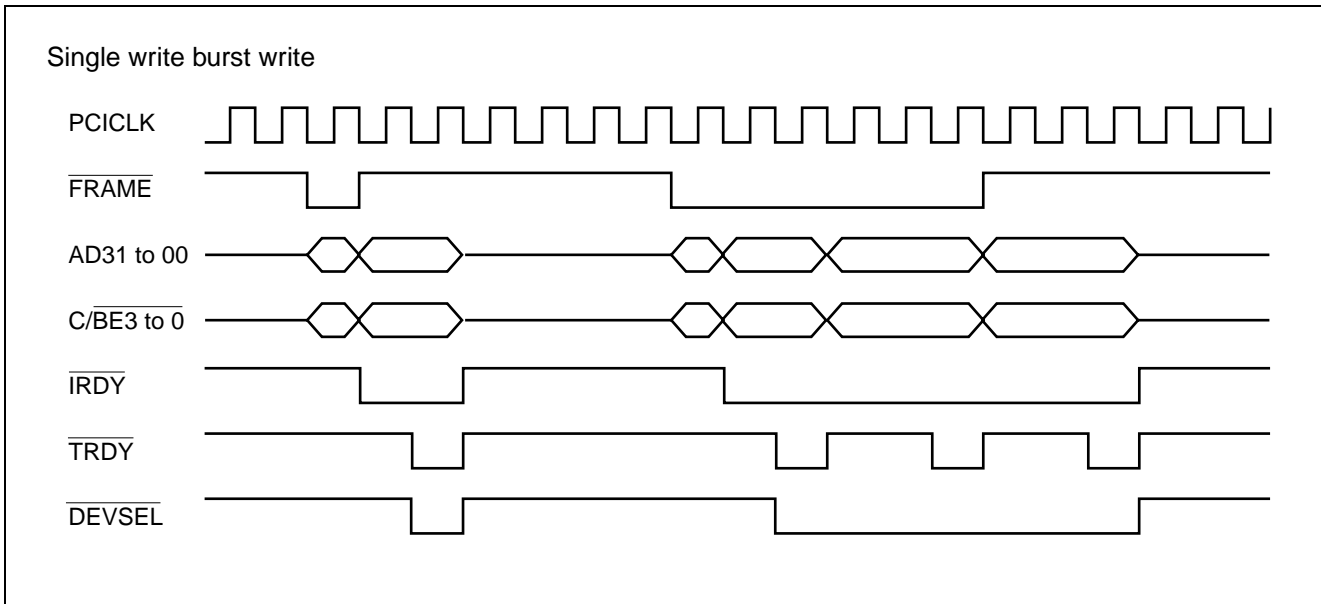
• Long-word access



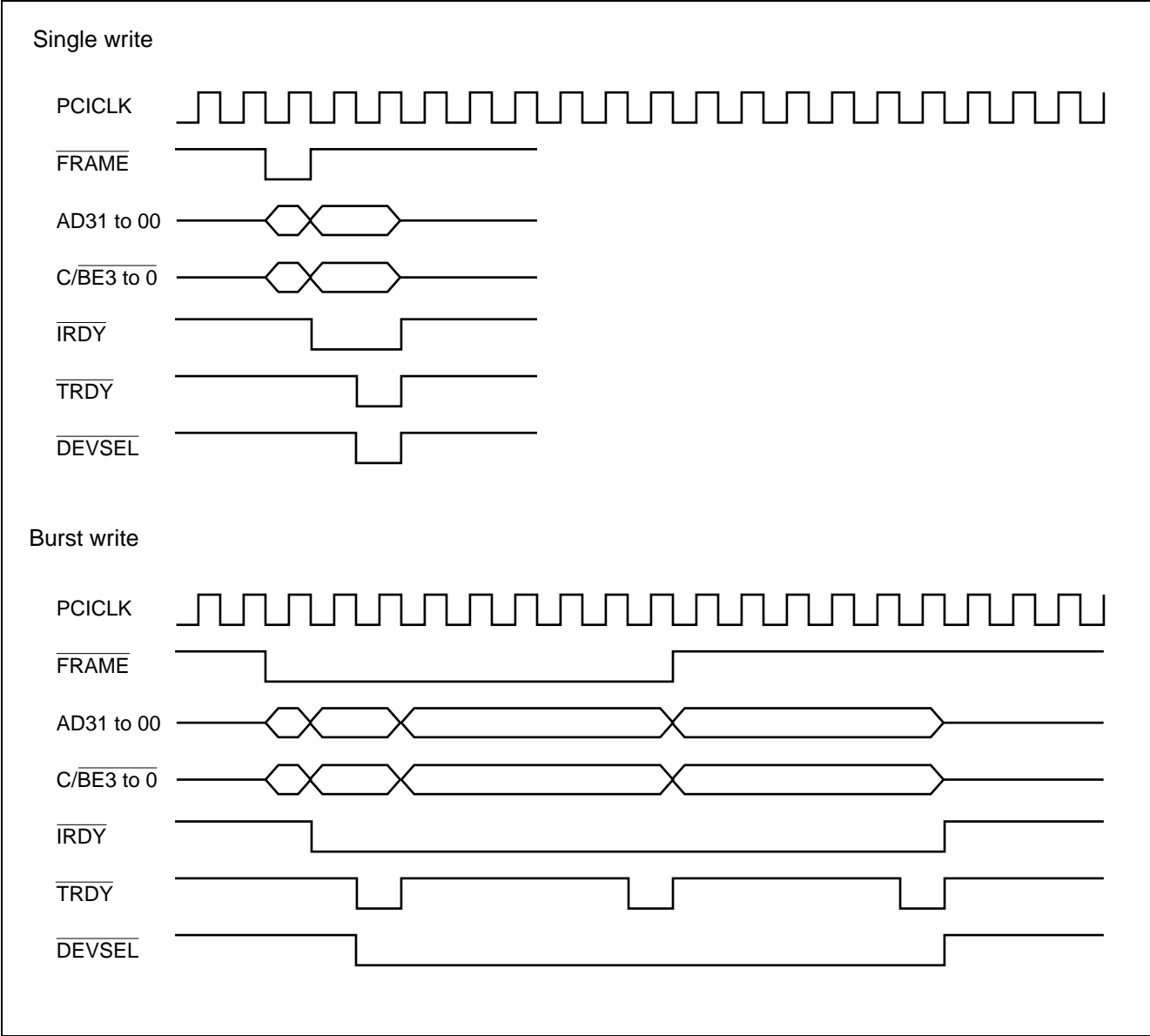
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(6) Target Mode – I/O, memory write timing

- Byte, word access



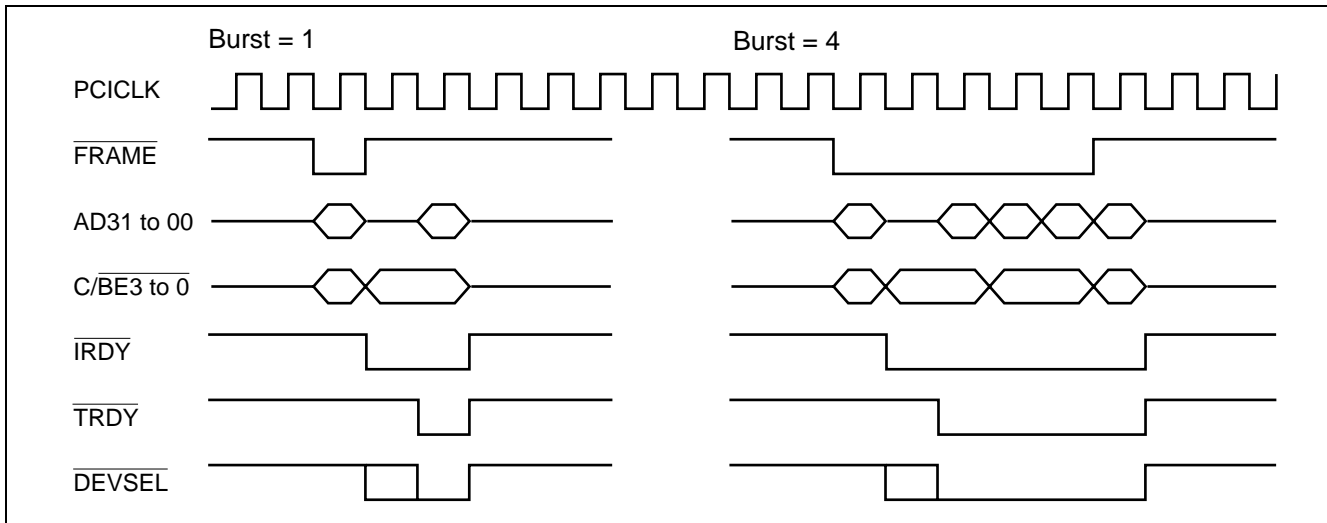
• Long-word access



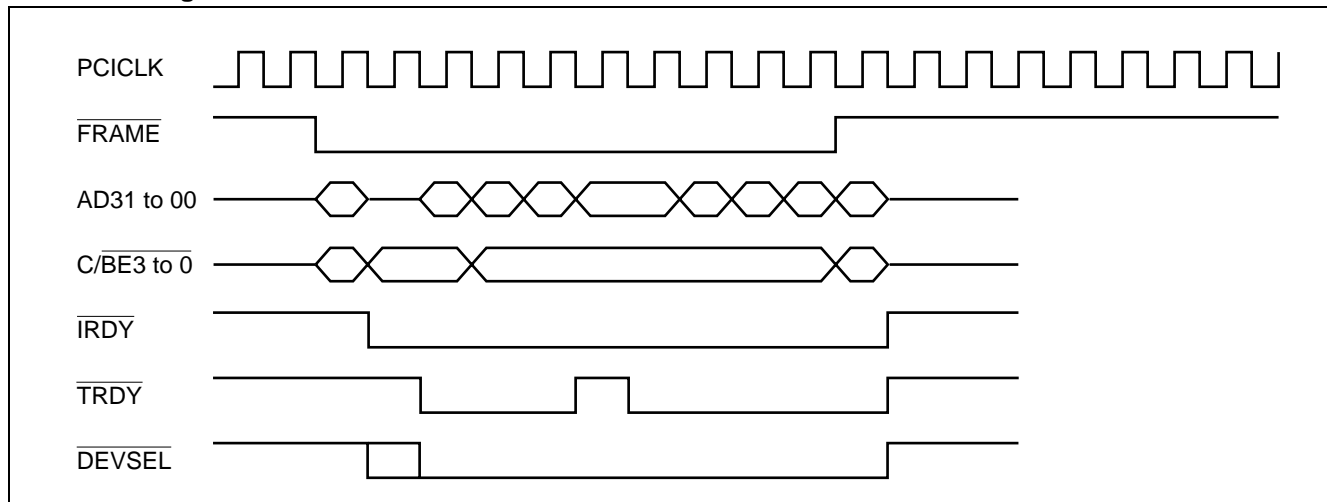
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(7) Data read timing (master mode)

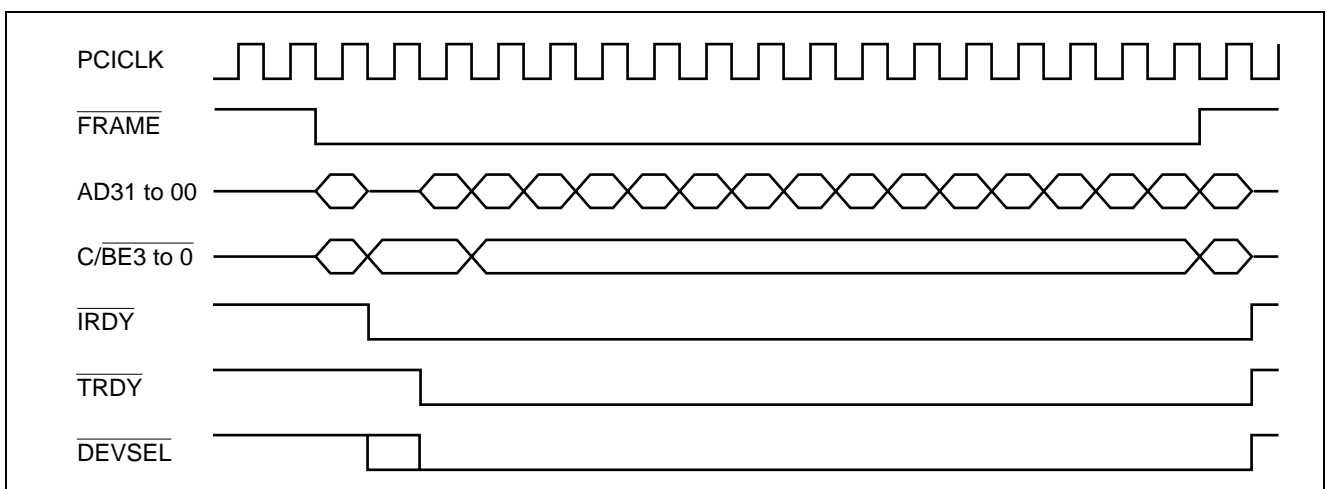
• Burst length = 1 and 4



• Burst length = 8

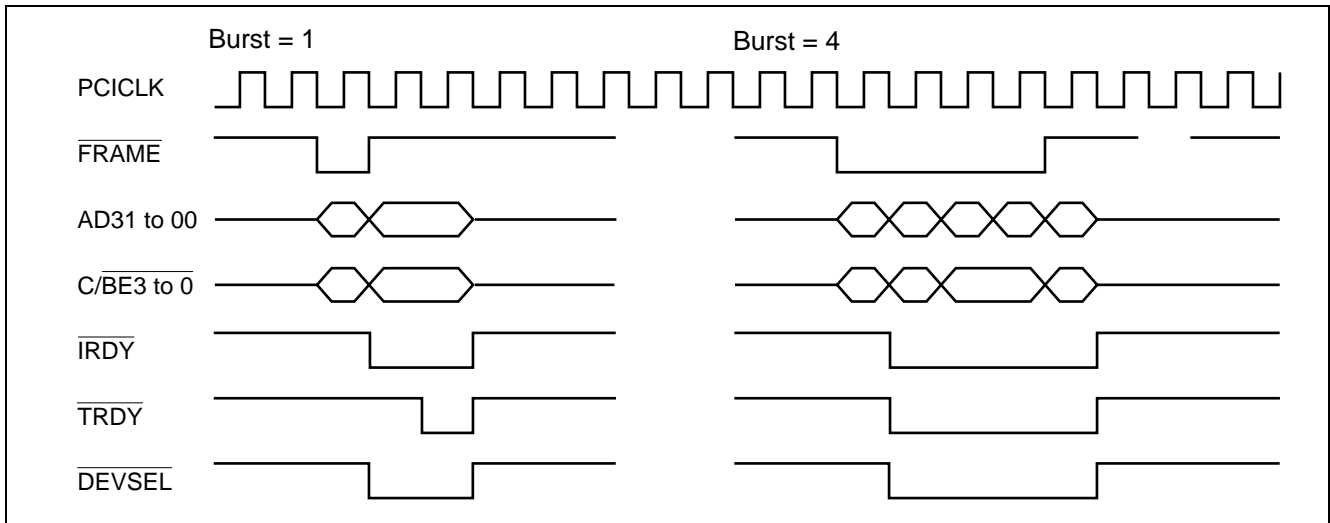


• Burst length = 16

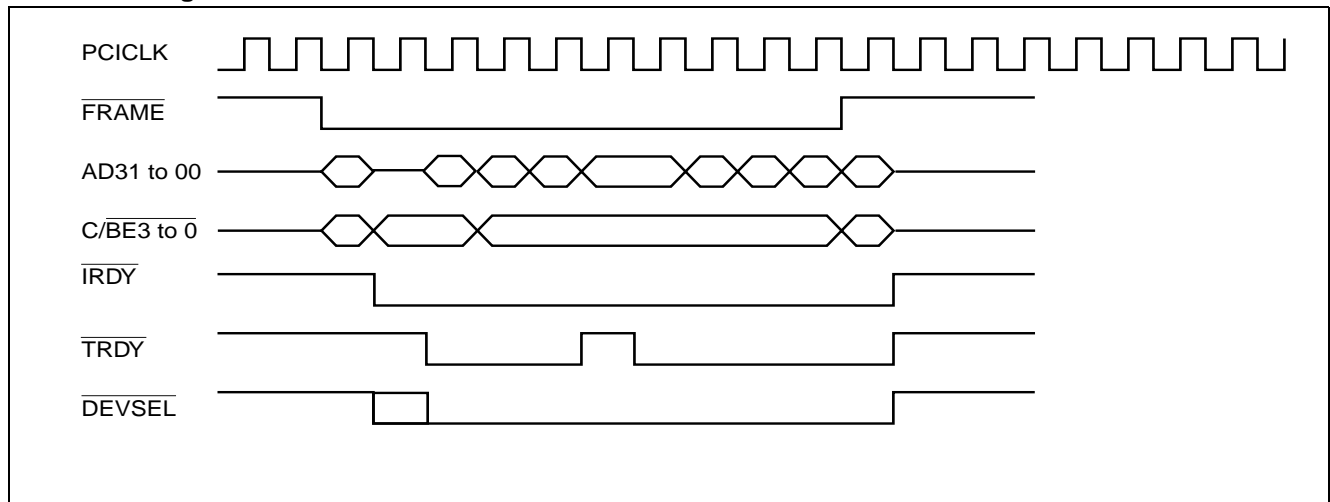


(8) Data write timing (master mode)

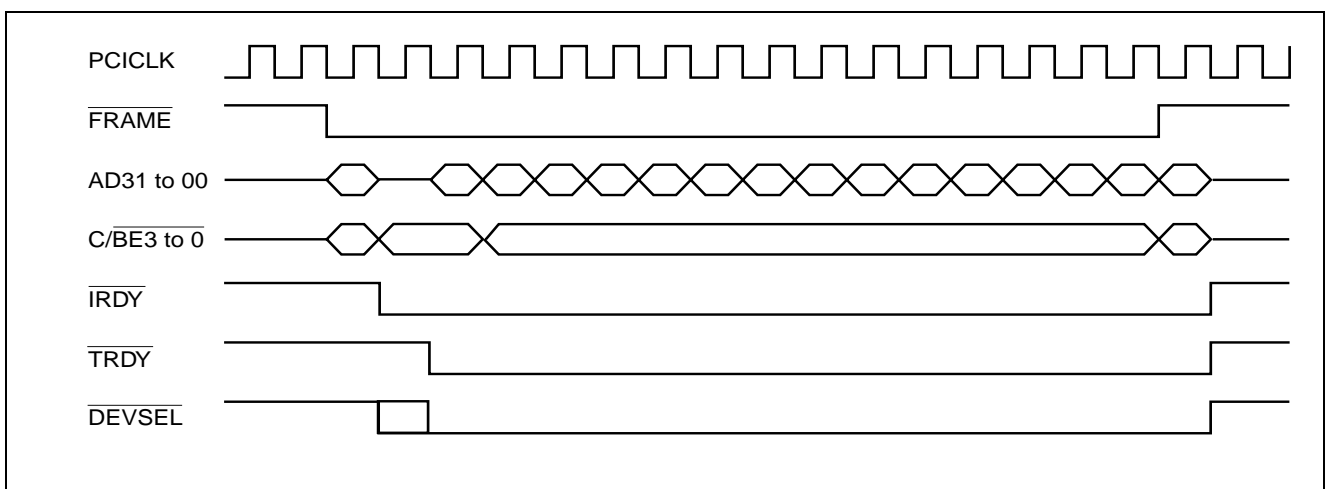
• Burst length = 1 and 4



• Burst length = 8



• Burst length = 16



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8. SCSI Interface

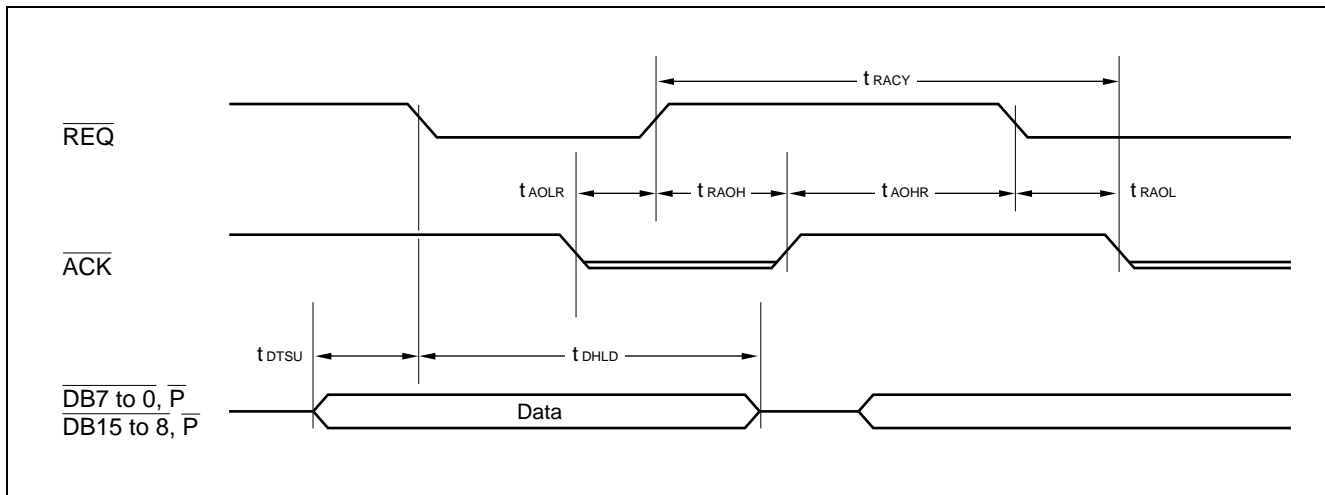
(1) Initiator asynchronous input timing (target → initiator)

| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------|-------------------------|------|
| | | Min. | Max. | |
| $\overline{\text{ACK}}$ set Low → $\overline{\text{REQ}}$ set High | t_{AOLR} | 0 | — | ns |
| $\overline{\text{REQ}}$ set High → $\overline{\text{ACK}}$ set High | t_{RAOH} | — | 60 | ns |
| $\overline{\text{ACK}}$ set High → $\overline{\text{REQ}}$ set Low | t_{AOHR} | 10 | — | ns |
| Data bus valid → $\overline{\text{REQ}}$ set Low | t_{DTSU} | 10 | — | ns |
| $\overline{\text{REQ}}$ set Low → data bus hold time | t_{DHLD} | 20 | — | ns |
| $\overline{\text{REQ}}$ set Low → $\overline{\text{ACK}}$ set Low | t_{RAOL} | — | 40 | ns |
| $\overline{\text{REQ}}$ set High → $\overline{\text{ACK}}$ set Low* | t_{RACY} | — | $3 t_{\text{CLF}} + 40$ | ns |

* : t_{RACY} ($\overline{\text{REQ}}$ set High → $\overline{\text{ACK}}$ set Low) is defined as either longer time of ($t_{\text{RAOH}} + t_{\text{AOHR}} + t_{\text{RAOL}}$) or t_{RACY} itself

Note: Time requirements in this section do not apply in the following cases;

- When data register FULL in data phase
- When last byte transferred

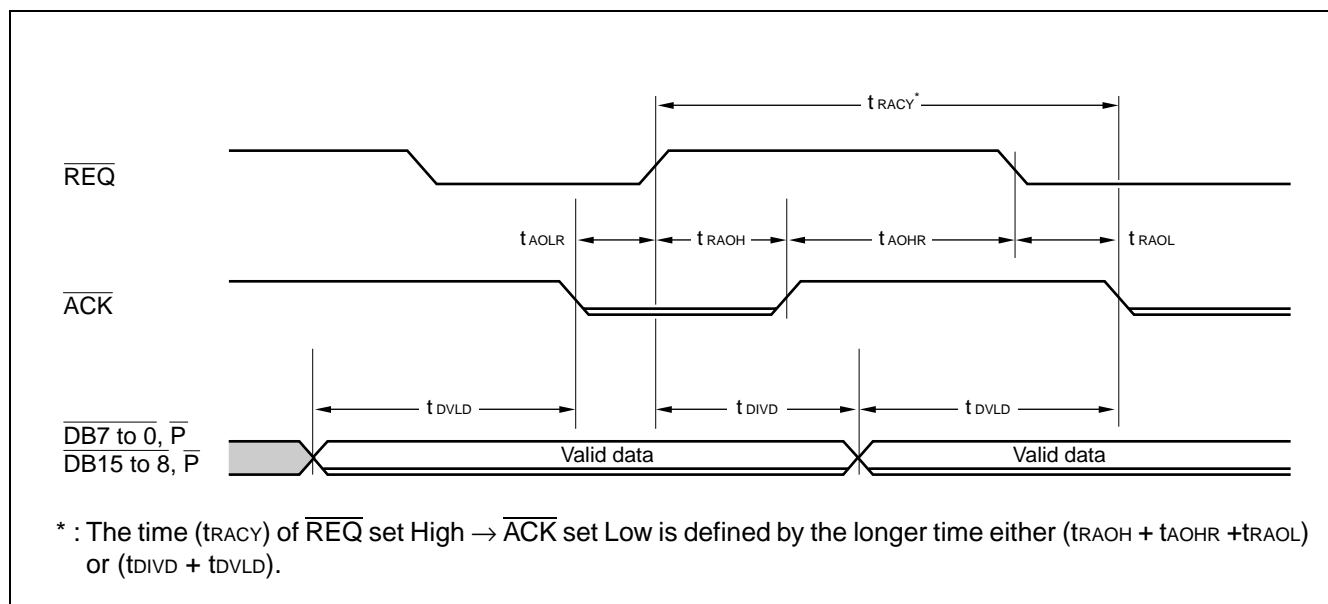


(2) Initiator asynchronous output timing (initiator → target)

| Parameter | Symbol | Value | | Unit |
|---|--------|------------------------|------|------|
| | | Min. | Max. | |
| \overline{ACK} set Low → \overline{REQ} set High | tAOLR | 0 | — | ns |
| \overline{REQ} set High → \overline{ACK} set High | tRAOH | — | 60 | ns |
| \overline{ACK} set High → \overline{REQ} set Low | tAOHR | 10 | — | ns |
| Data bus output defined → \overline{ACK} set Low* | tDVLD | $S \cdot t_{CLF} - 10$ | — | ns |
| \overline{REQ} set High → data bus hold time | tDIVD | 2 tCLF | — | ns |
| \overline{REQ} set Low → \overline{ACK} set Low | tRAOL | — | 40 | ns |

* : The value of S varies with the setting condition of the asynchronous setup time register (address 17h).

Note: This output timing regulations are not applicable when the data register is EMPTY in the data phase.

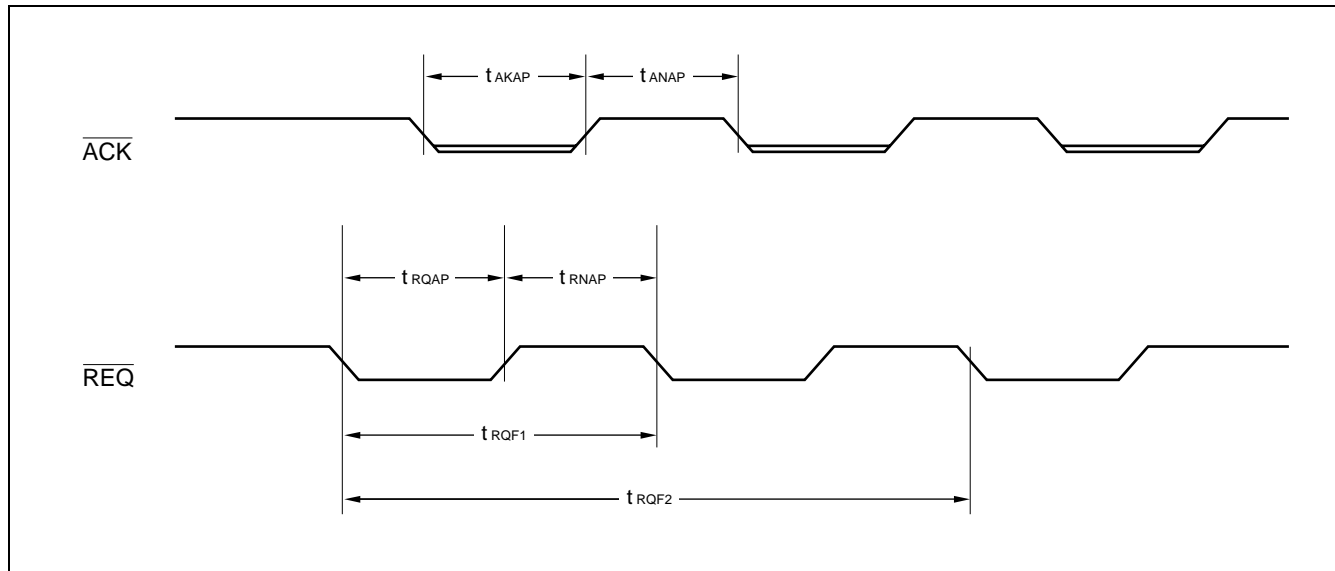


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(3) Initiator synchronous transfer $\overline{\text{REQ}}/\overline{\text{ACK}}$ timing

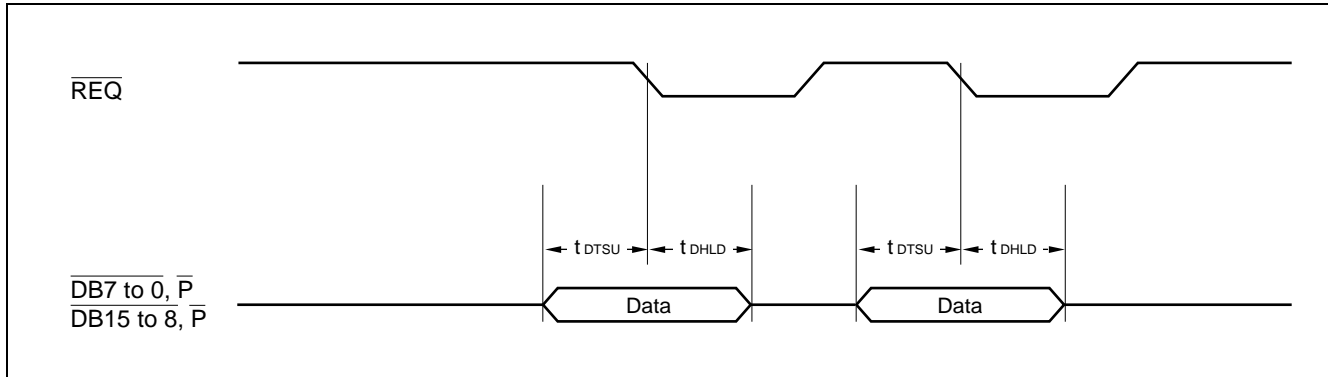
| Parameter | Symbol | Value | | Unit |
|--|-------------------|------------------------------|------|------|
| | | Min. | Max. | |
| $\overline{\text{ACK}}$ Assertion Period* | t_{AKAP} | $A \cdot t_{\text{CLF}} - 4$ | — | ns |
| $\overline{\text{ACK}}$ Negation Period* | t_{ANAP} | $N \cdot t_{\text{CLF}} - 6$ | — | ns |
| $\overline{\text{REQ}}$ Assertion Period | t_{RQAP} | 20 | — | ns |
| $\overline{\text{REQ}}$ Negation Period | t_{RNAP} | 20 | — | ns |
| $\overline{\text{REQ}}$ input cycle time (1) | t_{RQF1} | 1 tCLF | — | ns |
| $\overline{\text{REQ}}$ input cycle time (2) | t_{RQF2} | 3 tCLF | — | ns |

* : The values of A and N vary with the setting condition of the transfer period register (address 0Ch).



(4) Initiator synchronous transfer input timing (target → initiator)

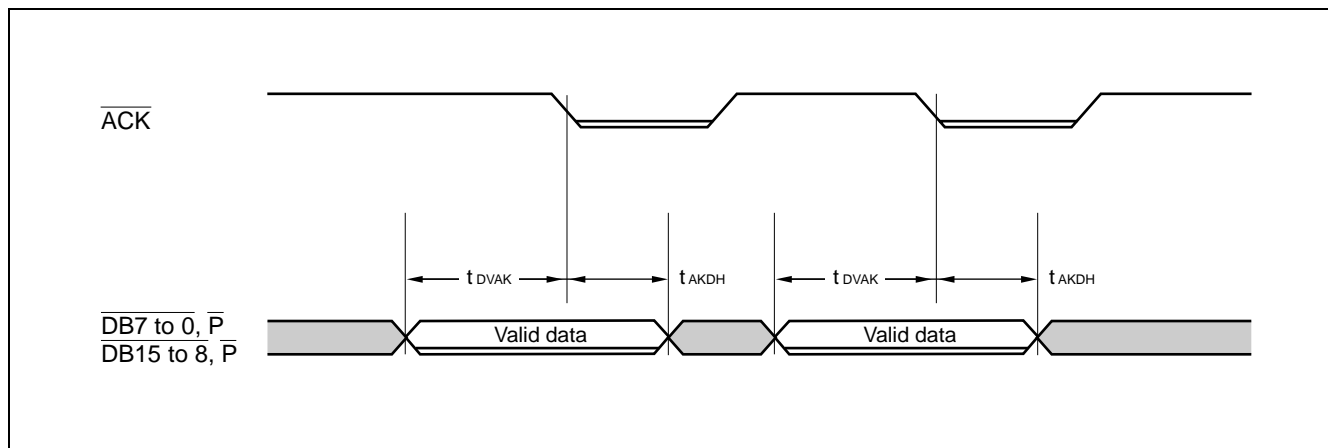
| Parameter | Symbol | Value | | Unit |
|--|--------|-------|------|------|
| | | Min. | Max. | |
| Data bus defined → $\overline{\text{REQ}}$ set Low | tDTSU | 5 | — | ns |
| $\overline{\text{REQ}}$ set Low → data bus hold time | tDHLD | 15 | — | ns |



(5) Initiator synchronous transfer output timing (initiator → target)

| Parameter | Symbol | Value | | Unit |
|---|--------|-------------------------------|------|------|
| | | Min. | Max. | |
| Data bus defined → $\overline{\text{ACK}}$ set Low* | tDVAK | $N \cdot t_{\text{CLF}} - 10$ | — | ns |
| $\overline{\text{ACK}}$ set Low → data bus hold time* | tAKDH | $A \cdot t_{\text{CLF}} - 5$ | — | ns |

* : The values of A and N vary with the setting condition of the transfer period register (address 0Ch).



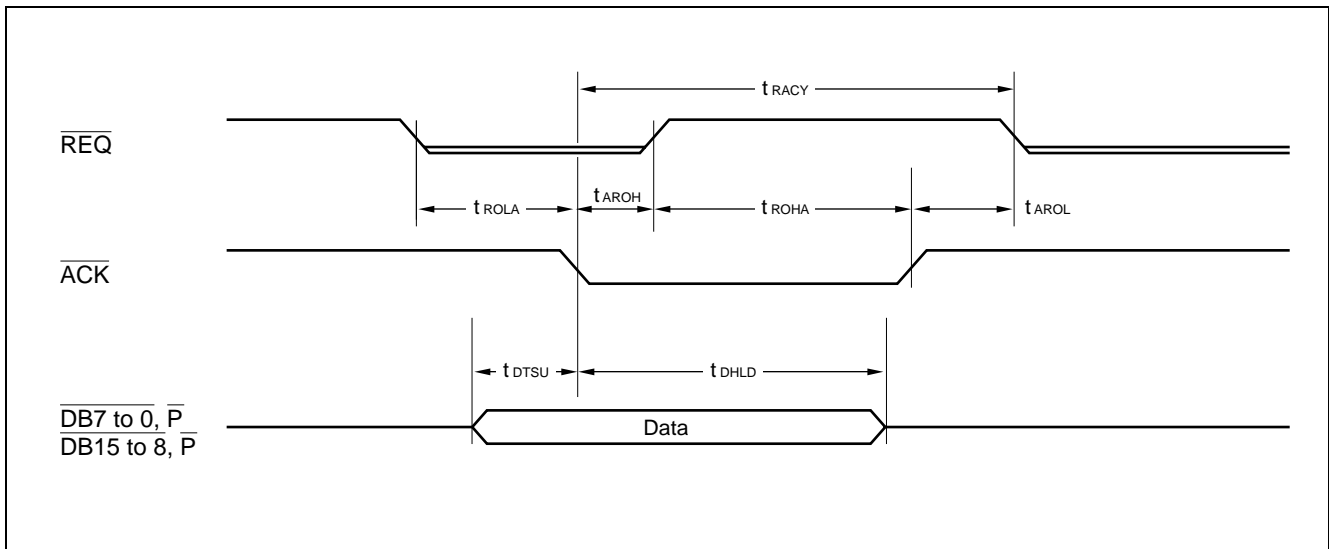
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(6) Target asynchronous input timing (initiator → target)

| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------|-------------------------|------|
| | | Min. | Max. | |
| $\overline{\text{REQ}}$ set Low → $\overline{\text{ACK}}$ set Low | t_{ROLA} | 0 | — | ns |
| $\overline{\text{ACK}}$ set Low → $\overline{\text{REQ}}$ set High | t_{AROH} | — | 60 | ns |
| $\overline{\text{REQ}}$ set High → $\overline{\text{ACK}}$ set High | t_{ROHA} | 0 | — | ns |
| Data bus defined → $\overline{\text{ACK}}$ set Low | t_{DTSU} | 10 | — | ns |
| $\overline{\text{ACK}}$ set Low → data bus hold time | t_{DHLD} | 20 | — | ns |
| $\overline{\text{ACK}}$ set High → $\overline{\text{REQ}}$ set Low | t_{AROL} | — | 40 | ns |
| $\overline{\text{ACK}}$ set Low → $\overline{\text{REQ}}$ set Low* | t_{RACY} | — | $3 t_{\text{CLF}} + 40$ | ns |

* : t_{RACY} ($\overline{\text{ACK}}$ set Low → $\overline{\text{REQ}}$ set Low) is defined as either longer time of ($t_{\text{AROH}} + t_{\text{ROHA}} + t_{\text{AROL}}$) or t_{RACY} itself

Note: The input timing regulations are not applicable when the data register is FULL in the data phase.

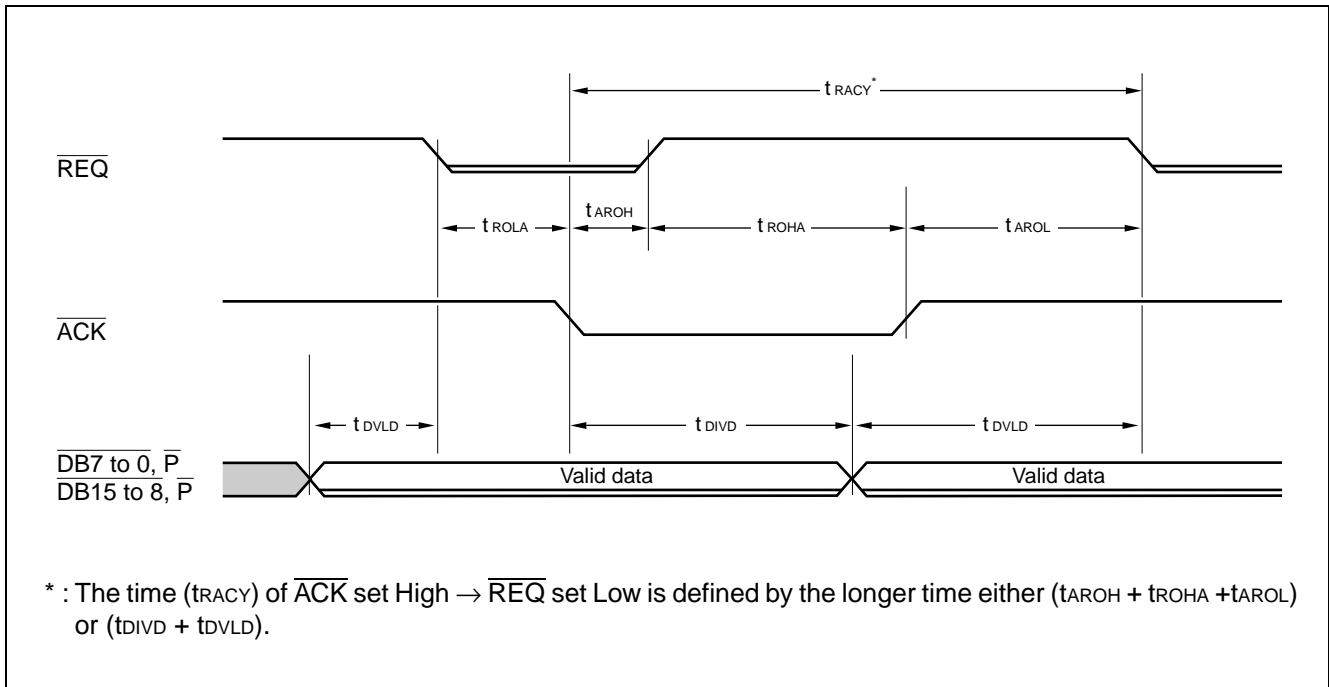


(7) Target asynchronous input timing (target → initiator)

| Parameter | Symbol | Value | | Unit |
|---|-------------------|-------------------------------|------|------|
| | | Min. | Max. | |
| $\overline{\text{REQ}}$ set Low → $\overline{\text{ACK}}$ set Low | t_{ROLA} | 0 | — | ns |
| $\overline{\text{ACK}}$ set Low → $\overline{\text{REQ}}$ set High | t_{AROH} | — | 60 | ns |
| $\overline{\text{REQ}}$ set High → $\overline{\text{ACK}}$ set High | t_{ROHA} | 0 | — | ns |
| Data bus defined → $\overline{\text{REQ}}$ set Low* | t_{DVLD} | $S \cdot t_{\text{CLF}} - 10$ | — | ns |
| $\overline{\text{ACK}}$ set Low → data bus hold time | t_{DIVD} | $2 t_{\text{CLF}}$ | — | ns |
| $\overline{\text{ACK}}$ set High → $\overline{\text{REQ}}$ set Low | t_{AROL} | — | 40 | ns |

* : The value of S varies with the setting condition of the asynchronous setup time register (address 17h).

Note: The output timing regulations are not applicable when the data register is EMPTY in the data phase.

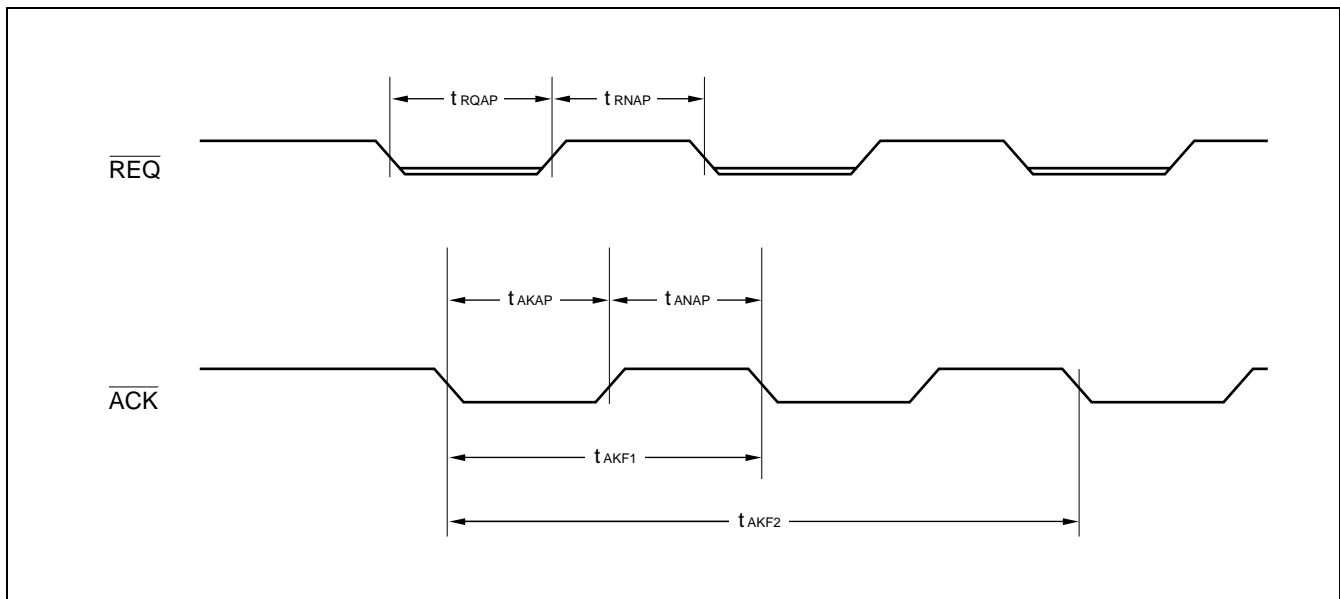


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(8) Target synchronous transfer $\overline{\text{REQ}}/\overline{\text{ACK}}$ timing

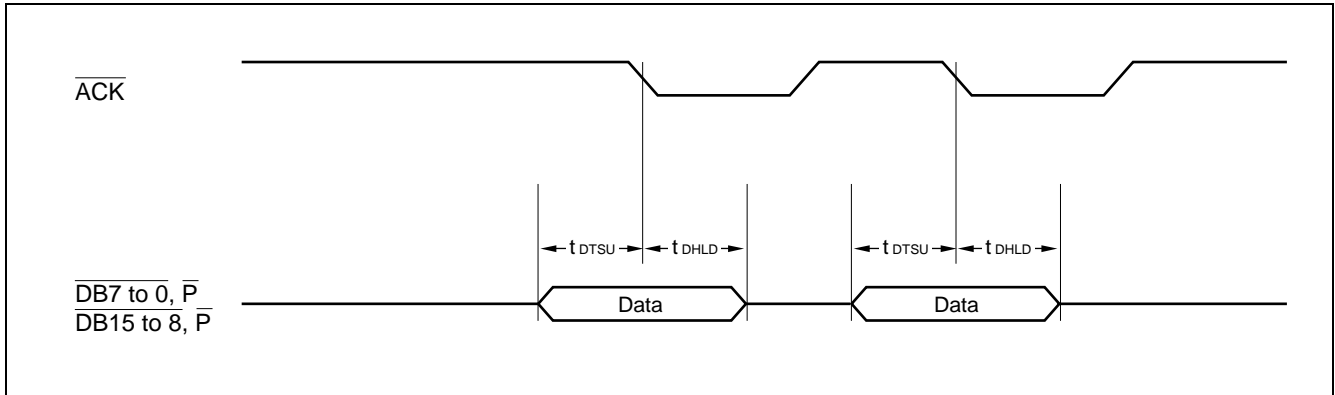
| Parameter | Symbol | Value | | Unit |
|--|-------------------|------------------------------|------|------|
| | | Min. | Max. | |
| $\overline{\text{REQ}}$ Assertion Period* | t _{RQAP} | $A \cdot t_{\text{CLF}} - 4$ | — | ns |
| $\overline{\text{REQ}}$ Negation Period* | t _{RNAP} | $N \cdot t_{\text{CLF}} - 6$ | — | ns |
| $\overline{\text{ACK}}$ Assertion Period | t _{AKAP} | 20 | — | ns |
| $\overline{\text{ACK}}$ Negation Period | t _{ANAP} | 20 | — | ns |
| $\overline{\text{ACK}}$ input cycle time (1) | t _{AKF1} | 1 t _{CLF} | — | ns |
| $\overline{\text{ACK}}$ input cycle time (2) | t _{AKF2} | 3 t _{CLF} | — | ns |

* : The values of A and N vary with the setting condition of the transfer period register (address 0Ch).



(9) Target synchronous transfer input timing (initiator → target)

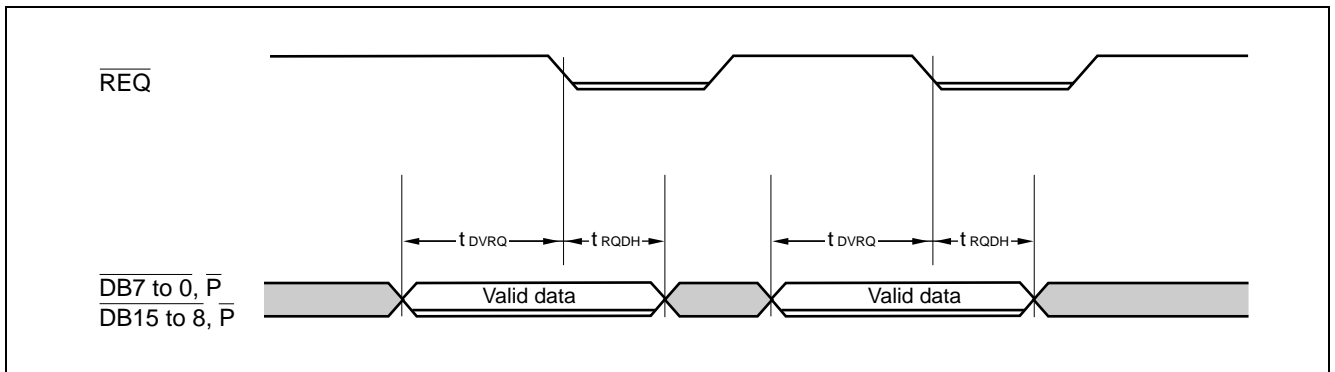
| Parameter | Symbol | Value | | Unit |
|--|--------|-------|------|------|
| | | Min. | Max. | |
| Data bus defined → $\overline{\text{ACK}}$ set Low | tDTSU | 5 | — | ns |
| $\overline{\text{ACK}}$ set Low → data bus hold time | tDHLd | 15 | — | ns |



(10) Target synchronous transfer output timing (target → initiator)

| Parameter | Symbol | Value | | Unit |
|---|--------|-------------------------------|------|------|
| | | Min. | Max. | |
| Data bus defined → $\overline{\text{REQ}}$ set Low* | tDVRQ | $N \cdot t_{\text{CLF}} - 10$ | — | ns |
| $\overline{\text{REQ}}$ set Low → data bus hold time* | tRQDH | $A \cdot t_{\text{CLF}} - 5$ | — | ns |

* : The values of A and N vary with the setting condition of the transfer period register (address 0Ch).



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(11) A, N, and S values in SCSI interface timing specifications

- Set value for transfer period register and A, N values

| Transfer period register | | | | | A | N | Transfer period register | | | | | A | N |
|--------------------------|---|---|---|---|-------------|-------------|--------------------------|---|---|---|---|----|----|
| 4 | 3 | 2 | 1 | 0 | | | 4 | 3 | 2 | 1 | 0 | | |
| 0 | 0 | 0 | 0 | 1 | (inhibited) | (inhibited) | 1 | 0 | 0 | 0 | 1 | 9 | 8 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 9 | 9 |
| 0 | 0 | 0 | 1 | 1 | 2 | 1 | 1 | 0 | 0 | 1 | 1 | 10 | 9 |
| 0 | 0 | 1 | 0 | 0 | 2 | 2 | 1 | 0 | 1 | 0 | 0 | 10 | 10 |
| 0 | 0 | 1 | 0 | 1 | 3 | 2 | 1 | 0 | 1 | 0 | 1 | 11 | 10 |
| 0 | 0 | 1 | 1 | 0 | 3 | 3 | 1 | 0 | 1 | 1 | 0 | 11 | 11 |
| 0 | 0 | 1 | 1 | 1 | 4 | 3 | 1 | 0 | 1 | 1 | 1 | 12 | 11 |
| 0 | 1 | 0 | 0 | 0 | 4 | 4 | 1 | 1 | 0 | 0 | 0 | 12 | 12 |
| 0 | 1 | 0 | 0 | 1 | 5 | 4 | 1 | 1 | 0 | 0 | 1 | 13 | 12 |
| 0 | 1 | 0 | 1 | 0 | 5 | 5 | 1 | 1 | 0 | 1 | 0 | 13 | 13 |
| 0 | 1 | 0 | 1 | 1 | 6 | 5 | 1 | 1 | 0 | 1 | 1 | 14 | 13 |
| 0 | 1 | 1 | 0 | 0 | 6 | 6 | 1 | 1 | 1 | 0 | 0 | 14 | 14 |
| 0 | 1 | 1 | 0 | 1 | 7 | 6 | 1 | 1 | 1 | 0 | 1 | 15 | 14 |
| 0 | 1 | 1 | 1 | 0 | 7 | 7 | 1 | 1 | 1 | 1 | 0 | 15 | 15 |
| 0 | 1 | 1 | 1 | 1 | 8 | 7 | 1 | 1 | 1 | 1 | 1 | 16 | 15 |
| 1 | 0 | 0 | 0 | 0 | 8 | 8 | 0 | 0 | 0 | 0 | 0 | 16 | 16 |

Note: The A and N values in the register setting represent the assertion and negation periods (in clock-cycle units). The numerical value is applicable to the A and N values in AC characteristics.

• Set value for asynchronous setup time register and S value

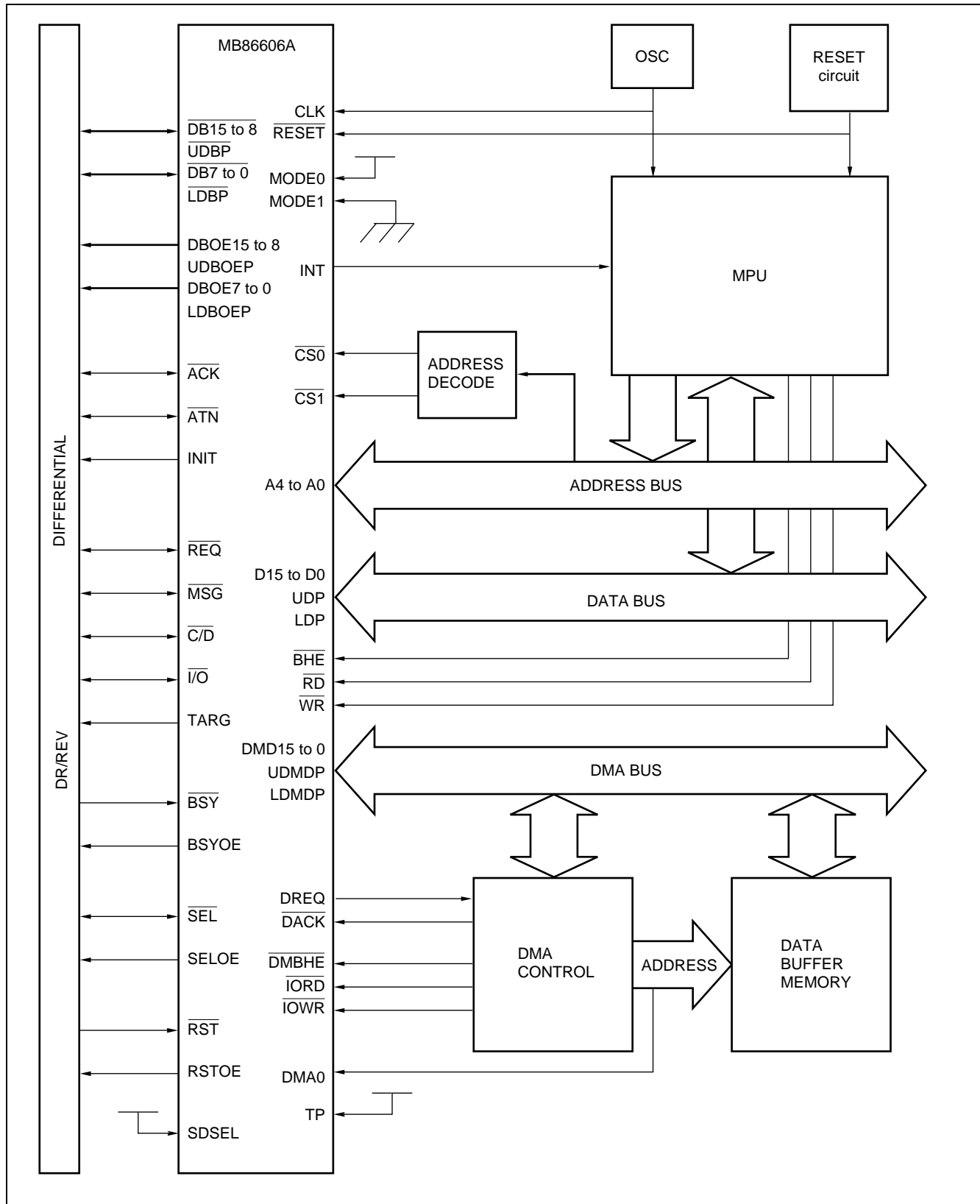
| Asynchronous setup time setting register | | | | S |
|--|---|---|---|----|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |
| 0 | 0 | 0 | 0 | 16 |

Note: The S (setup time) value of the setup time setting register in asynchronous data transfer represents the time required to assert the $\overline{\text{REQ}}$ or $\overline{\text{ACK}}$ signal after setting data at the data bus (in clock-cycle units). The numerical value is applicable to the S value in AC characteristics.

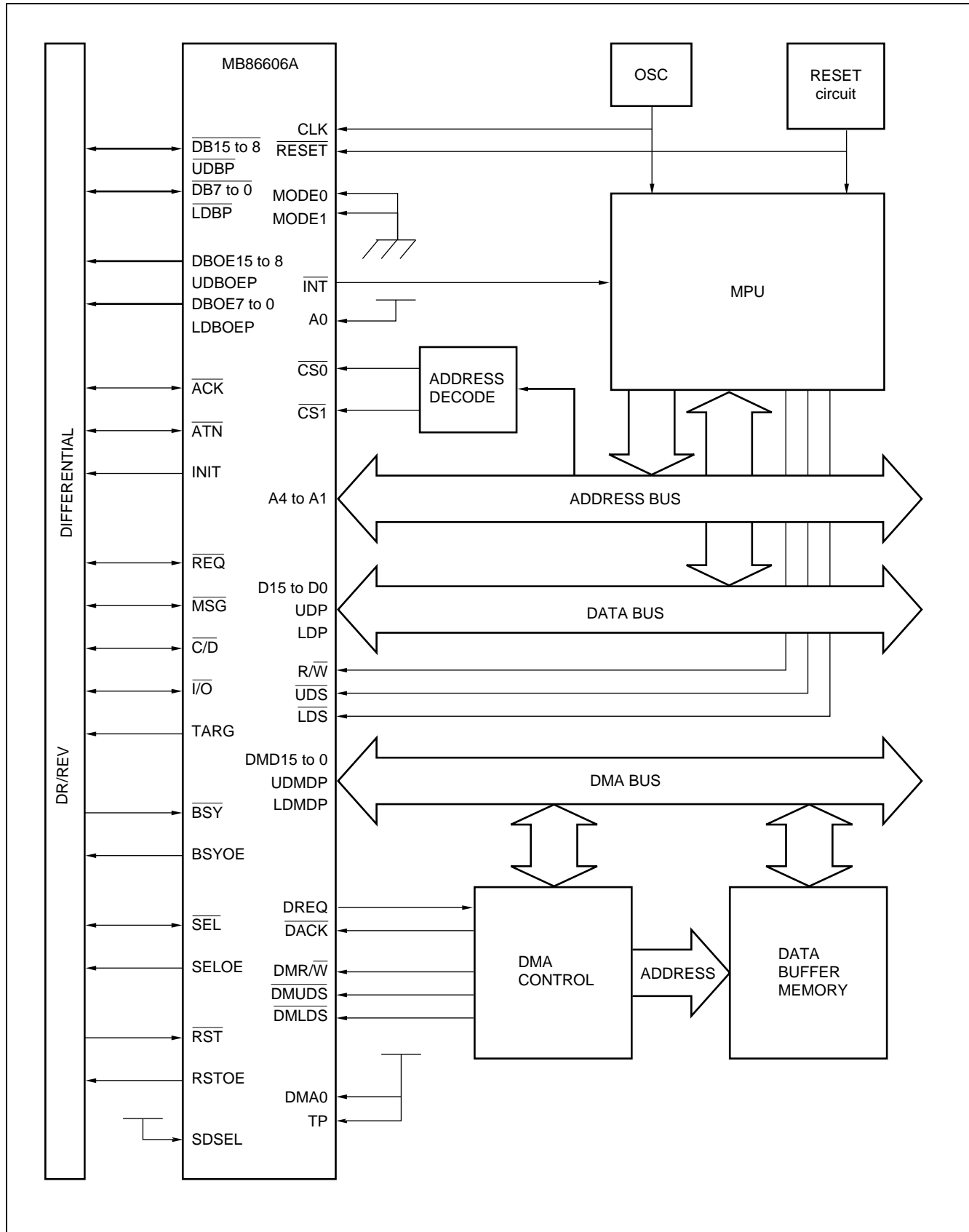
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SYSTEM CONFIGURATION

1. 80-Series Separate Bus Type

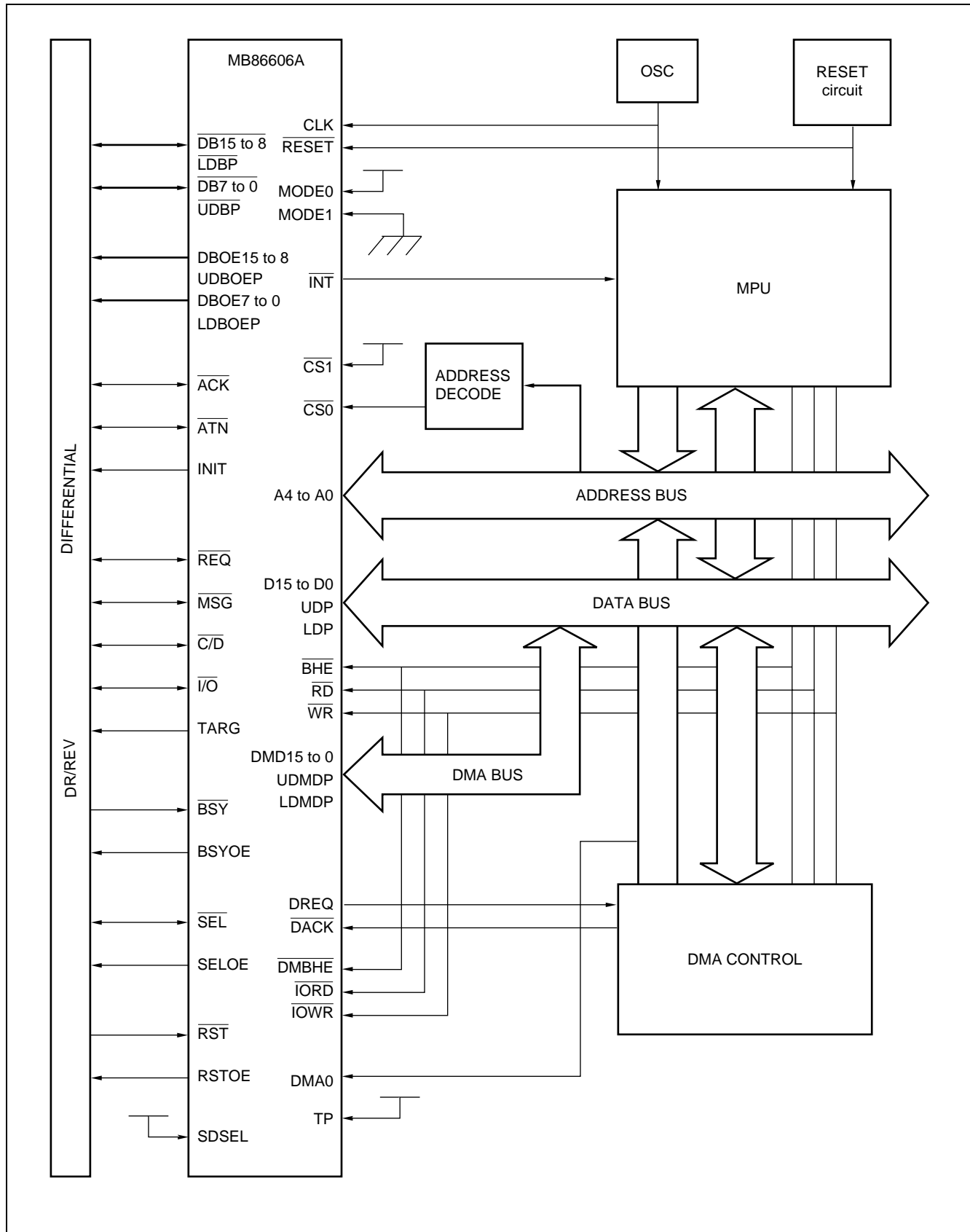


2. 68-Series Separate Bus Type

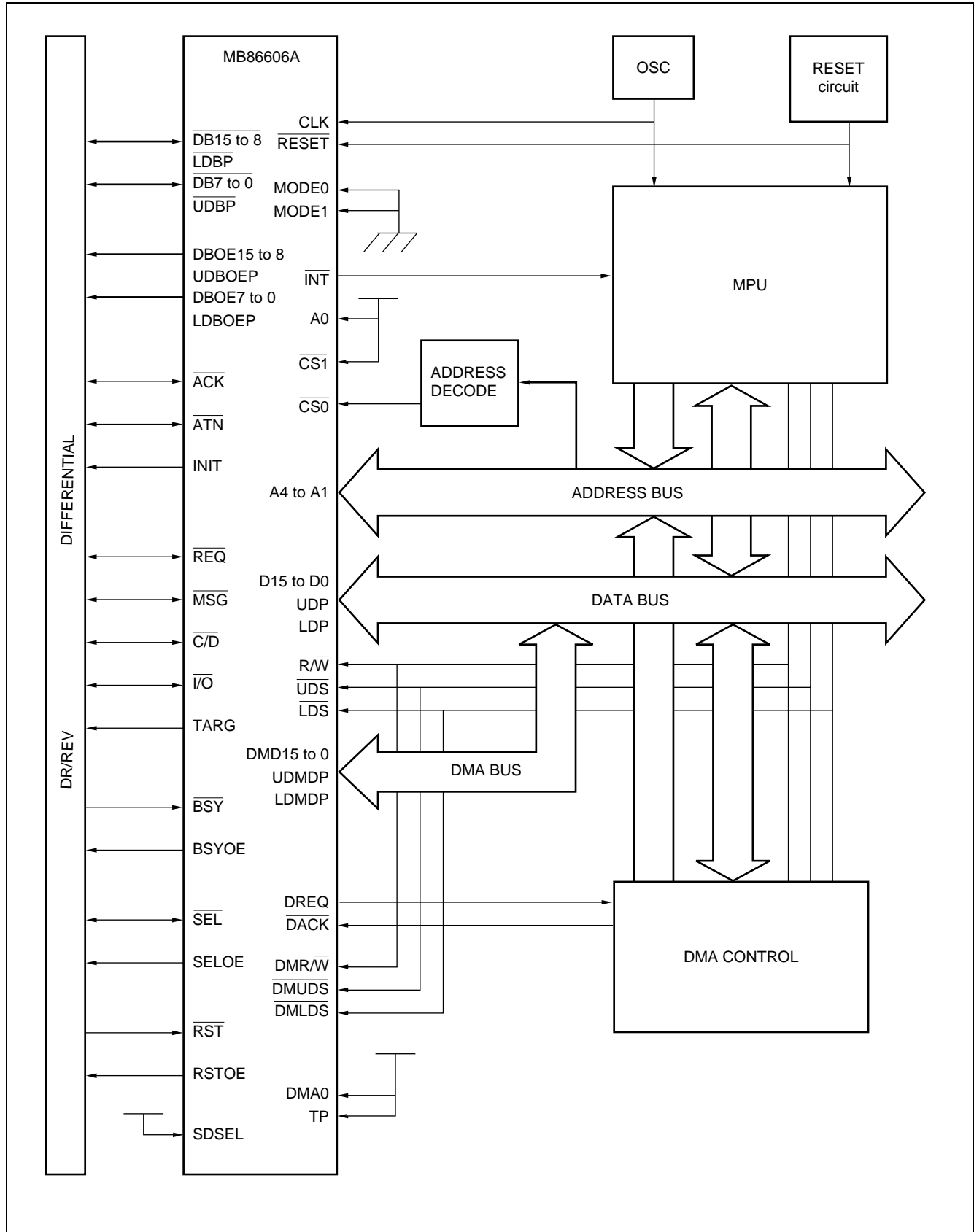


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3. 80-Series Common Bus Type

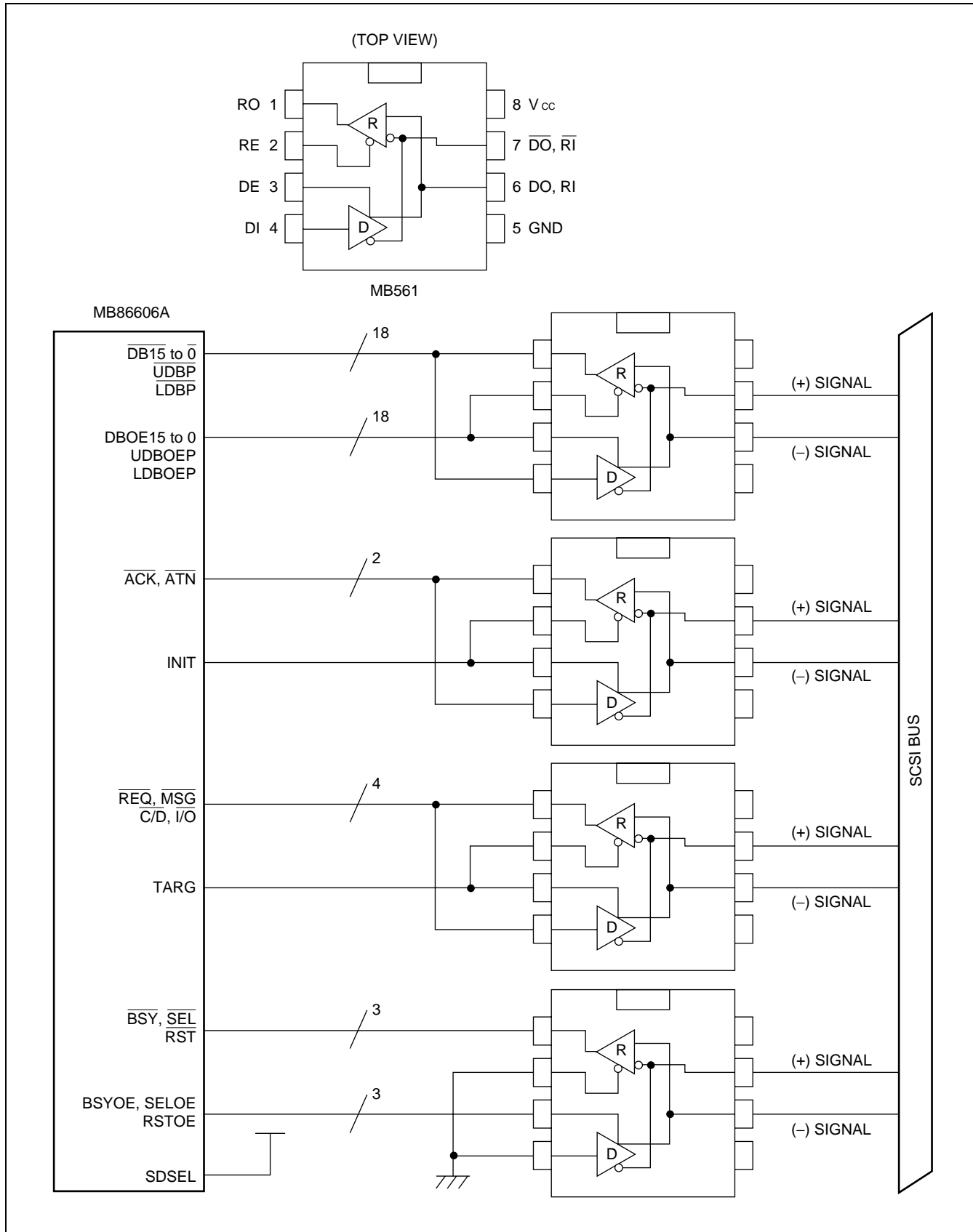


4. 68-Series Common Bus Type

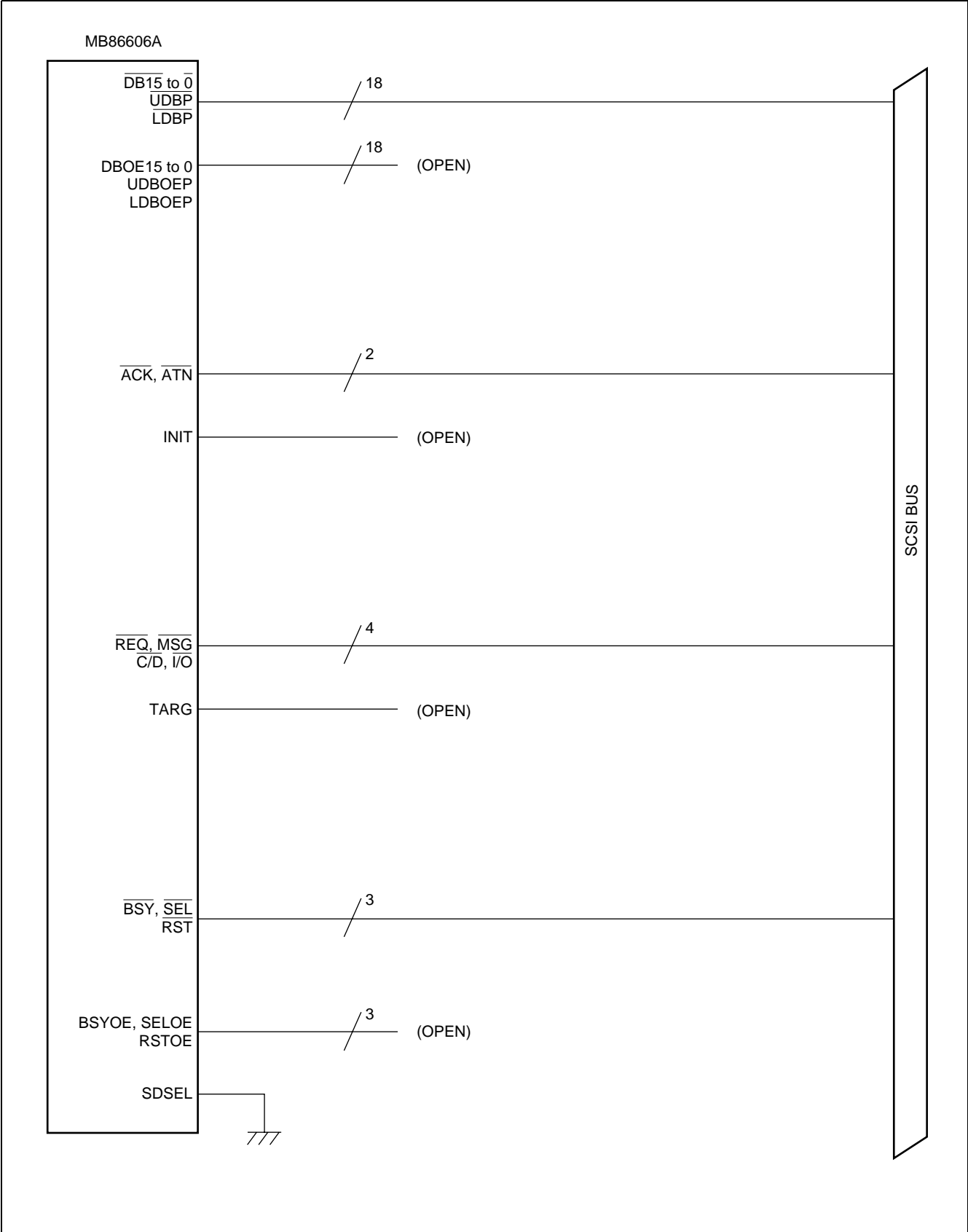


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5. Example of Connection in Differential Mode (Example of Driver/Receiver Connection)



6. Example of Connection in Single-end Mode



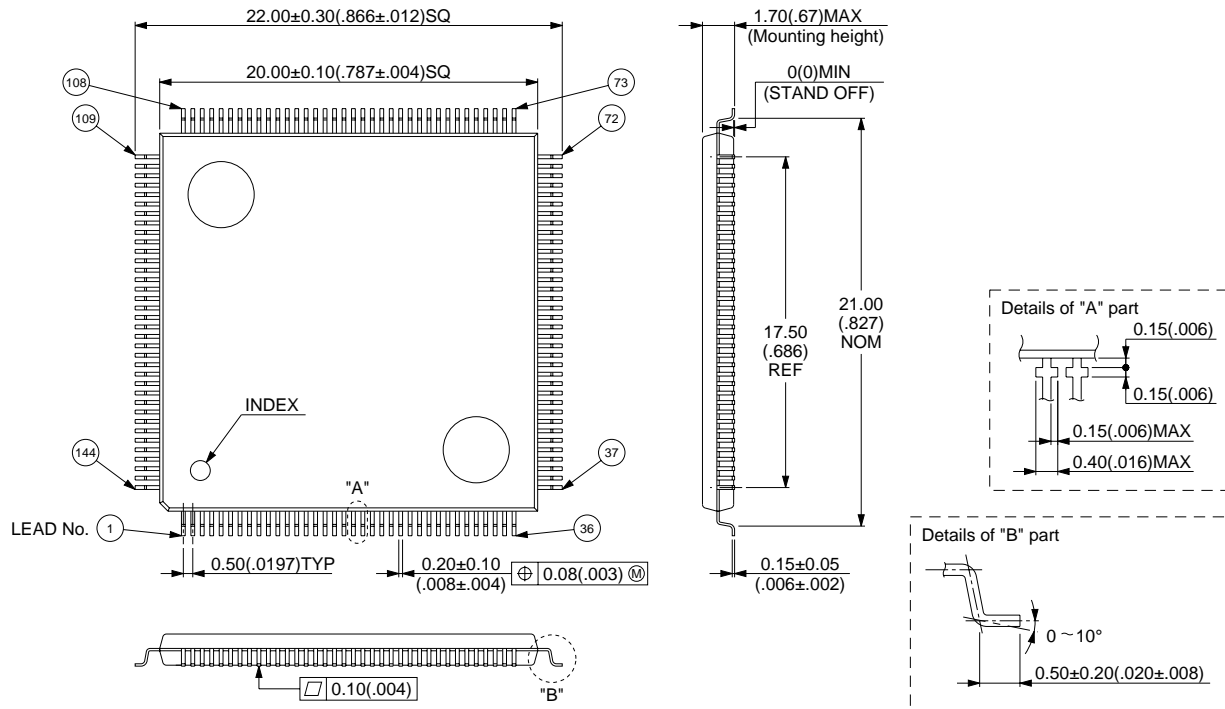
MB86606A

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|--------------|--|---------|
| MB86606APMT2 | 144-pins, Plastic LQFP (FPT-144P-M08) | |

■ PACKAGE DIMENSION

144-pin plastic LQFP
(FPT-144P-M08)



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Dimensions in mm (inches)

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