

Linear IC Converter

CMOS

A/D Converter

(With 4-channel Input at 12-bit Resolution)

MB88101A

■ DESCRIPTION

The MB88101A is an analog-to-digital converter that converts its analog input to a 12-bit digital value and outputs it as serial data.

The MB88101A employs a successive approximation method for A/D conversion.

The MB88101A has four input channels selectable for analog input under control of the dedicated external pins.

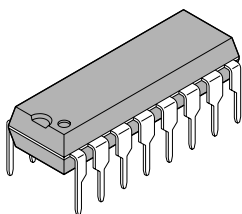
The MB88101A can be switched to a mode for continuous A/D conversion, in which it outputs serial data from the MSB or LSB selectable depending on the mode setting.

■ FEATURES

- 4-channel analog input
- One analog input channel selectable for conversion by external control
- CR-type successive approximation system with a sample-and-hole circuit
- 12-bit resolution
- Serial output of 12-bit digital data
- Capable of continuous conversion (continuous conversion mode)
- MSB or LSB selectable for serial output
- CMOS process
- Package options of 16-pin DIP, SSOP, and SOP available

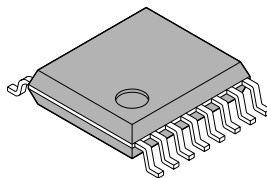
■ PACKAGES

16-pin Plastic DIP



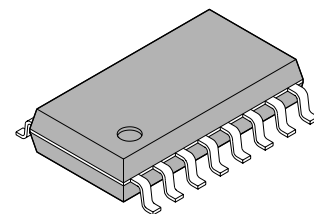
(DIP-16P-M04)

16-pin Plastic SSOP



(FPT-16P-M05)

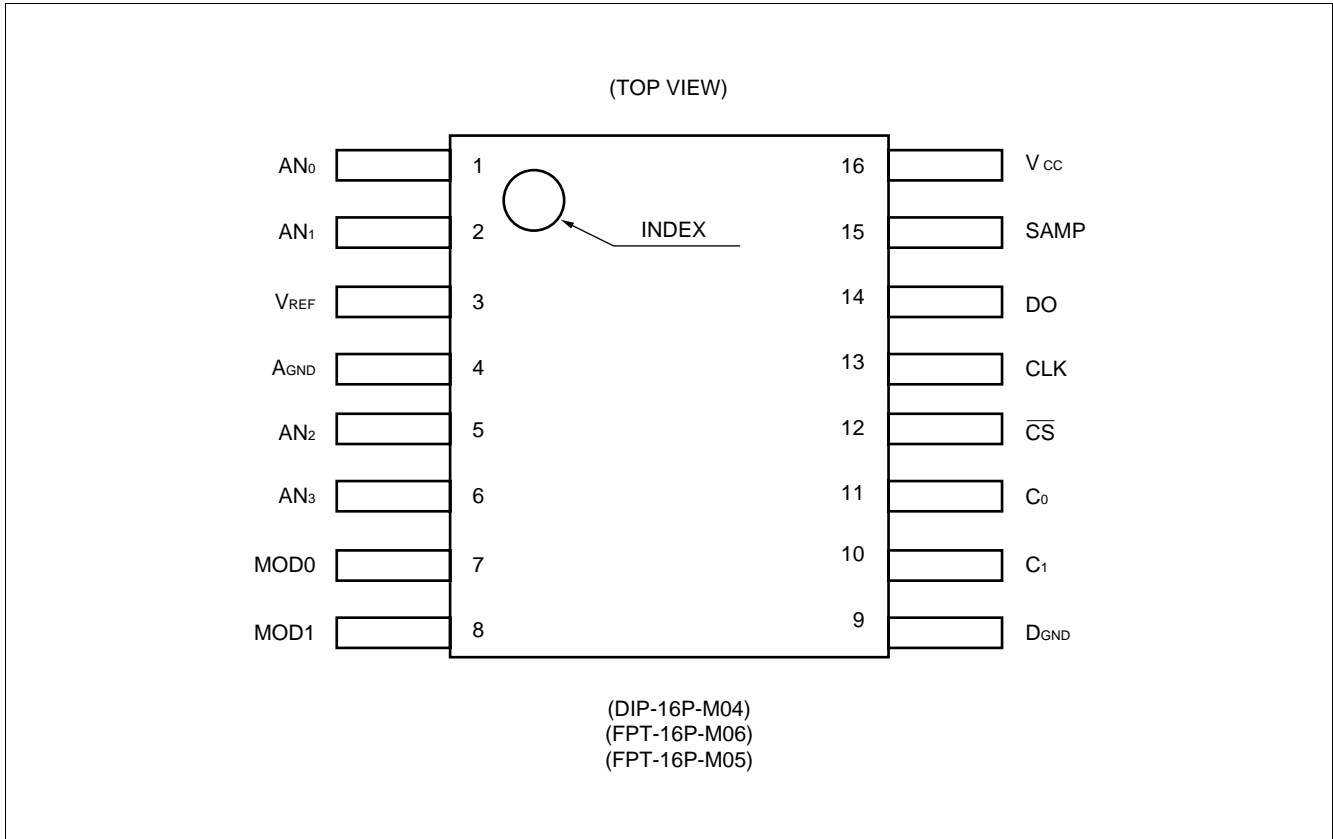
16-pin Plastic SOP



(FPT-16P-M06)

MB88101A

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

| Pin no. | Symbol | I/O | Descriptions |
|------------------|--|-----|---|
| 1 2 5 6 | AN ₀ AN ₁ AN ₂ AN ₃ | I | Analog input pins. One of these channels can be selected depending on the C ₀ and C ₁ settings. |
| 14 | DO | O | This pin outputs the result of A/D conversion. The result is 12-bit serial data output in synchronization with the rise of CLK. |
| 13 | CLK | I | Clock input pin for A/D conversion |
| 12 | \overline{CS} | I | Chip select signal input pin. Setting the signal level to "L" after turning the power on starts A/D conversion; setting it to "H" stops A/D conversion. When this pin is "H", the DO and SAMP pins are "Hi-z". |
| 11 10 | C ₀ C ₁ | I | Input pins for selecting the analog input channels from among pins AN ₀ to AN ₃ . See Table 1 for the correspondence between the pin settings and the channels selected. To switch the channel in mode 2 or 3, set these pins before the SAMP pin goes "H". |
| 7 8 | MOD0 MOD1 | I | Conversion mode setting pins. For the correspondence between the pin settings and the modes selected, see Table 2 and "■ FUNCTIONAL DESCRIPTION." |
| 15 | SAMP | O | This pin becomes active in prior to data output. Serial data is output from the DO pin three clock cycles after the signal level at this pin goes "L" after "H" for one clock cycle. |
| 3 | V _{REF} | — | Reference voltage input pin |
| 4 | A _{GND} | — | Analog circuit ground pin |
| 9 | D _{GND} | — | Digital circuit ground pin |
| 16 | V _{CC} | — | Power supply pin |

• Channel selection

Table 1 Pin Settings and Channel Selection

| C ₁ | C ₀ | Channel |
|----------------|----------------|-----------------|
| L | L | AN ₀ |
| L | H | AN ₁ |
| H | L | AN ₂ |
| H | H | AN ₃ |

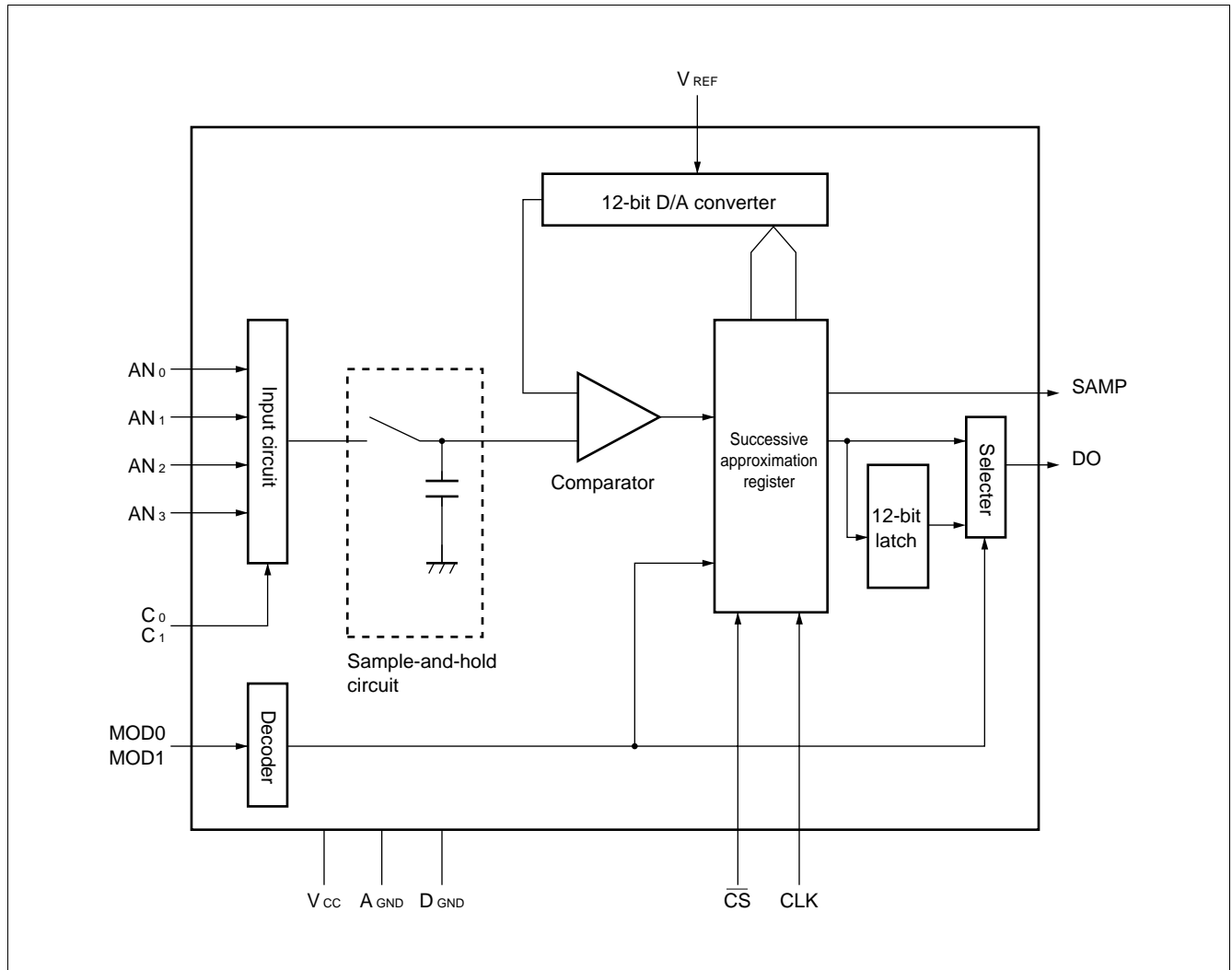
• Mode selection

Table 2 Pin Settings and Mode Selection

| MOD 0 | MOD1 | Mode |
|-------|------|------------|
| L | L | Mode 1 |
| L | H | Mode 2 |
| H | L | (Disabled) |
| H | H | Mode 3 |

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■ BLOCK DIAGRAM

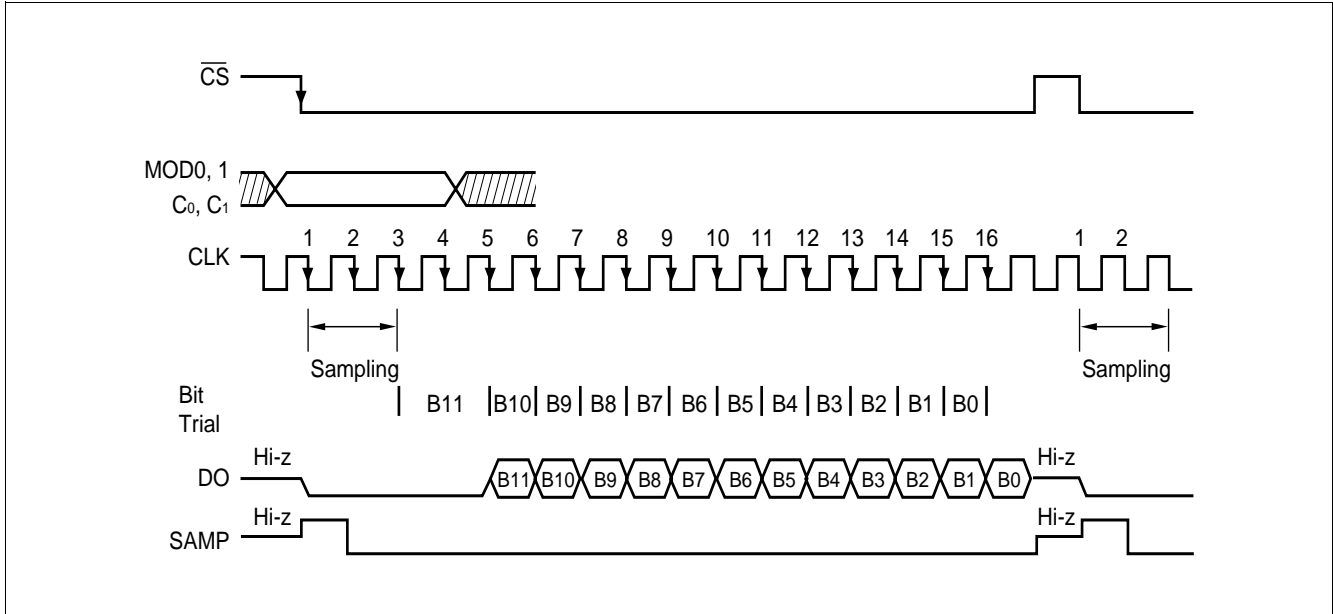


FUNCTIONAL DESCRIPTION

1. Mode 1

This mode sets the DO pin to "L" and stops conversion upon completion of conversion of 12 bits. To restart conversion, set CS to "H" once then to "L". In this mode, converted data is output from the MSB.

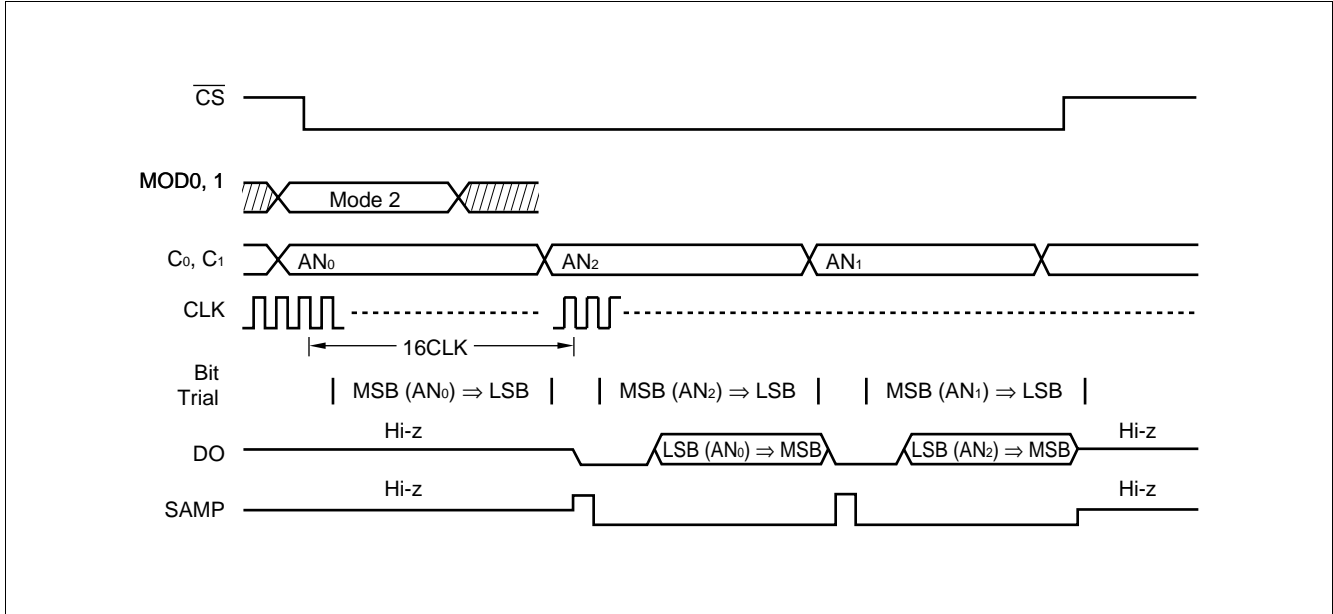
Timing diagram



2. Mode 2

This mode continues conversion until CS becomes "H" after it becomes "L". Converted data is output from the LSB, with the first piece of converted data output 20 clock cycles after CS becomes "L". Changing the channel select pin settings before starting sampling of one analog input allows another to be converted.

Timing diagram

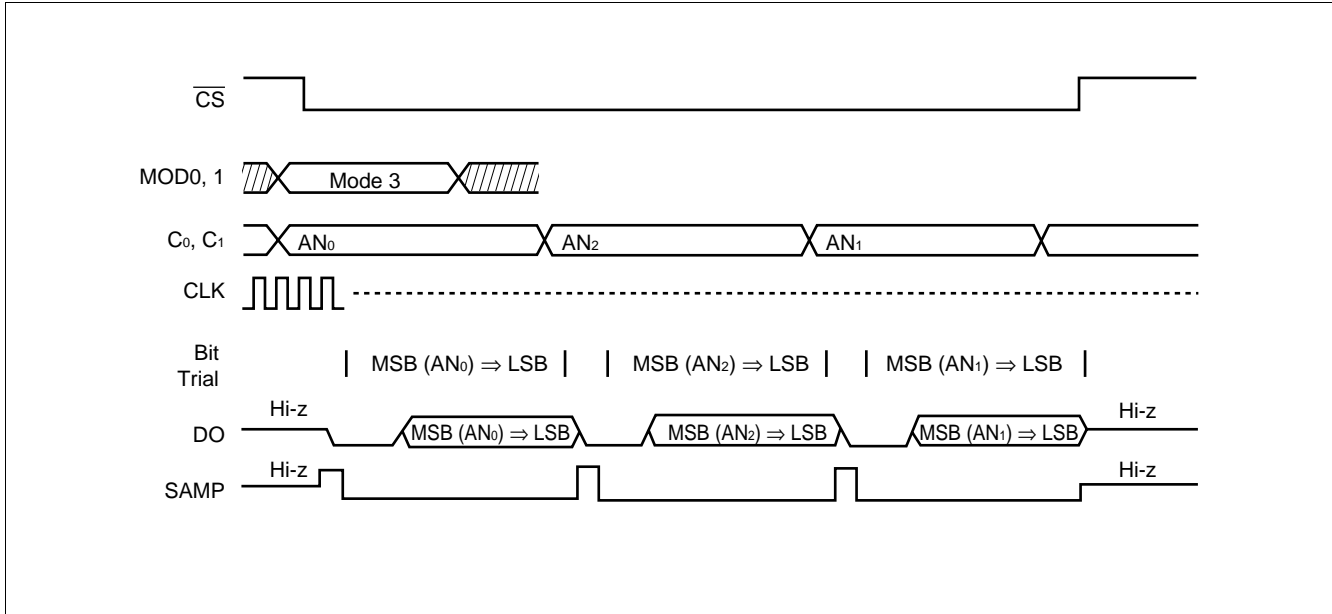


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3. Mode 3

This mode continues conversion until \overline{CS} becomes "H" after it becomes "L". Converted data is output from the MSB. Changing the channel select pin settings before starting sampling of one analog input allows another to be converted.

- Timing diagram



■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Conditions | Rating | | Unit |
|-----------------------|------------------|------------------------------|--------|-----------------------|------|
| | | | Min. | Max. | |
| Power supply voltage | V _{CC} | Based on GND (Ta = +25°C) | -0.3 | +7.0 | V |
| | V _{REF} | | -0.3* | +7.0* | V |
| Input voltage | V _{IN} | | -0.3 | V _{CC} + 0.3 | V |
| Output voltage | V _{OUT} | | -0.3 | V _{CC} + 0.3 | V |
| Power consumption | P _D | — | — | 150 | mW |
| Operating temperature | Ta | — | -20 | +85 | °C |
| Storage temperature | T _{stg} | — | -55 | +150 | °C |

* : V_{CC} ≥ V_{REF}

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|-----------------------|-----------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| Power supply voltage | V _{CC} | 3.3 | — | 5.5 | V |
| | GND | — | 0 | — | V |
| Operation temperature | Ta | -20 | — | +85 | °C |

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ ELECTRICAL CHARACTERISTIC

1. DC Characteristics

(1) Digital section

($V_{CC} = 3.3\text{ V to }5.5\text{ V}$, $D_{GND} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit |
|---------------------------------------|-----------|----------------------------------|--|----------------|------|----------------|---------------|
| | | | | Min. | Typ. | Max. | |
| Power supply voltage | V_{CC} | V_{CC} | — | 3.3 | 5.0 | 5.5 | V |
| Power supply current | I_{CC} | | Operation at CLK = 166kHz (with no load) | — | 0.8 | 2.0 | mA |
| Input leakage current | I_{ILK} | MOD0, 1 CLK CS C0 C1 | $V_{IN} = 0\text{ to }V_{CC}$ | -10 | — | 10 | μA |
| Low-level input voltage | V_{IL} | | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V |
| High-level input voltage | V_{IH} | | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V |
| High-impedance output leakage current | I_{OLZ} | DO SAMP | $V_{IN} = 0\text{ to }V_{CC}$ | -10 | — | 10 | μA |
| Low-level output voltage | V_{OL} | | $I_{OL} = 2.5\text{ mA}$ | — | — | 0.4 | V |
| High-level output voltage | V_{OH} | | $I_{OH} = -400\ \mu\text{A}$ | $V_{CC} - 0.4$ | — | — | V |

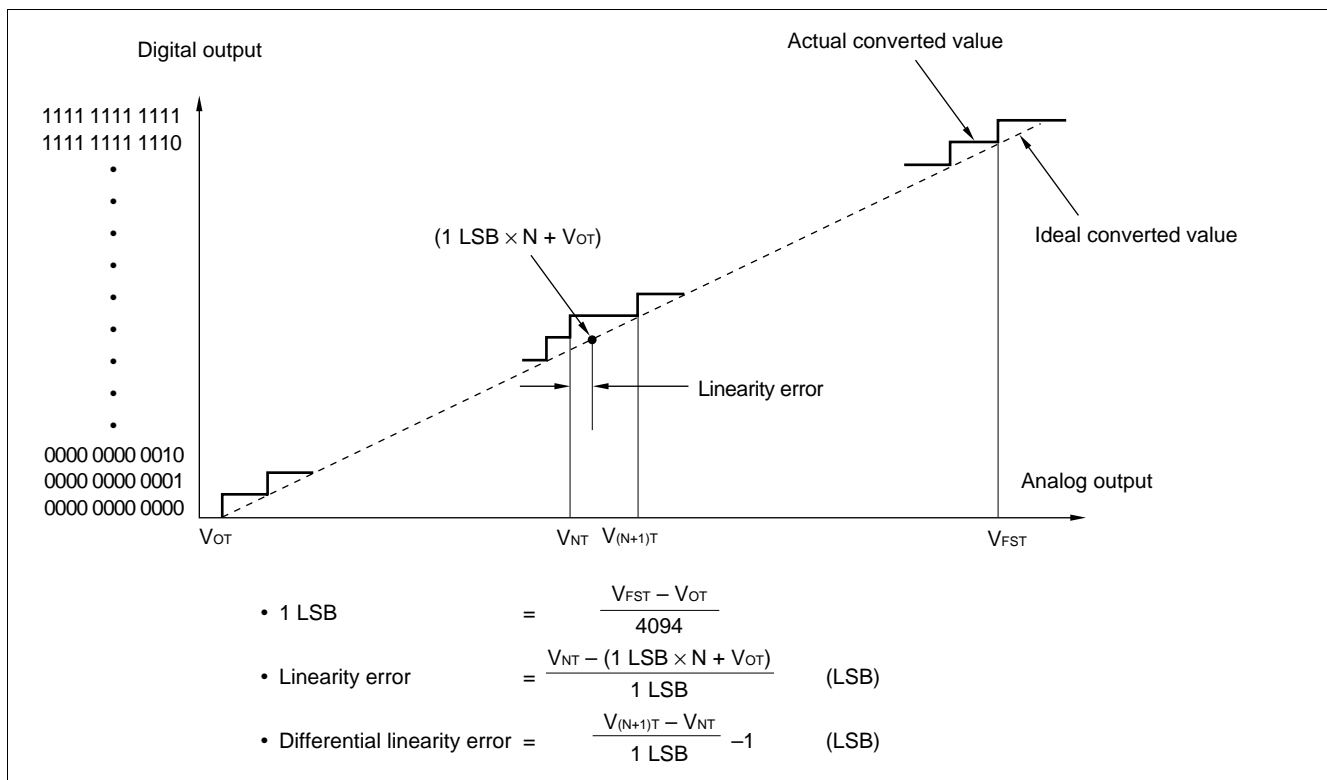
(2) Analog section

($V_{REF}, V_{CC} = 3.3\text{ V to }5.5\text{ V}$ ($V_{CC} \geq V_{REF}$), $A_{GND} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

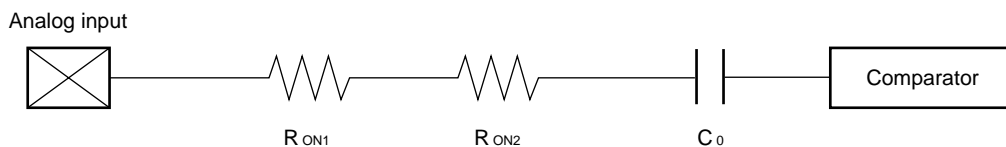
| Parameter | Symbol | Pin name | Value | | | Unit |
|------------------------------|-----------|------------|-------|------|-----------|---------------|
| | | | Min. | Typ. | Max. | |
| Resolution | — | AN0 to AN3 | — | 12 | — | bits |
| Linearity error | — | | -4.0 | — | 2.0 | LSB |
| Differential linearity error | — | | -1.0 | — | 3.0 | LSB |
| Conversion time | — | — | — | 16 | — | CLK |
| Consumption current | I_{REF} | V_{REF} | — | 100 | 300 | μA |
| Analog reference voltage | — | | 3.3 | 5.0 | V_{CC} | V |
| Analog input voltage | — | AN0 to AN3 | 0 | — | V_{REF} | V |

(3) Definitions of A/D converter terms

- Resolution
Analog transition identifiable by the A/D converter
- Linearity error
Deviation of the straight line drawn between the zero transition point (0000 0000 0000 ↔ 0000 0000 0001) and the full-scale transition point (1111 1111 1110 ↔ 1111 1111 1111) of the device from actual conversion characteristics
- Differential linearity error
Deviation from the ideal input voltage required to shift output code by one LSB



• Analog input equivalent circuit



- R_{ON1} = About 1.5 k Ω
- R_{ON2} = About 1.5 k Ω
- C_0 = About 60 pF

Note: The above values are reference values.

- Notes:
- The tolerance of output impedance of an external circuit connected to this A/D converter has an effect on conversion time (CLK frequency). See "■ TYPICAL CHARACTERISTICS".
 - If the output impedance of the external input is too high, the analog voltage sampling time may be short.
 - When turning the device on, turn the power supply for the digital system first before turning V_{REF} on.

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2. AC Characteristics

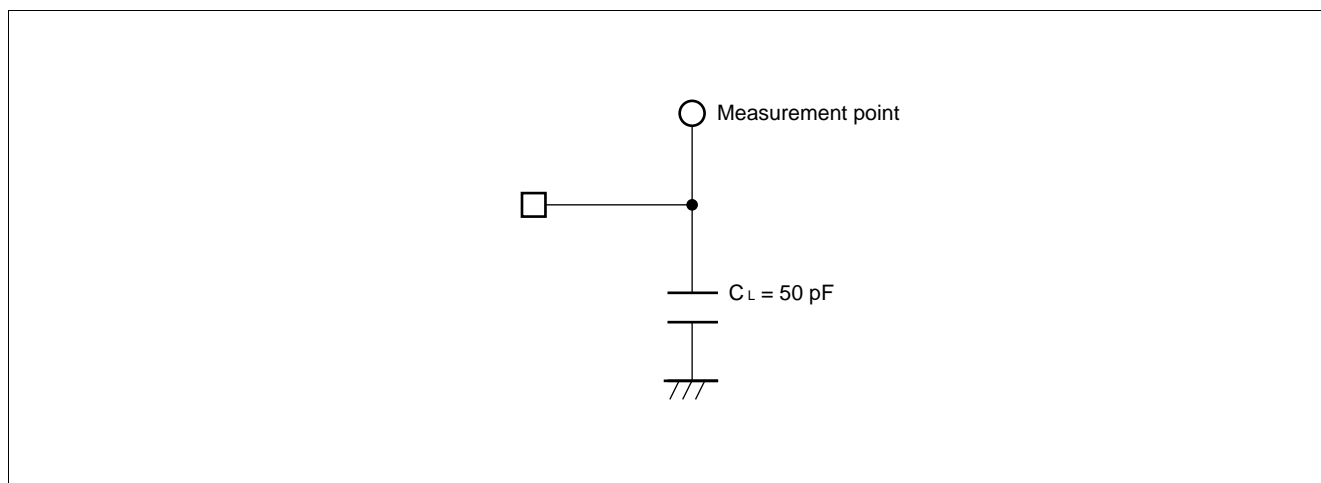
($V_{REF}, V_{CC} = 3.3\text{ V to }+5.5\text{ V}$ ($V_{CC} \geq V_{REF}$), $A_{GND} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

| Parameter | Symbol | Conditions | Value | | Unit |
|-------------------------------------|-----------|-----------------------------------|-----------------|------|---------------|
| | | | Min. | Max. | |
| Clock cycle time | t_{CLK} | $V_{CC} = 5\text{ V} \pm 10\%$ *1 | 1.0 | 30.0 | μs |
| | | — | 6.0 | 30.0 | μs |
| Low-level clock pulse width | t_{CKL} | — | 2.8 | 14.8 | μs |
| High-level clock pulse width | t_{CKH} | — | 2.8 | 14.8 | μs |
| Clock rise time | t_{Cr} | — | — | 0.2 | μs |
| Clock fall time | t_{Cf} | | | | |
| $\overline{\text{CS}}$ setup time | t_{CSS} | — | $t_{CKL} + 0.4$ | — | μs |
| $\overline{\text{CS}}$ hold time | t_{CSH} | — | 1.0 | — | μs |
| $\overline{\text{CS}}$ release time | t_{CSR} | — | 1.0 | — | CLK |
| Channel setup time | t_{CHS} | — | 0 | — | μs |
| Channel hold time | t_{CHH} | — | 1.0 | — | CLK |
| Data output delay time | t_{DO} | *2 | — | 0.5 | μs |
| MOD setup time | t_{MOS} | — | 0.2 | — | μs |
| MOD hold time | t_{MOH} | — | 0.1 | — | μs |
| Data active delay time | t_{DVE} | — | — | 0.5 | μs |
| Data float delay time | t_{DZE} | — | — | 0.5 | μs |
| SAMP active delay time | t_{SVE} | — | — | 0.5 | μs |
| SAMP float delay time | t_{SZE} | — | — | 0.5 | μs |
| SAMP high-level output delay time | t_{SHD} | *2 | — | 0.5 | μs |
| SAMP low-level output delay time | t_{SLD} | *2 | — | 0.5 | μs |

*1: Depending on the output impedance of the external circuit connected to the analog input pin

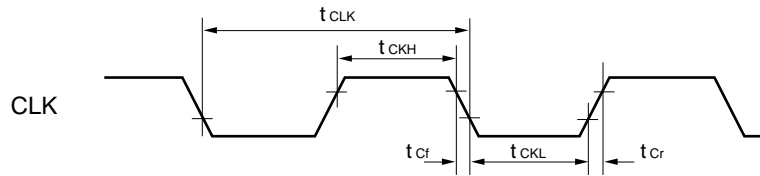
*2: See “• AC test circuit.”

• AC test circuit



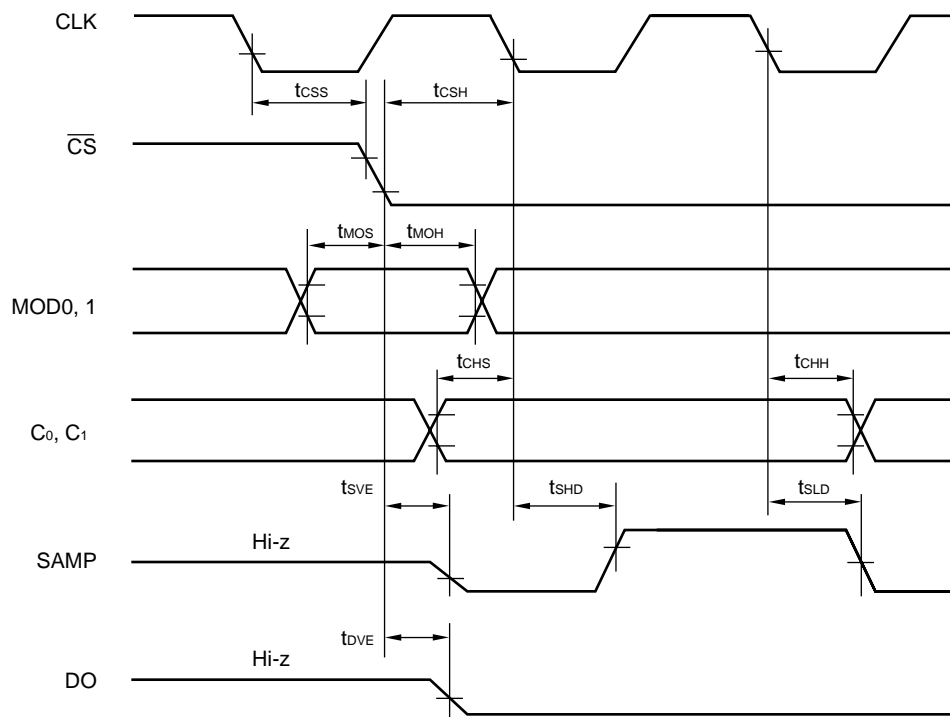
■ TIMING DIAGRAM

(1) Input clock timing



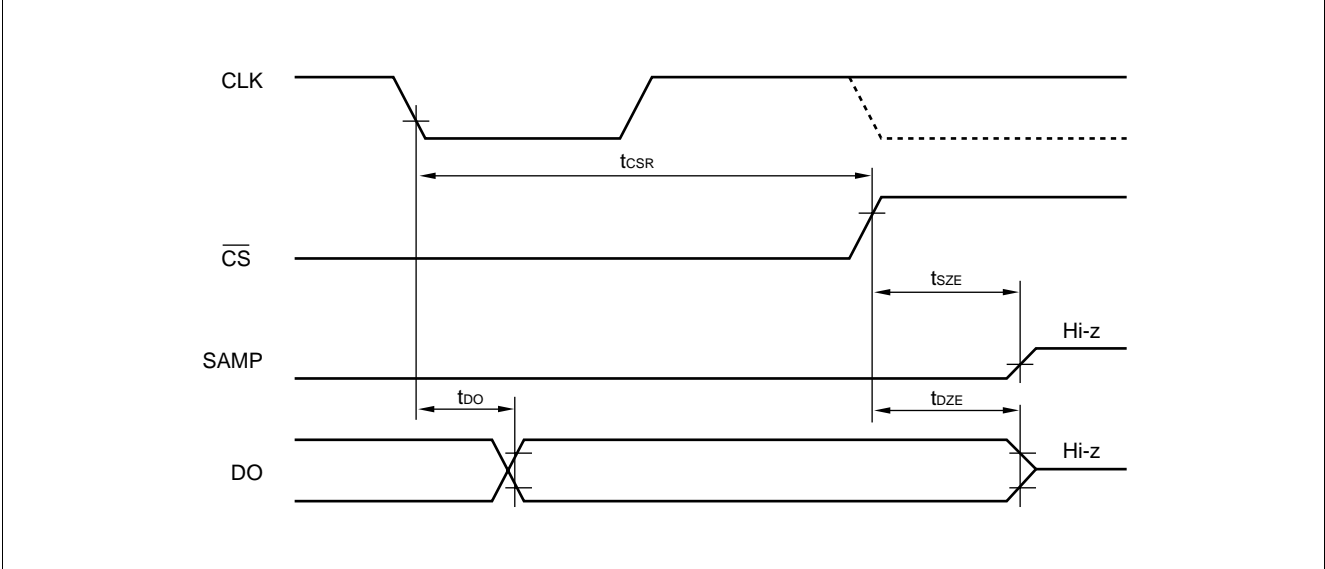
Evaluation levels are 80% and 20% of the V_{CC} .

(2) A/D startup timing

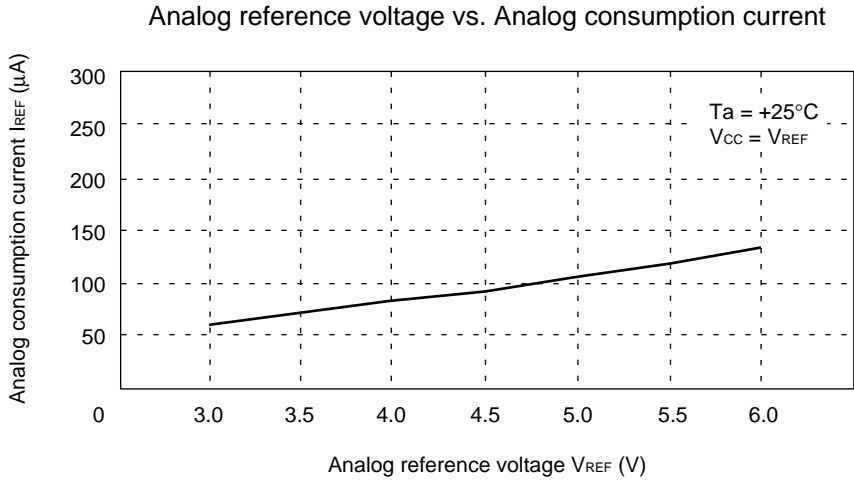
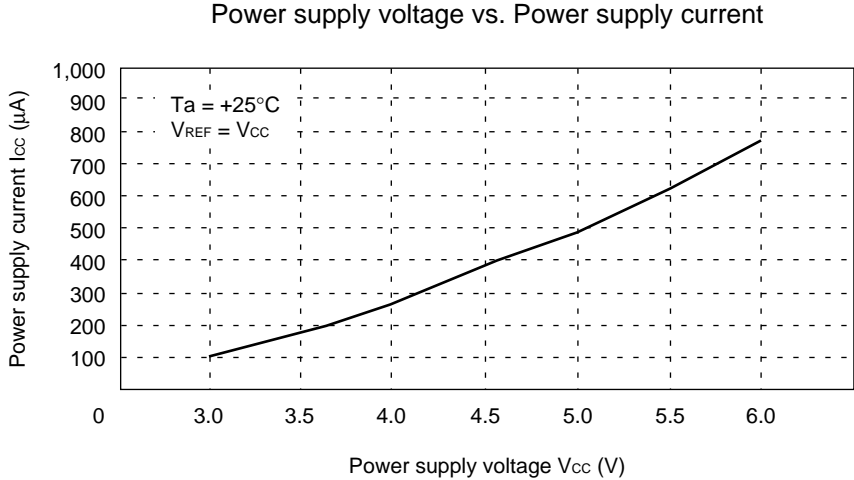


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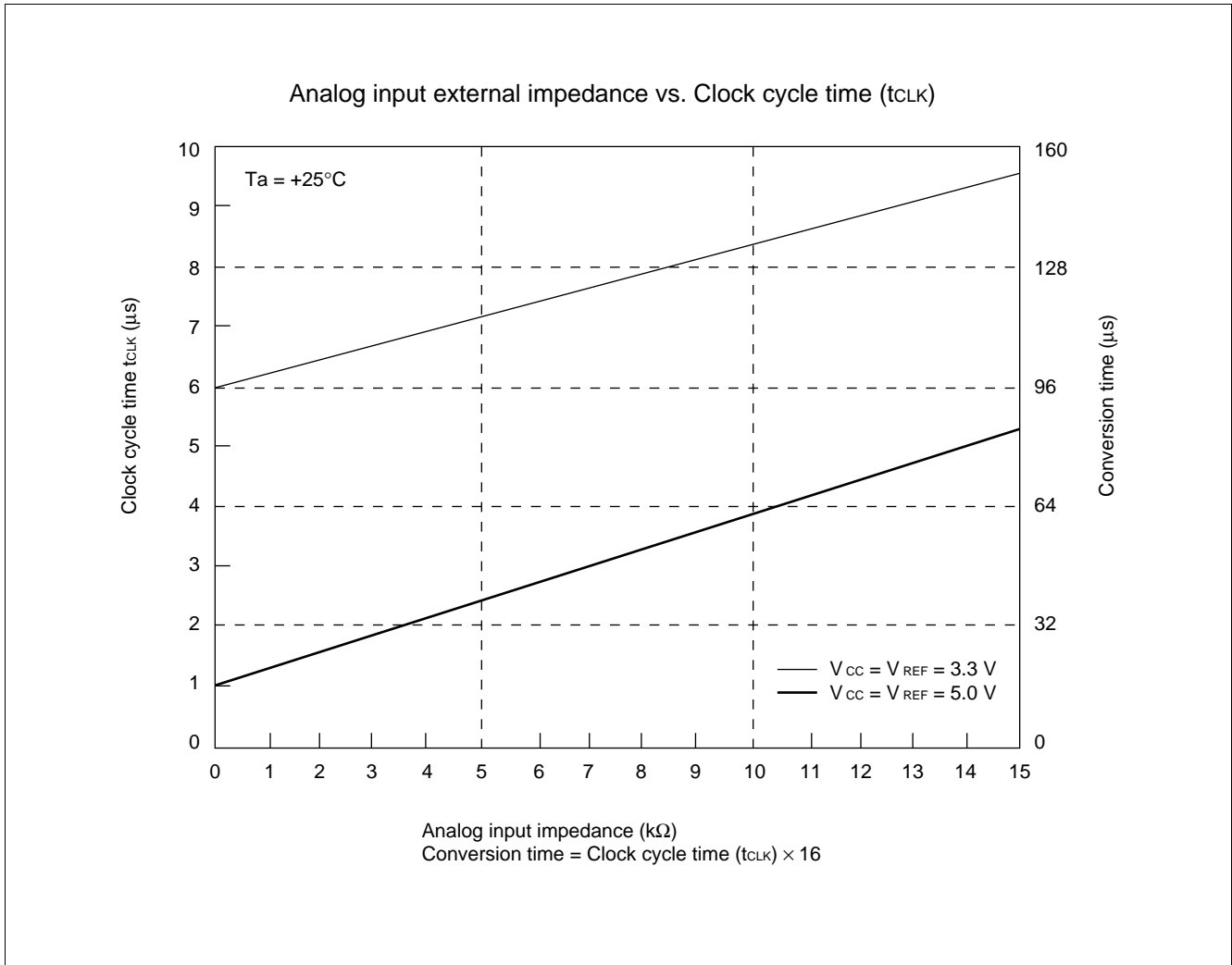
(3) Data output delay time and A/D stop timing



■ TYPICAL CHARACTERISTICS



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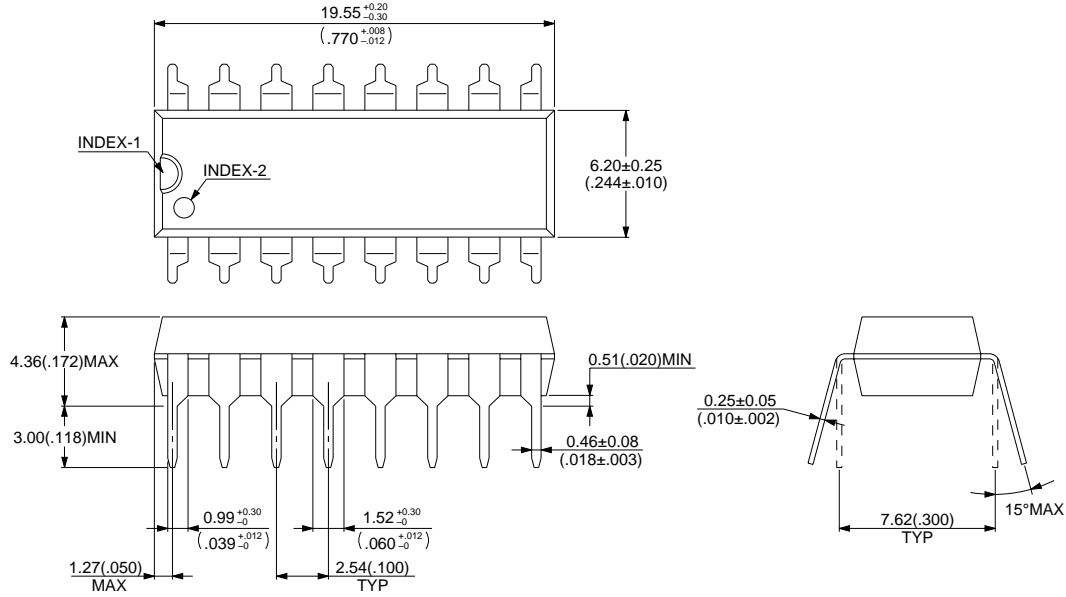
■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------|--------------------------------------|---------|
| MB88101AP | 16-pin Plastic DIP (DIP-16P-M04) | |
| MB88101APFV | 16-pin Plastic SSOP (FPT-16P-M05) | |
| MB88101APF | 16-pin Plastic SOP (FPT-16P-M06) | |

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PACKAGE DIMENSIONS

16-pin Plastic DIP
(DIP-16P-M04)

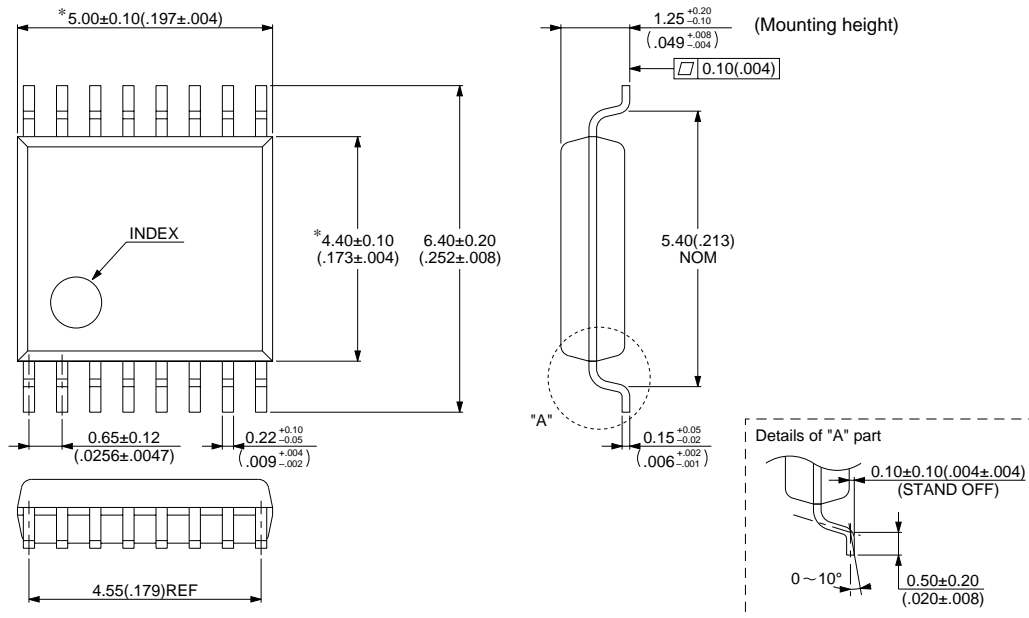


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Dimensions in mm (inches)

16-pin Plastic SSOP
(FPT-16P-M05)

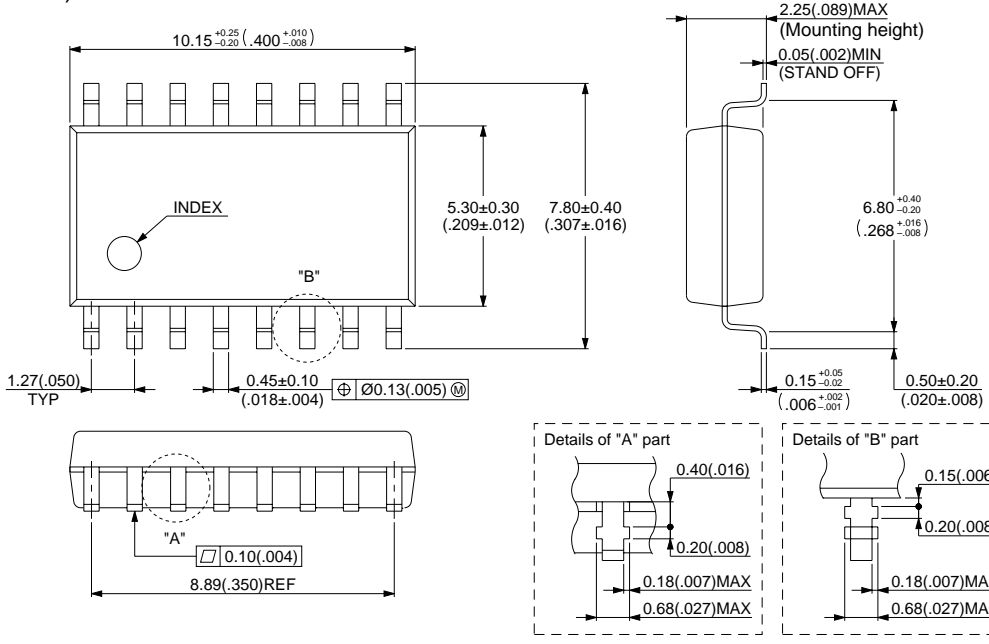
*: This dimension do not include resin protrusion.



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Dimensions in mm (inches)

16-pin Plastic SOP
(FPT-16P-M06)



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Dimensions in mm (inches)

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