

Linear IC Converter

CMOS

D/A Converter for Digital Tuning (12-channel, 8-bit, on-chip OP amp, low-voltage)

MB88346L

■ DESCRIPTION

The Fujitsu MB88346L is an 8-bit D/A converter capable of low-voltage operation, and designed with a built-in amp on each of its 12 analog output lines for large-current drive capability.

The use of serial data input means that only three control lines are required, and enables cascade connection of multiple MB88346L chips.

The MB88346L is suitable for applications such as electronic volume controls and replacement of semi-fixed resistors in tuning systems.

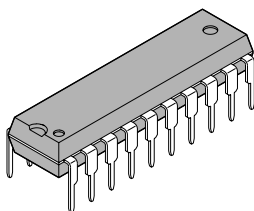
In addition, the MB88346L is both function-compatible and pin-compatible with the MB88346B now in use, allowing easy substitution of the MB88346L for reduced supply voltage.

■ FEATURES

- Low voltage operation (V_{CC}/V_{DD} : 2.7 to 3.6 V)
- Ultra-low power consumption (0.5 mW/ch at $V_{CC} = 3$ V)
- Ultra-compact space-saving package lineup (SSOP-20)
- Contains 12-channel R-2R type 8-bit D/A converter
- On-chip analog output amps (sink current max. 1.0 mA, source current max. 1.0 mA)
- Analog output range from 0 to V_{CC}
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Serial data input, maximum operating speed 2.5 MHz
- (maximum operating speed in cascade connection is 1.5 MHz)
- CMOS process
- Package lineup includes DIP 20-pin, SOP 20-pin, SSOP 20-pin.

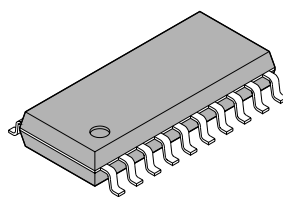
■ PACKAGES

20-pin plastic DIP



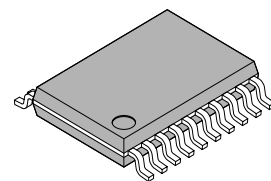
(DIP-20P-M02)

20-pin plastic SOP



(FPT-20P-M01)

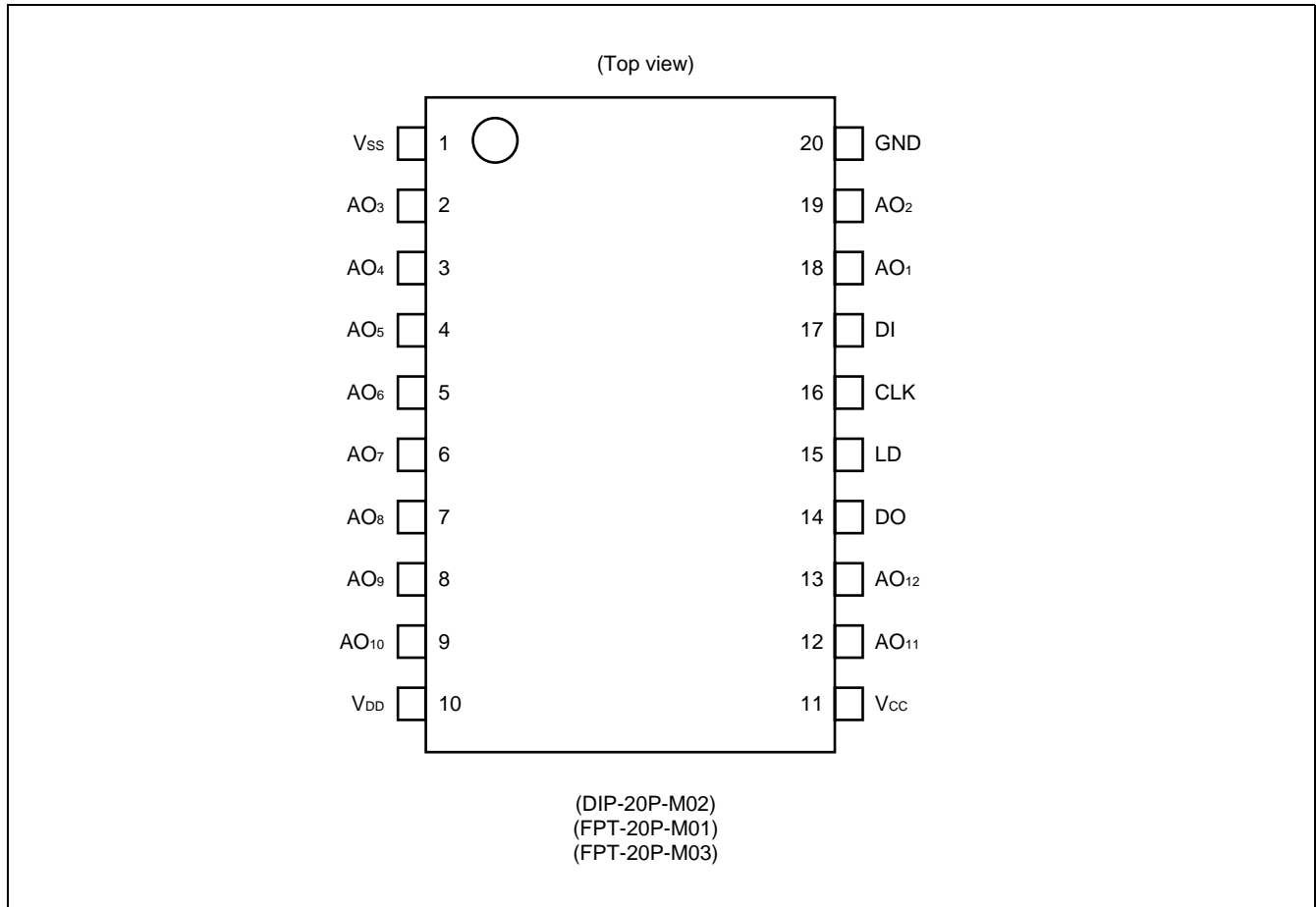
20-pin plastic SSOP



(FPT-20P-M03)

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■ PIN ASSIGNMENT

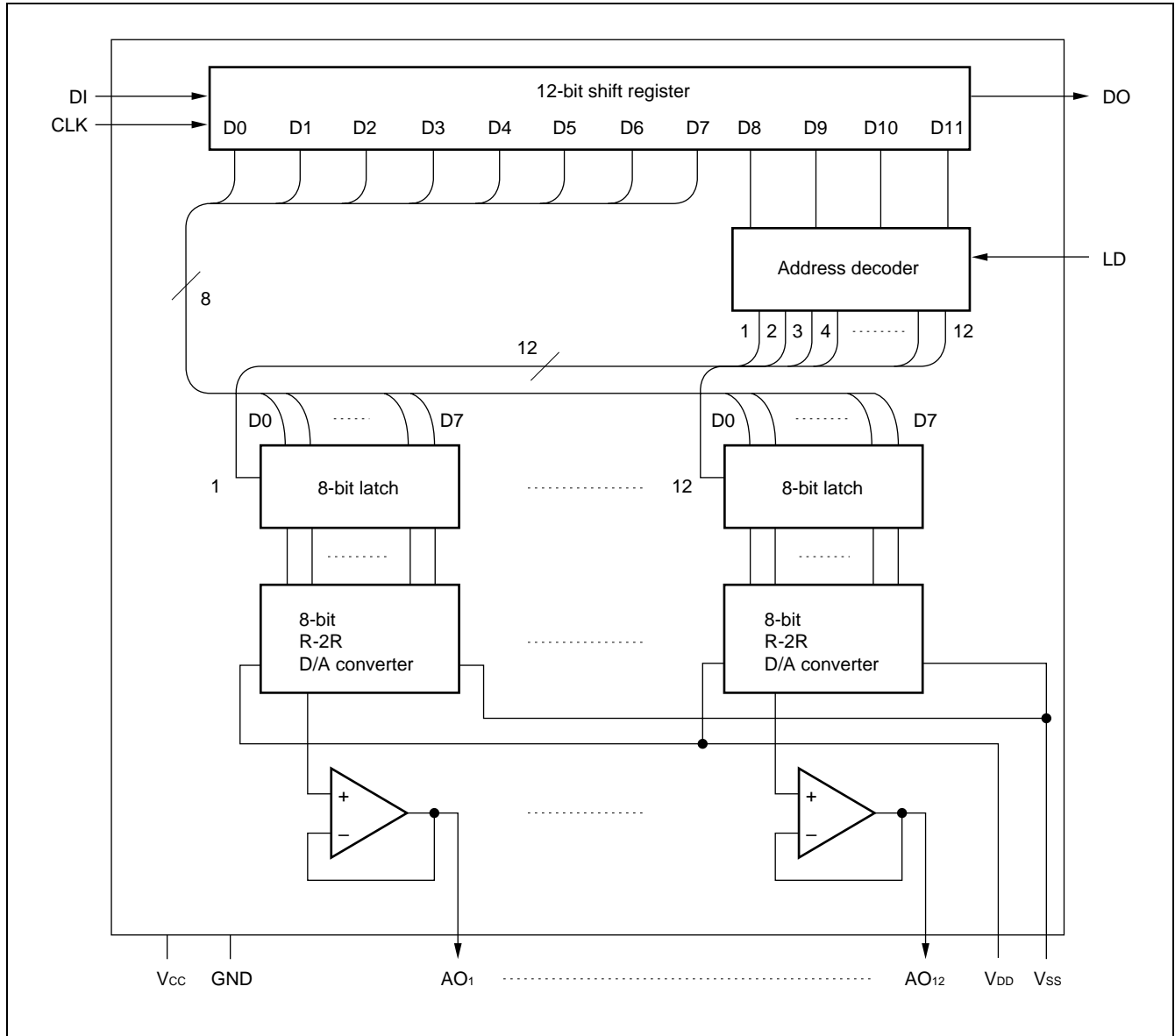


■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
17	DI	I	Serial address/data input to the internal 12-bit shift register: The address/data format is that upper 4 bits (D11 to D8) indicate an address and lower 8 bits (D7 to D0) indicate data. The D11 (MSB) is the first-in bit and D0 (LSB) is the last-in bit.
14	DO	O	Outputs MSB bit data from 12-bit shift register.
16	CLK	I	Shift clock input to the internal 12-bit shift register: At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB).
15	LD	I	Load strobe input for a 12-bit address/data: A high level on the LD pin latches a 4-bit address (upper 4 bits: D11 to D8) of the internal 12-bit shift register into the internal address decoder, and writes 8-bit data (lower 8 bits: D7 to D0) of the shift register into an internal data latch selected by the latched address.
18 19 2 3 4 5 6 7 8 9 12 13	AO ₁ AO ₂ AO ₃ AO ₄ AO ₅ AO ₆ AO ₇ AO ₈ AO ₉ AO ₁₀ AO ₁₁ AO ₁₂	O	8-bit D/A output pins with OP amps.
11	V _{CC}	—	MCU interface and OP amp power supply pin.
20	GND	—	MCU interface and OP amp ground pin.
10	V _{DD}	—	D/A converter power supply pin.
1	V _{SS}	—	D/A converter ground pin.

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■ BLOCK DIAGRAM

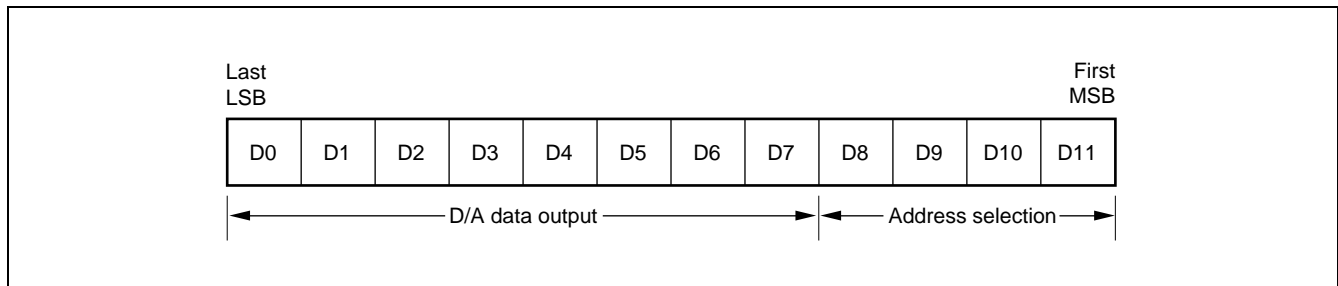


■ DATA CONFIGURATION

The MB88346L has a 12-bit shift register for chip control functions. The 12-bit shift register must be used to set up data in the configuration shown below.

The data configuration has a total of 12 bits, four for address selection and eight for D/A data output.

1. Shift Register Control Data Configuration



2. D/A Converter Control Signals

D0	D1	D2	D3	D4	D5	D6	D7	D/A data output
0	0	0	0	0	0	0	0	$\cong V_{SS}$
1	0	0	0	0	0	0	0	$\cong V_{LB} + V_{SS}$
0	1	0	0	0	0	0	0	$\cong V_{LB} \times 2 + V_{SS}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$\cong V_{LB} \times 254 + V_{SS}$
1	1	1	1	1	1	1	1	$\cong V_{DD}$

$$V_{LB} = (V_{DD} - V_{SS})/255$$

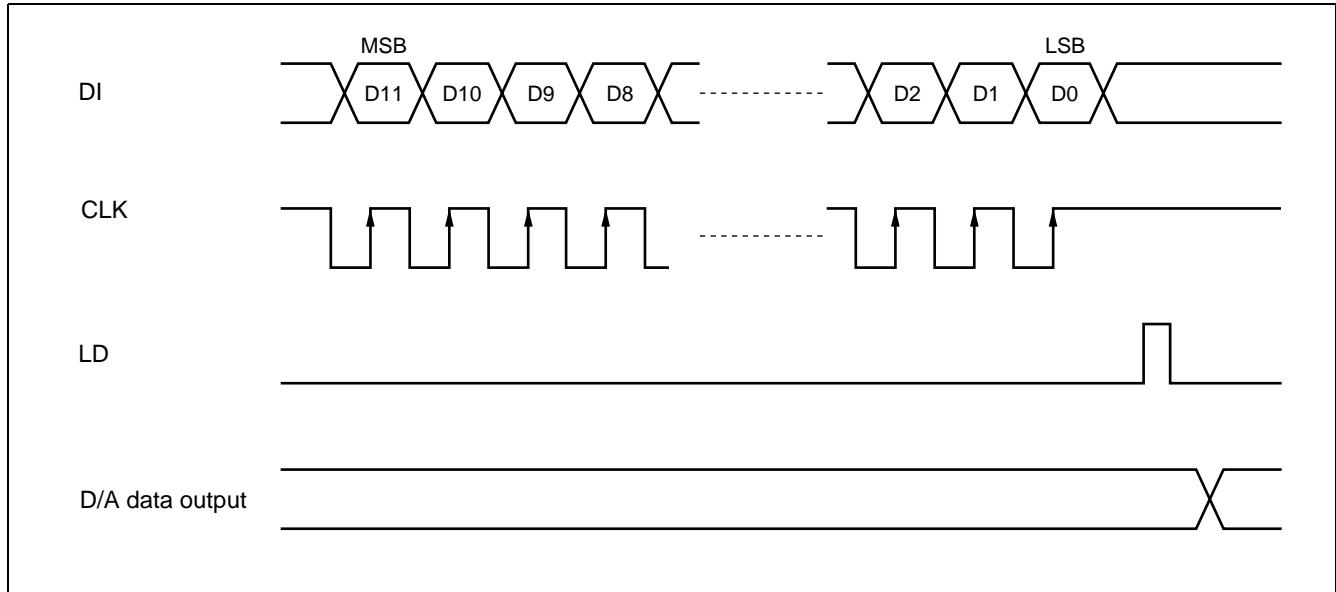
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3. Address Selection Signals

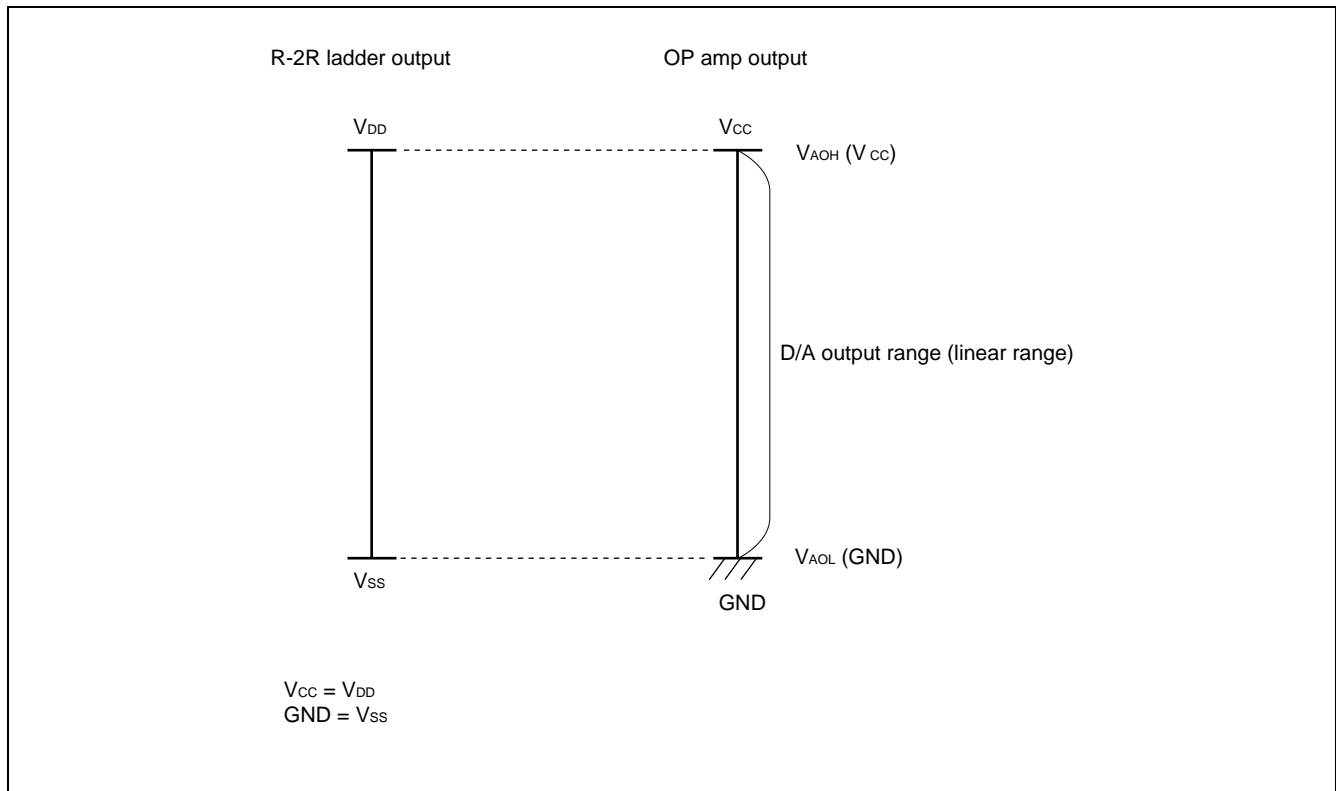
D8	D9	D10	D11	Address selection
0	0	0	0	Don't Care
0	0	0	1	AO ₁ selection
0	0	1	0	AO ₂ selection
0	0	1	1	AO ₃ selection
0	1	0	0	AO ₄ selection
0	1	0	1	AO ₅ selection
0	1	1	0	AO ₆ selection
0	1	1	1	AO ₇ selection
1	0	0	0	AO ₈ selection
1	0	0	1	AO ₉ selection
1	0	1	0	AO ₁₀ selection
1	0	1	1	AO ₁₁ selection
1	1	0	0	AO ₁₂ selection
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

■ OPERATING DESCRIPTION

1. Timing Chart for Data Condition Setup



2. Analog Output Voltage Range



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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
Power supply voltage	V _{CC}	GND used as reference, Ta = 25°C	-0.3	+7.0	V
	V _{DD} *		-0.3	+7.0	V
Input voltage	V _{IN}		-0.3	V _{CC} + 0.3	V
Output voltage	V _{OUT}		-0.3	V _{CC} + 0.3	V
Power consumption	P _D	—	—	250	mW
Operating temperature	Ta	—	-20	+85	°C
Storage temperature	Tstg	—	-55	+150	°C

* : V_{CC} ≥ V_{DD}

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage 1	V _{CC}	—	2.7	—	3.6	V
	GND	—	—	0	—	V
Power supply voltage 2	V _{DD}	V _{DD} - V _{SS} ≥ 2.0 V	2.0	—	V _{CC}	V
	V _{SS}		GND	—	V _{CC} - 2.0	V
Analog output source current	I _{AL}	V _{CC} = 3.0 V	—	—	1.0	mA
Analog output sink current	I _{AH}	V _{CC} = 3.0 V	—	—	1.0	mA
Oscillator limiting output capacity	C _{AL}	—	—	—	0.1	μF
Digital data value range	—	—	#00	—	#FF	—
Operating temperature	Ta	—	-20	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) Digital Block

($V_{DD}, V_{CC} = +2.7\text{ V to }3.6\text{ V}$ ($V_{CC} \geq V_{DD}$), $GND = V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	V_{CC}	V_{CC}	—	2.7	3.0	3.6	V
Power supply current 1	I_{CC}		Stationary (CLK signal stopped), no load	—	1.2	3.0	mA
Input leak current	I_{ILK}	CLK, DI, LD	$V_{IN} = 0\text{ to }V_{CC}$	-10	—	10	μA
L level input voltage	V_{IL}		—	—	—	$0.2 V_{CC}$	V
H level input voltage	V_{IH}		—	$0.8 V_{CC}$	—	—	V
L level output voltage	V_{OL}	DO	$I_{OL} = 2.5\text{ mA}$	—	—	0.4	V
H level output voltage	V_{OH}		$I_{OH} = -400\ \mu\text{A}$	$V_{CC} - 0.4$	—	—	V

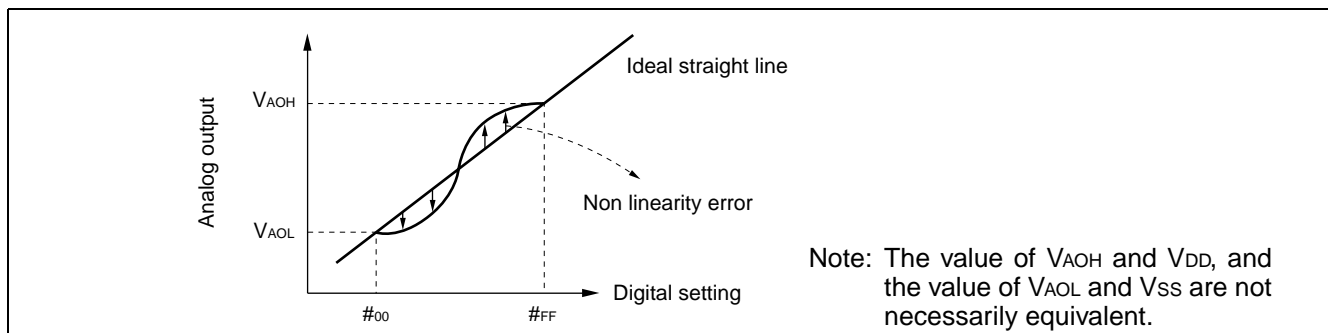
(2) Analog Block 1

($V_{DD}, V_{CC} = +2.7\text{ V to }3.6\text{ V}$ ($V_{CC} \geq V_{DD}$), $GND = V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min.	Typ.	Max.	
Power consumption	I_{DD}	V_{DD}	Maximum setting value from #00 to #FF	—	0.6	1.5	mA
Analog voltage	V_{DD}	V_{DD}	$V_{DD} - V_{SS} \geq 2.0$	2.0	—	V_{CC}	V
	V_{SS}	V_{SS}		GND	—	$V_{CC} - 2.0$	V
Resolution	Res	AO ₁ to AO ₁₂	—	—	8	—	bits
Monotonic increase	Rem		—	—	8	—	bits
Nonlinearity error	LE		$V_{DD} \leq V_{CC} - 0.1\text{ V}$, $V_{SS} \geq 0.1\text{ V}$, no load	-1.5	—	1.5	LSB
Differential linearity error	DLE		-1.0	—	1.0	LSB	

Nonlinearity error: Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at "00" and output voltage at "FF."

Differential linearity error: Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



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(3) Analog Block 2

(V_{DD} , $V_{CC} = +2.7\text{ V to }3.6\text{ V}$ ($V_{CC} \geq V_{DD}$), $GND = V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

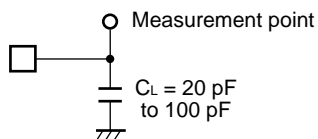
Parameter	Symbol	Pin	Condition	Value			Unit
				Min.	Typ.	Max.	
Output minimum voltage 1	V_{AOL1}	AO ₁ to AO ₁₂	$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AL} = 0\ \mu\text{A}$ Digital data = #00	V_{SS}	—	$V_{SS} + 0.1$	V
Output minimum voltage 2	V_{AOL2}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AL} = 500\ \mu\text{A}$ Digital data = #00	$V_{SS} - 0.2$	V_{SS}	$V_{SS} + 0.2$	V
Output minimum voltage 3	V_{AOL3}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AH} = 500\ \mu\text{A}$ Digital data = #00	V_{SS}	—	$V_{SS} + 0.2$	V
Output minimum voltage 4	V_{AOL4}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AL} = 1.0\text{ mA}$ Digital data = #00	$V_{SS} - 0.3$	V_{SS}	$V_{SS} + 0.3$	V
Output minimum voltage 5	V_{AOL5}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$ $I_{AH} = 1.0\text{ mA}$ Digital data = #00	V_{SS}	—	$V_{SS} + 0.3$	V
Output maximum voltage 1	V_{AOH1}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AL} = 0\ \mu\text{A}$ Digital data = #FF	$V_{DD} - 0.1$	—	V_{DD}	V
Output maximum voltage 2	V_{AOH2}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AL} = 500\ \mu\text{A}$ Digital data = #FF	$V_{DD} - 0.2$	—	V_{DD}	V
Output maximum voltage 3	V_{AOH3}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AH} = 500\ \mu\text{A}$ Digital data = #FF	$V_{DD} - 0.2$	V_{DD}	$V_{DD} + 0.2$	V
Output maximum voltage 4	V_{AOH4}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AL} = 1.0\text{ mA}$ Digital data = #FF	$V_{DD} - 0.3$	—	V_{DD}	V
Output maximum voltage 5	V_{AOH5}		$V_{DD} = V_{CC} = 3.0\text{ V}$, $V_{SS} = GND = 0.0\text{ V}$, $I_{AH} = 1.0\text{ mA}$ Digital data = #FF	$V_{DD} - 0.3$	V_{DD}	$V_{DD} + 0.3$	V

2. AC Characteristics

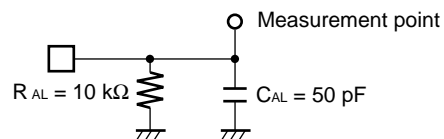
($V_{DD}, V_{CC} = +2.7\text{ V to }3.6\text{ V}$ ($V_{CC} \geq V_{DD}$), $GND = V_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Clock L level pulse width	tCKL	—	200	—	ns
Clock H level pulse width	tCKH	—	200	—	ns
Clock rise time Clock fall time	tCr tCf	—	—	200	ns
Data setup time	tDCH	—	30	—	ns
Data hold time	tCHD	—	60	—	ns
Load setup time	tCHL	—	200	—	ns
Load hold time	tLDC	—	100	—	ns
Load H level pulse width	tLDH	—	100	—	ns
Data output delay time	tDO	See “• Load condition 1”	70	600	ns
D/A output settling time	tLDD	See “• Load condition 2”	—	300	μs

• Load condition 1

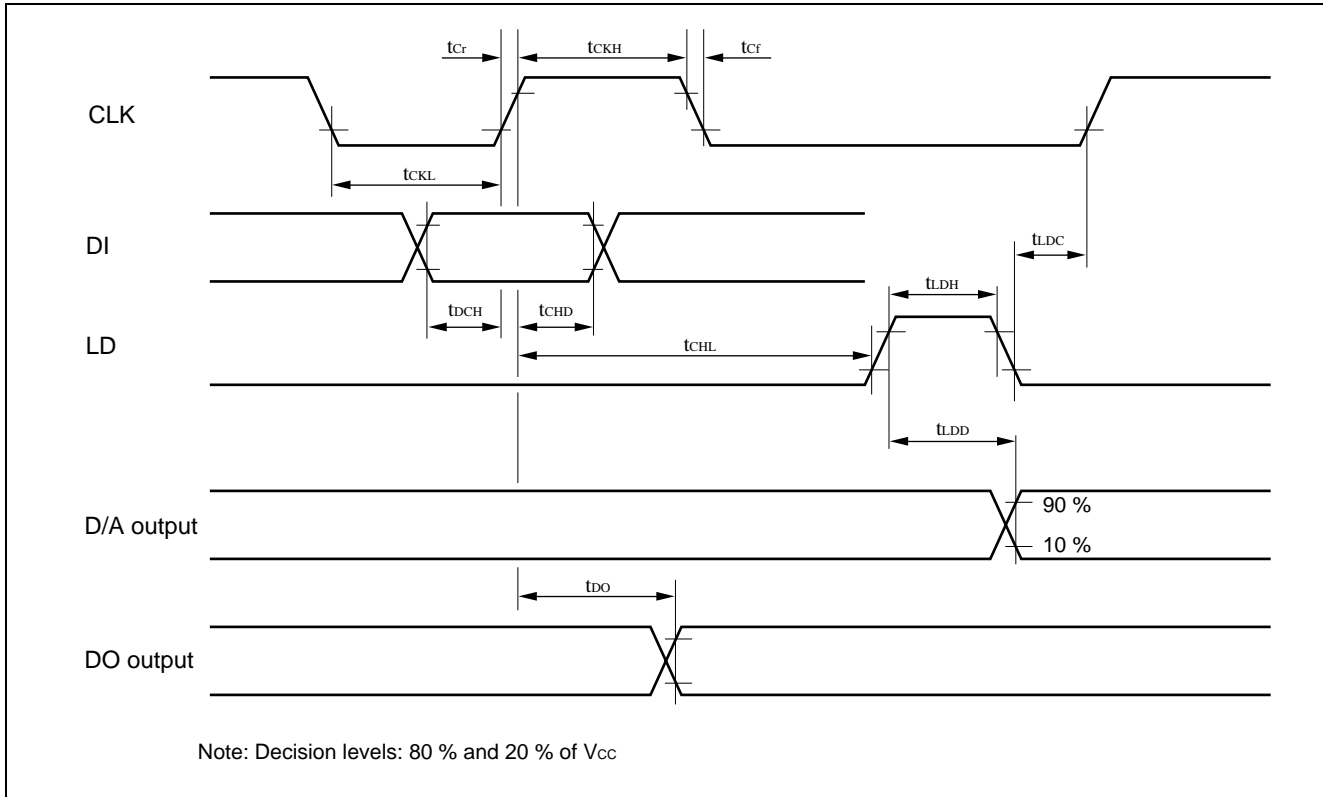


• Load condition 2

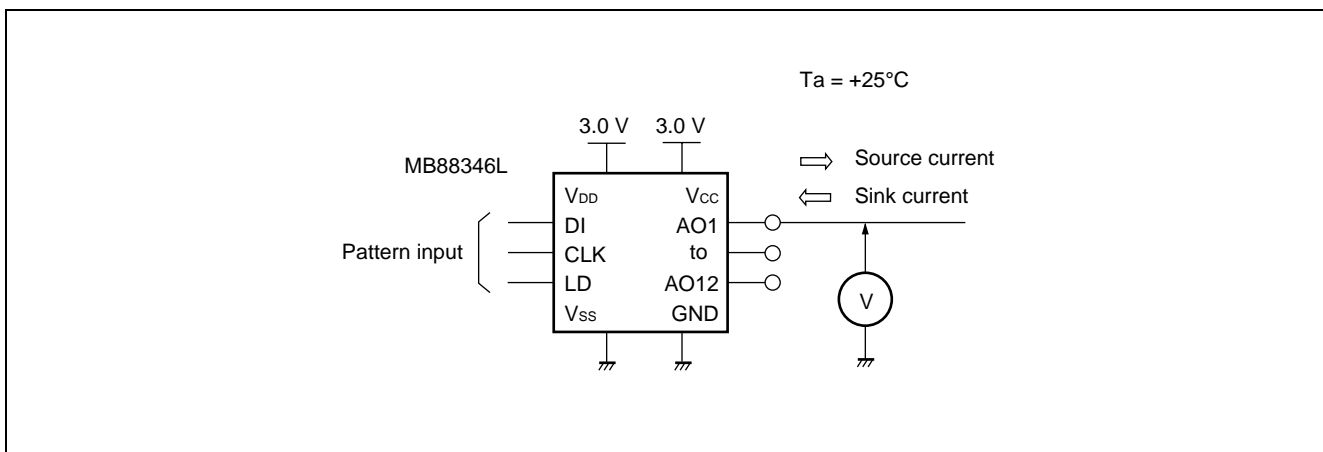


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• Input/output timing

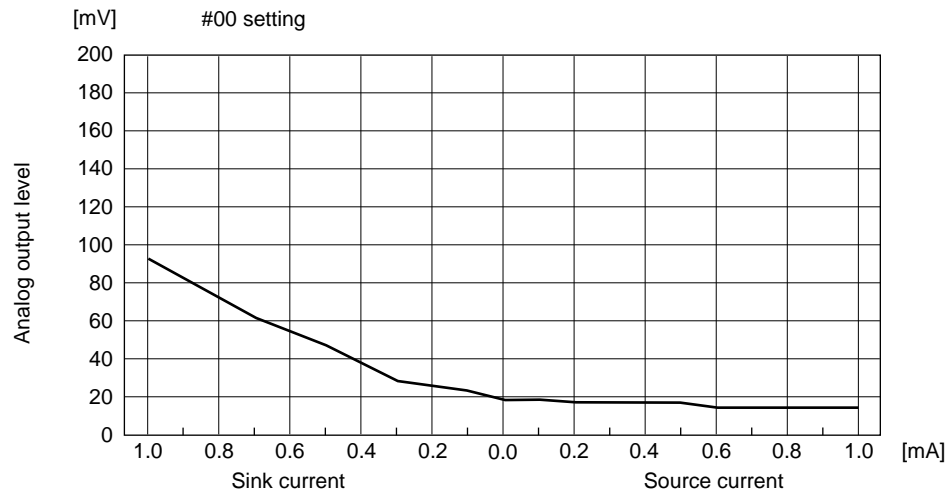
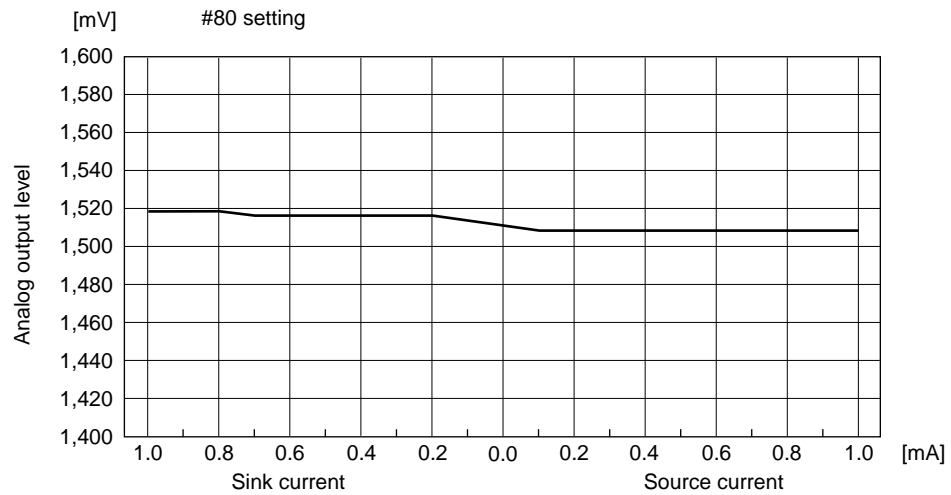
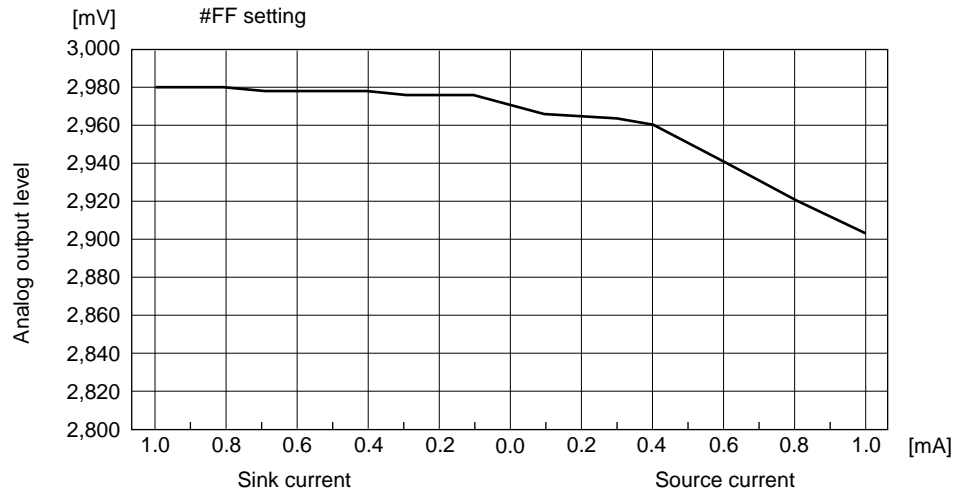


■ V_{AO} vs. I_{AO} CHARACTERISTICS: EXAMPLE



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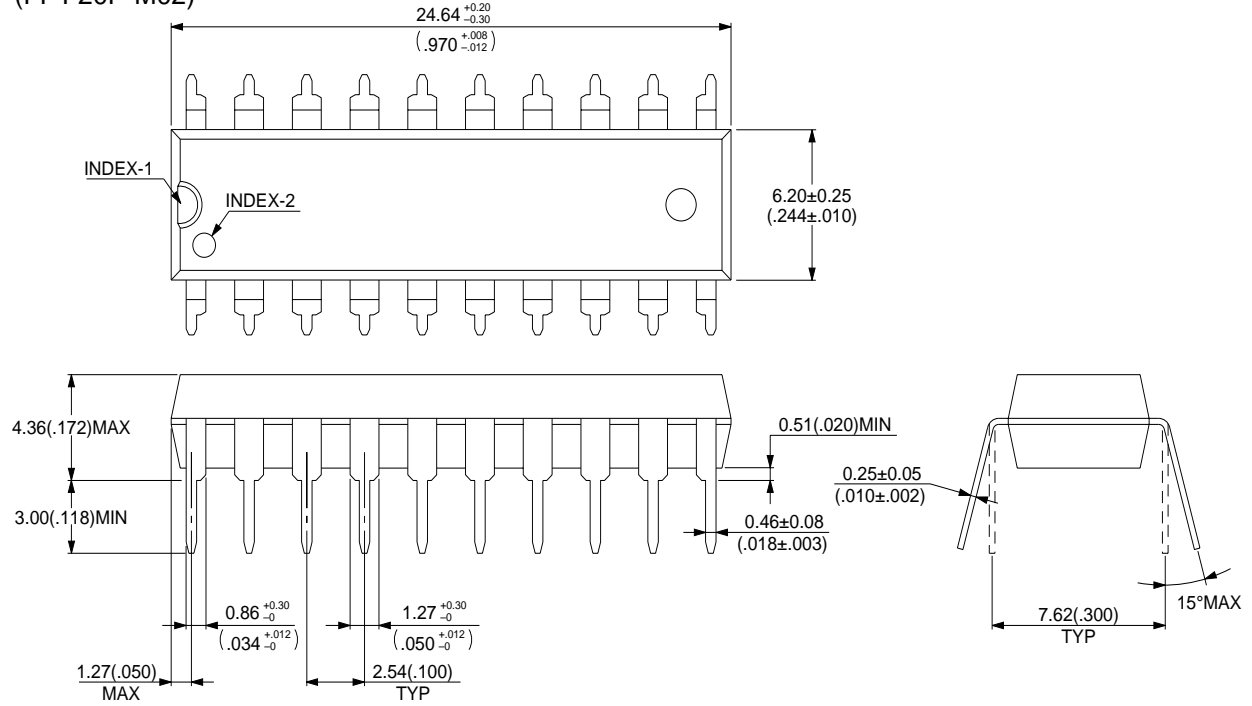
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■ ORDERING INFORMATION

Part number	Package	Remarks
MB88346LP	20-pin Plastic DIP (DIP-20P-M02)	
MB88346LPF	20-pin Plastic SOP (FPT-20P-M01)	
MB88346LPFV	20-pin Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSIONS

20-pin Plastic DIP
(FPT-20P-M02)



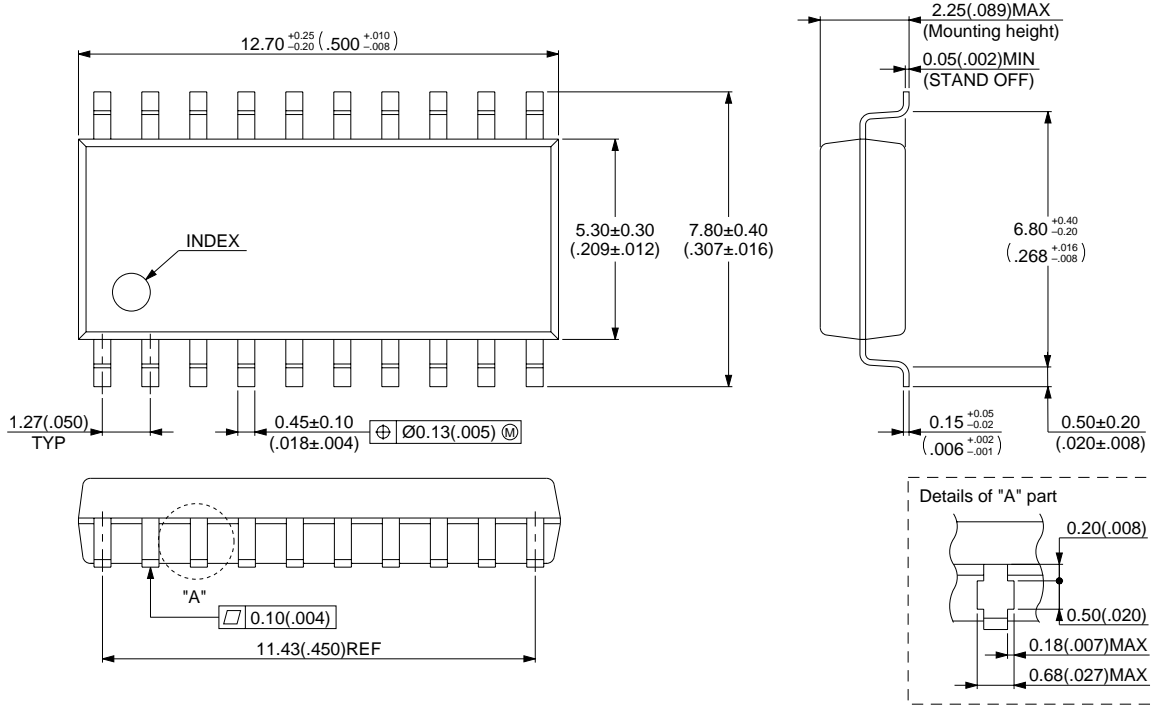
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Dimensions in mm (inches).

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20-pin Plastic SOP
(FPT-20P-M01)



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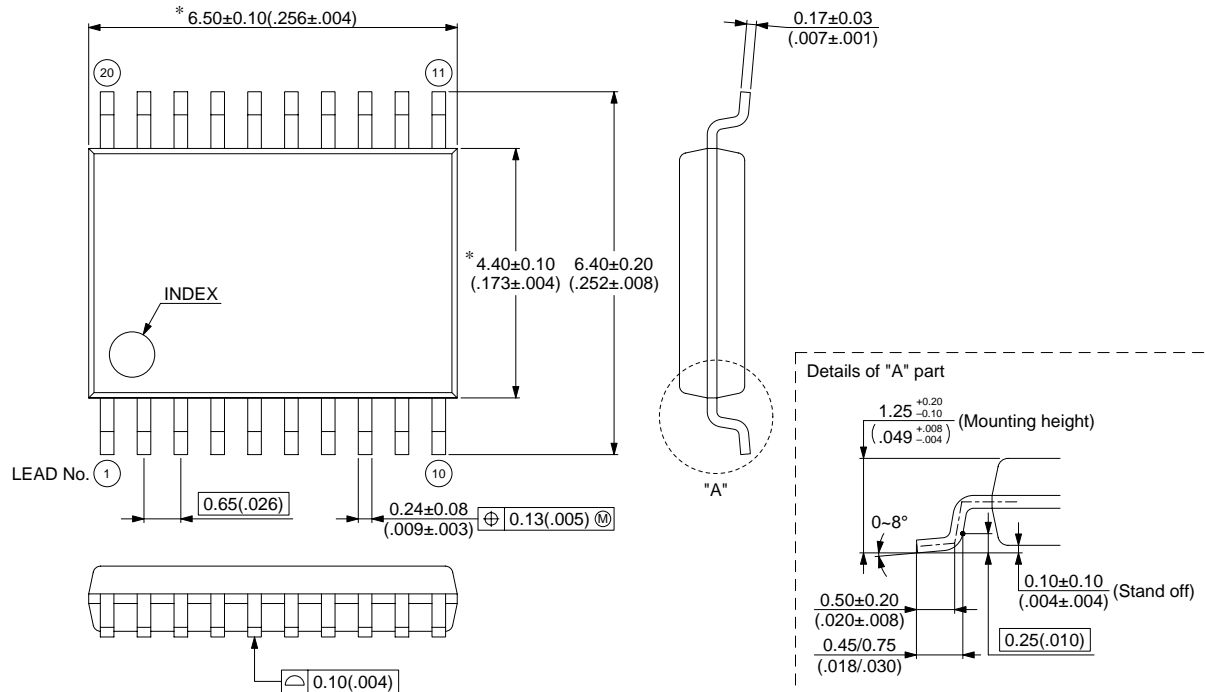
Dimensions in mm (inches)

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20-pin Plastic SSOP
(FPT-20P-M03)

Note 1) *:This dimension does not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)

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